Improving manufacturability of highly scaled RF GaN HEMTs

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Abstract

HRL's 40 nm T3 GaN MMIC process offers a unique combination of high fT/fmax, breakdown voltage, power, gain, low-noise, and high efficiency at mmW frequencies for both transmit and receive mmW RF applications. HRL recently started offering a T3 GaN foundry service to customers with a mature process-design-kit (PDK) and prototyping services on multi-project-wafer (MPW) foundry runs. This report describes the efforts made to improve yield and manufacturability for the T3 MPW foundry. Improvements in nitride passivation, selective area n+ GaN regrowth, ohmic metal spec limits and e-beam lithography have all improved yield and reduced rework rates while maintaining device performance.

INTRODUCTION

The unique strengths of HRL's 40 nm T3 GaN technology are summarized in Table 1, with a comparison between the legacy T3 process (prior to beginning of GaN process maturation programs) and the updated T3 process, focusing on key device parameters.

TABLE I
Improvements in key FET electrical parameters between Legacy and Updated T3 processes

Parameter	Median ± std. dev. (Legacy T3)	Median ± std. dev. (Updated T3)
f_T (GHz)	132 ± 21	134 ± 12
Peak transconductance, $g_{m,peak}$ (mS/mm)	783 ± 255	817 ± 76
Breakdown Voltage, BV (V)	77 ± 16	72 ± 15
FET On-resistance, R_{on} (ohm-mm)	0.87 ± 1.8	0.85 ± 0.07
Pulsed-current density at V_{Knee}, Idn (mA/mm)	508 ± 135	719 ± 110

These FET characteristics enable high efficiency, high power, low noise, and excellent bandwidth and gain at the MMIC level, with load pull at Ka-band delivered 2.3 W/mm of output power at 12 V and 2.7 W/mm at 14 V. HRL has leveraged this to successfully demonstrated a wide range of T3 RF MMIC components [1-2]. In recent years, HRL has substantially updated the legacy T3 process to improve yield, reproducibility, and manufacturability and facilitate an open access foundry offering. External customers have been designing into this foundry service and demonstrating their own novel MMIC power-amplifier prototypes [3-4]. Offering these open access foundry services in a high-mix low-volume fab environment has required a dedicated focus on improving key areas of device performance, while also improving device manufacturability.

T3 FABRICATION IMPROVEMENTS

Figure 1 shows four areas of manufacturing improvements that have resulted in improved control over key parameters in the updated T3 process: 1) implementation of MBE SiN surface passivation, 2) improvements to the n+ GaN MBE ohmic regrowth process, 3) modification of the ohmic metal to n+ GaN regrowth critical dimension and 4) improvements in T-gate lithography and fabrication techniques.

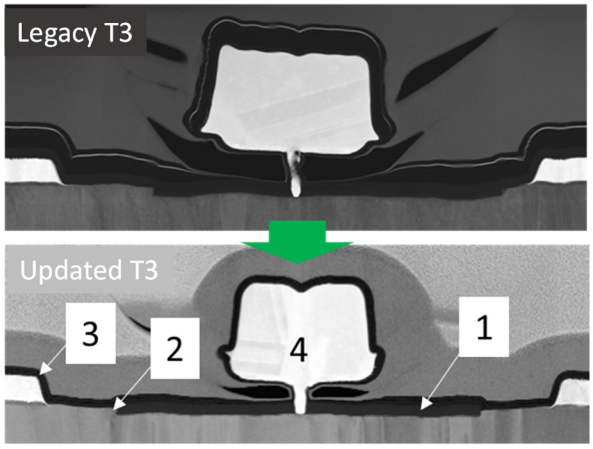

Figure 1. Cross-sectional images of the legacy (top) and updated (bottom) T3 gate processes. Highlighted areas include: 1) Implementation of MBE nitride passivation, 2) more consistent selective area MBE GaN regrowth, 3) more consistent alignment between ohmic metal and regrown GaN and 4) general improvements in e-beam lithography resulting in improved T-gate alignment, metallization and fabrication.

Figure 2 and Table 1 show the resulting impact on key FET characteristics. Variability in FET on-resistance, DC transconductance, current gain cutoff frequency (fT), and pulsed drain current density under quiescent bias stress (Idn) are all substantially improved with the updated process.

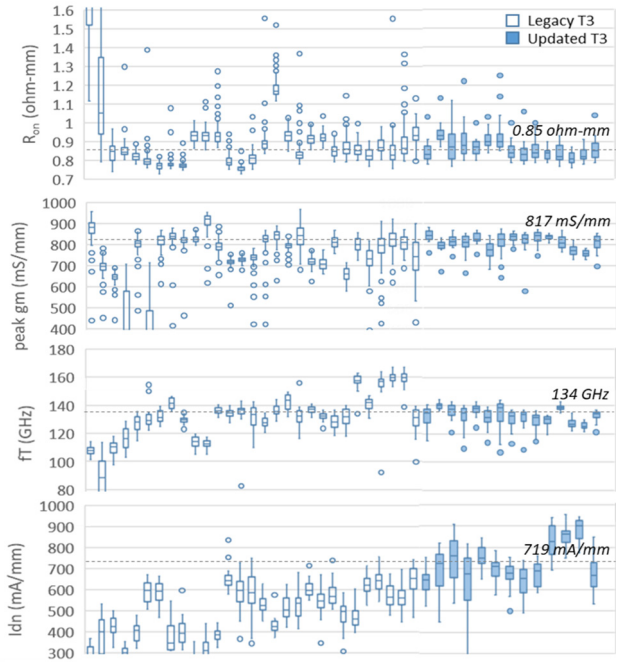

Figure 2. Manufacturability updates to the T3 GaN process have resulted in substantial improvements in control of key transistor electrical parameters. Measurements are from process-control monitor FETs, and each box represents 25 data points across one 100mm wafer

Of particular note is the substantial improvement in the pulsed drain current density, Idn. Idn is the drain current density measured in a pulsed IdVd measurement with the gate under forward bias (on-state), Vds=+2V, 200 ns quiescent stress, and off-state quiescent stress bias of Vds=+15V, Vgs=-5V. These conditions simulate large-signal RF operation and enable characterization of DC-to-RF dispersion – also known as current collapse -- due to trapping of electrons. Idn has been found to be a strong indicator of RF device performance, specifically for power handling of T3 devices. Passivation of the epitaxial surface using MBE SiN deposited in-situ in the growth chamber has resulted in substantially improved current collapse and Idn in the updated T3 process by improving control of the epi/SiN interface chemistry. As a result, the drain current density under large-signal RF operation is substantially increased, while maintaining high f_T, $g_{m,peak}$ and V_{bd}.

The n+ GaN MBE ohmic regrowth process and ohmic metallization processes were updated to improve device on-resistance consistency and reduce rework rate. The over-etch percentage of the GaN etch to define the n+ GaN contact

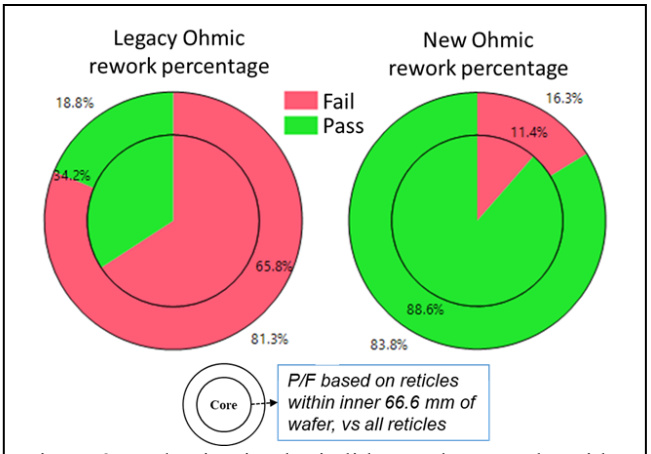

Figure 3. Reduction in ohmic lithography reworks with increased spec limits allowed by increasing the ohmic metallization lithography to n+ GaN regrowth setback by +50%

region was increased, while the target thickness of the regrown n+ GaN was also increased. This results in widening the process window for the regrowth process, ensuring that the etch depth is sufficient to guarantee exposure of the 2DEG, while increasing the n+ GaN thickness ensures that the regrown GaN will contact the 2DEG. The combination of both of these leads to consistently achieving the <1 ohm-mm R_{ON} metric which reducing cross-wafer variability (Table 1, Figure 2). To further minimize R_{ON} variability, and widen photolithography process windows, the setback of the

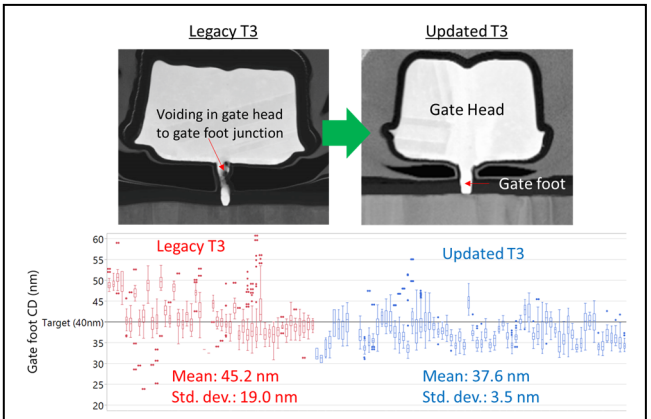

Figure 4. Top, highlighting of impact of T-gate e-beam lithography process improvements on the mechanical aspect of the T-gate. Bottom, impact of e-beam lithography process improvements on gate foot critical dimensions. Each box represents 25 data points across one 100mm wafer

photolithography for ohmic metallization was modified relative to the n+ GaN. Increasing this setback by 50% allows for more alignment tolerance during photolithography and results in a decrease of reworks for ohmic metallization photolithography from 66% to 11% for core reticles (Figure 3).

Finally, general improvements in e-beam lithography and the T3 gate etch process have improved gate critical dimension and alignment consistency in the updated process. The e-beam lithography resist development conditions were also optimized to improve tri-layer resist undercut consistency. As shown in Figure 4, these improvements not only reduce voiding in the gate head to gate foot junction and improved T-gate structural integrity, minimizing instances of gate tilting, but also more consistently achieve the targeted gate foot size. This results in improved control over key DC and RF electrical parameters, such as f_T (Figure 2), while also minimizing reworks for e-beam lithography issues.

CONCLUSIONS

Key process improvements are demonstrated here, succeeding in maintaining/improving key device parameters, while improving overall manufacturability of HRL's T3 GaN. Process improvements consist of MBE SiN surface passivation, optimization of the n+ GaN MBE ohmic regrowth process, tuning alignment tolerances of ohmic metallization and improving in T-gate e-beam lithography. These process optimizations resulted in a decrease in cycle time, while both improving device performance and reducing cross-wafer variability.

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