Reliability Assessment of 940 nm VCSEL Array based on Pulsed Mode Thermal Analysis

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Abstract

In order to obtain a relative accuracy of lifetime prediction of reliability test for VCSEL array device, the junction temperature (T_j) extraction has been investigated and analyzed in this manuscript. We propose a modified array thermal model which is achieved by unit area including 2 × 2 emitters based on the thermal characterizations of single emitter and array device. Adopting the additional parameters of thermal coupling and common thermal dissipation path into the model, peak and average T_j can be analyzed for the VCSEL array within 380 emitters under pulsed or CW operation.

To further verify the T_j extraction with a certain pulse condition, accelerated life testing (ALT) was performed for a criteria of 5 % power degradation at operating current (I_{op}). The array lifetime prediction can be analyzed by the calculation of temperature acceleration factor (E_A) and current acceleration factor (n) with the modified T_j value.

INTRODUCTION

In order to meet the requirements for data communication, current density of a single VCSEL is much higher than a typical emitter in a VCSEL array device for high power applications. Typically, reliability estimation/analysis of a datacom VCSEL is based on CW current stress [1-2]. With VCSEL array for high power applications such as 3D sensing and Time of Flight, there are the added concerns for eye safety requirements. Therefore these, array-type VCSEL devices are operated under pulse mode [3-4]. Achieving optimal electrical-to-optical conversion efficiency for each VCSEL emitter becomes critical especially for larger array VCSEL devices to minimize high power consumption and meet reliability requirements. In this work, we present a lifetime reliability analysis by the proposed thermal model for pulsed mode operation with a specific pulse width and duty cycle. It would be a modification to examine acceleration factor (AF) parameters to approach an improvement of lifetime prediction for accelerated life test (ALT) or high temperature operating life (HTOL) tests.

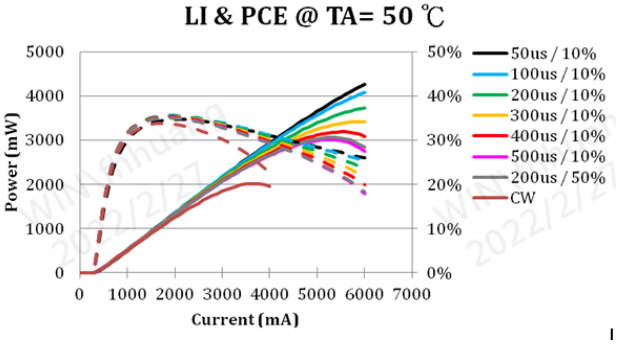


Figure. 1. Output power versus current at 50 °C for CW mode and pulsed mode with different pulse width.

VCSEL DESIGN

The tested chips are front side emitter VCSEL array with oxide-confined aperture. The ion-implantation makes isolation on the surface. The epitaxy is grown on an n-type GaAs substrate with three multi-quantum wells sandwiched between n-type and p-type distributed Bragg reflector (DBR) layers with an $Al_{0.98}Ga_{0.02}As$ layer above the MQWs for oxidation. In order to expose the oxide layer, the etching pattern is trench-type and is made by an inductive coupled plasma (ICP) reactive ion etching. The etch depth is controlled by in situ reflectivity measurement system. The oxide aperture is formed by the selective wet oxidation converting $Al_{0.98}Ga_{0.02}As$ to Al_xO_y at a specific temperature. The test VCSEL array device contains 380 emitter elements with emitter pitch of 31 µm, and chip size of 848 × 746 µm^2. Oxide aperture diameter of each emitter is about 10 µm. The test device was packaged via die attach to copper-plated TO can package for thermal management. The test device was evaluated for thermal and reliability characteristics.

Figure 1 shows light-current (*L-I*) curves and corresponding power conversion efficiency (PCE) from 50 to 500 µs pulse duration @ 10% duty cycle, 200 µs pulse @ 50% duty cycle and CW test conditions. The maximum PCE is close to 35 % at an optical output power of 1.3 W. Peak optical power reduces at longer pulse condition as expected due to thermal effect. Since reliability depends on the junction temperature, a proper pulse-mode output power is typically half of the peak power close to maximum PCE.

The operating output power of the test VCSEL array is around 2 W at the operating current (I_{op}) of 3 A (11 kA/cm^2).

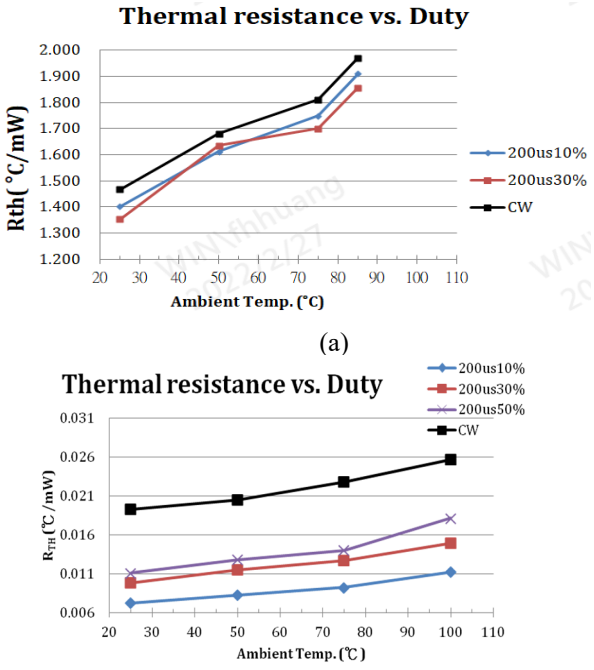


Figure 2. Thermal resistances versus duty cycles at threshold current level (pulse width=200 μs): (a) single emitter (duty cycle: 10 %, 20 %, and CW), (b) array device (duty cycle: 10 %, 20 %, 50% and CW).

JUNCTION TEMPERATURE EXTRACTION METHOD

According to the proposed method [5], emission spectra detection is general method to measure junction temperature (T_j) for single emitter VCSEL device, which is using wavelength shift to calculate T_j with wavelength temperature coefficient (R_λ) and the dissipated power as a function of wavelength:

$$T_j = T_A + (\lambda_1 - \lambda_0)R_\lambda \quad (1)$$

where R_λ is wavelength temperature coefficient (nm/°C).

However, the effects of thermal coupling and mode hopping usually occur in VCSEL array devices with large number of single emitters, which would lead to temperature detection error and an underestimation of T_j characteristic. For a high-power semiconductor laser, the modified T_j measurement has been proposed with regard to electrical-to-optical conversion efficiency [6].

$$T_j = T_A + R_{TH} \times (I \times V - P_O) \quad (2)$$

$$R_{TH} = \frac{\Delta°C}{\Delta W} = \frac{\Delta°C/\Delta\lambda}{\Delta W/\Delta\lambda} = \frac{1}{R_\lambda \times R_{diss}} \quad (3)$$

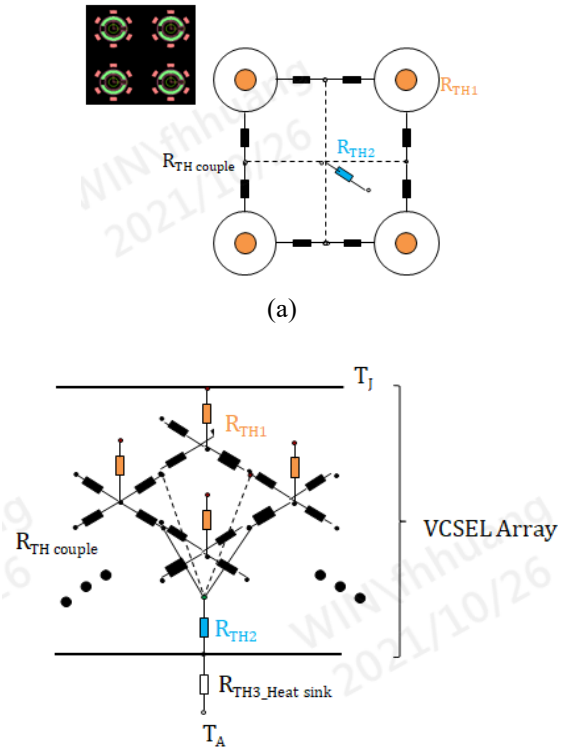
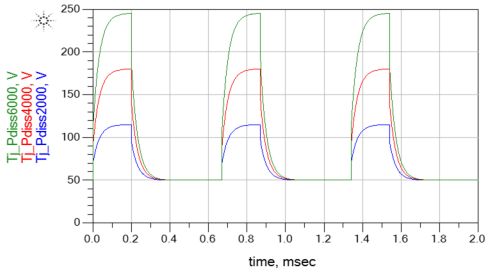


Figure 3. Thermal model of VCSEL array: (a) unit area (2×2 emitters) within thermal coupled $R_{TH,couple}$ and R_{TH2}, (b) the completed array schematic (380 emitters) with $R_{TH3,heat\ sink}$.

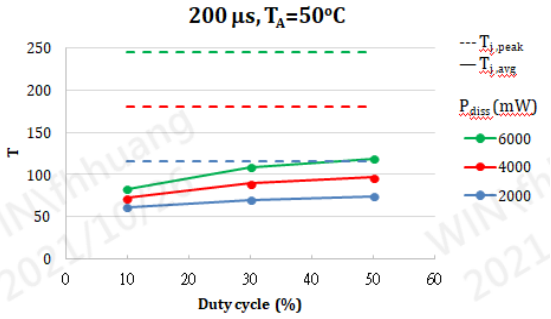
where P_o is optical power under operation current, R_λ is wavelength temperature coefficient, and R_{diss} is dissipated power as a function of wavelength. To measure R_{diss}, the peak wavelength must be recorded at the fundamental mode when the current is slightly above threshold current level.

Based on a typical method, R_{TH} were extracted for single emitter and array devices under pulsed operation with different duty cycles were analyzed as shown in Figure 2. The data shows that R_{TH} value is not a constant, but is dependent on T_A. At higher T_A operating condition a VCSEL quantum efficiency and optical power generally decrease this is equivalent to an increase in R_{TH}. Figure 2 (a) shows an almost ΔR_{TH} of 0.5 °C/mW in single emitter while setting T_A up to 85 °C. For an array device, T_j characteristic is also impacted by the emitter pitch and thermal dissipation capability from the heat sink. Figure 2 (b) demonstrates R_{TH} of the array device with the maximum T_A of 100 °C. The data shows that the overall R_{TH} value of the array VCSEL is lower than that of a single emitter. The measurement results imply that the peak T_j ($T_{j,peak}$) values are different for a single emitter and an array device when T_j is derived directly from R_{TH}. Theoretically, $T_{j,peak}$ should be the same value for a pulsed mode operation, when a single emitter and an array devices are driven at the same current density. This means that T_j derived by this method for each VCSEL emitter in the array device at I_{op} or higher applied current underestimates

the actual junction temperature in comparison to a single VCSEL at the same current density.



(a)



(b)

Figure 4. Simulation of thermal behavior (T_A=50°C, pulse width=200 µs): (a) transient waveform with power dissipations of 2.0, 4.0, and 6.0 W (duty cycle=20 %), (b) $T_{j,avg}$ and $T_{j,peak}$ with different duty cycles.

Furthermore, we can only detect average T_j ($T_{j,avg}$) at lower duty cycle due to the limitation of thermal measurement within the sampling detection limit [7]. In practical, the $T_{j,avg}$ is lower than $T_{j,peak}$. This makes difficult to perform an accurate lifetime analysis through the typical reliability test. To achieve improved estimate of T_j for reliability analysis, a modified thermal model for a VCSEL array is shown in Figure 3. Figure 3 (a) shows a unit area including 2 × 2 emitters. For a small pitch distance between emitters, 2 thermal resistances, $R_{TH,couple}$ and R_{TH2}, are adopted to describe thermal coupling effect and a common thermal path. Figure 3 (b) displays the completed model with heat sink ($R_{TH,heat\ sink}$). Based on the thermal model, we can analyze transient thermal behavior with any power dissipations (P_{diss}) and duty cycles by simulation. Setting P_{diss} at 2.0 W, 4.0 W, and 6.0 W, calculated $T_{j,peak}$ and $T_{j,avg}$ are shown in Figure 4 (a). To further make a precise T_j simulation, we calibrated the thermal parameters in the model by the measured $T_{j,avg}$ at various duty cycles. Figure 4 (b) shows the result of $T_{j,peak}$ and $T_{j,avg}$ versus duty cycles after the calibration. This means that we can determine the reasonable test conditions of duty-cycle dependence and current density for lifetime reliability test and analysis.

VCSEL Reliability Test

The most common accelerated aging is achieved by controlling current and junction temperature. The challenge is how to accurately measure junction temperature under pulsed mode operation, which can affect E_A extraction and lifetime prediction [4]. In order to understand the reliable operating conditions for the VCSEL array, MTTF test has been performed relying on $T_{j,modified}$ values which is a new factor calculated from $T_{j,avg}$ and $T_{j,peak}$. The test condition list for the test is presented in TABLE I, where the pulse width is 200 µs with duty cycle of 30 %. Figure 5 shows the plot of optical power degradation versus time with the test condition of I=4100 mA and $T_{j,modified}$=169 °C. The result exhibits a stable degradation of 8 % after 500 hours of stress without reaching the typical failure criteria, 10 % degradation. For the lifetime analysis, we set 5 % power degradation at I_{op} to be the failure criteria. Figure 6 plots the Arrhenius life-stress acceleration within 3 current densities and 3 modified temperatures, where the current densities were set at 11, 13.7, and 16.1 kA/cm^2, respectively.

TABLE I Current Densities and $T_{j,modified}$ Conditions for DC Stress

I (A)	J_D (kA/cm^2)	T_A=55 °C	T_A=70 °C	T_A= 83 °C
3.3	11.1			150 °C
4.1	13.7	127 °C	147 °C	169 °C
4.8	16.1		165 °C	

The unreliability for time to failure was set to be 50 %. After the time-to-failure analysis, we obtain the calculated AF values of temperature acceleration factor E_A=0.68 eV and current acceleration factor n=4.7 as shown in Table II. The experiment shows a high n value compared to the published reports [3]. This means that another electrical characteristic also impacts the reliability result besides the pulsed $T_{j,modified}$ extraction. The cause of the phenomena is the so-called lateral sheet resistance degradation which has been investigated in [8]. Due to the mechanism of a defect being generated in the oxidation and diffusing into the surrounding P-type mirror layers and diffusion/drift of the unpaired interstitial hydrogen donors into the surrounding isolation implant region, lateral junction causes an increase of threshold current. To remove the acceptor compensation effect, a process of high-temperature anneal has to be performed after oxidation process. Although the current acceleration factor is beyond the typical value, we tried to verify the lifetime prediction based on the MTTF test result. ALT was performed to check degradation trend with 96 samples. Figure 7 shows the trend of power degradation in the test. The samples were stressed tested at 11.7 kA/cm^2 with 10 % duty cycle, and $T_{j,modified}$ was set at 147 °C with T_A=85 °C. The optical output power was tested at I_{op} every

24 hours. The result depicts a reasonable estimate time around 4,500 hours to achieve 5 % power degradation.

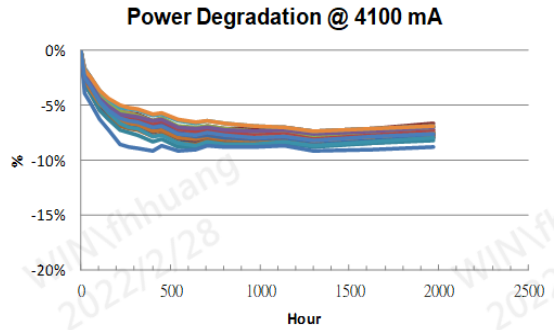


Figure 5. Optical power degradation plot at I=4100 mA and $T_{j,modified}$=169 °C.

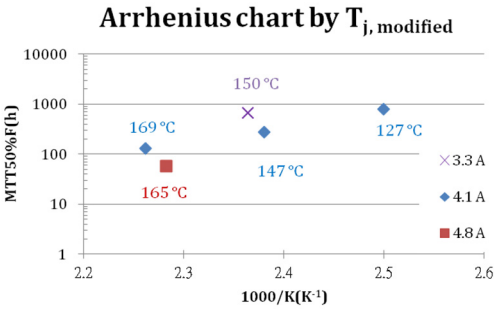


Figure 6. Arrhenius plot for a criteria of 5 % power degradation at operating current (I_{op}), where the current were set at 3.3, 4.1, and 4.8 A, respectively.

TABLE II ACTIVATION ENERGY (E_A) AND CURRENT ACCELERATION FACTOR (n) OF THE VCSEL ARRAY

Factor	This experiment
E_A	0.68
n	4.7

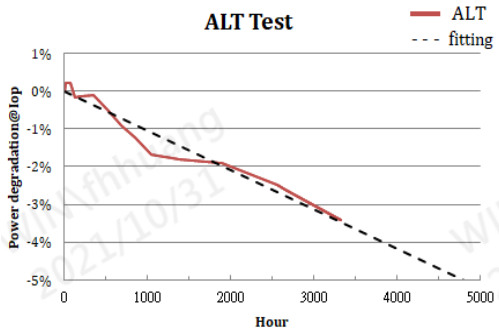


Figure 7. Power degradation trend chart in ALT test at operating current (I_{op}), and $T_{j,modified}$ was set at 147 °C.

CONCLUSIONS

This work demonstrates a lifetime reliability analysis for VCSEL array under pulsed mode operation. By contrast to the conventional T_j measurement, thermal coupling effects among emitters in the array and peak junction temperature analysis have been investigated. Through building up a thermal model with $R_{TH,couple}$, 2 temperatures, $T_{j,avg}$ and $T_{j,peak}$, can be easily obtained by the simulation of transient behavior with different power dissipations and duty cycles.

By the MTTF test result with the dedicated pulse width and the extraction of acceleration parameters, a non-typical n value presents in this experiment. To further modify the current acceleration factor, process modification and development of burn-in condition have to be taken into account for improving the device characteristic under high current operation. Based on this methodology for pulsed-mode thermal analysis, we now have a model to accurately predict the lifetime of array VCSEL devices under a specific pulse width and duty cycle.

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