1E7 Hours MTTF At 200 °C Of 100V RF AlGaN/GaN-SiC HEMT Through ALT Characterization

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Abstract

Ten million hours median time to failure (MTTF) at 200 °C channel temperature is reported for RF GaN-SiC HEMT operating at 100V. Data is extrapolated from accelerated life testing (ALT) at three temperatures: 300°C, 315°C and 330°C. In order to capture significant statistical variations 10 ALT representative samples for each temperature were sorted from two wafers coming from different lots. Failure is set at 20% degradation in saturated drain-source current (I_{DSS}). The AlGaN/GaN on SiC HEMT technology characterized at 100 V is based on a 0.5 µm GaN process with back-via holes.

INTRODUCTION

Groundbreaking 2.3 kW single RF transistor amplifiers at UHF [1] have been reported recently by increasing operation beyond standard 50 V. Furthermore, a 5-kW single RF GaN transistor for L-band applications will be presented at IMS-2022 [2]. Achieving multi-kW power level in single RF GaN transistor amplifiers will be a major milestone in facilitating replacement of TWTA or other vacuum electron devices in mega-watt class RF systems. In order to enable this technology shift a new class of RF GaN transistors are required which can reliably operate at 100 - 150 V bias. Several advantages of operating RF GaN HEMT at higher voltage are: higher power density, higher efficiency, higher impedance and wider bandwidth; this paper is the first to address the reliability of high-voltage RF GaN HEMT.

Whenever a new semiconductor technology is developed and brought to market, obvious concerns about its reliability arise. Over the past 70 years a set of stringent tests have been developed to estimate the lifetime of any semiconductor technology in its intended operating conditions and environment [3 – 4]. A generally accepted figure of merit for good reliability is a lifetime in the field of 10 million hours at a channel (FET) or junction (BJT) operating temperature of 200 °C. The characterization technique developed to estimate or extrapolate such lifetime is through accelerated life testing where a pool of semiconductor devices is operated at elevated temperature to intentionally induce failure and measure the time it takes for 50% of the samples in each pool to fail. ALT characterization eliminates a poorly designed technology that would result in too short lifetime while also comparing a new to a baseline technology. In this paper ALT characterization is described for an RF AlGaN/GaN on SiC HEMT technology that operates at 100 V DC bias [5 – 6].

ACCELERATED LIFE TESTING CONDITIONS

Two wafers from two different fabrication lots are represented at each temperature. The test structure is representative of the product device FET design with respect to geometry, spacings, and dimensions. It is a 2 x 300 µm device with 0.6mm gate periphery. Devices were biased at 100 V with a power density of ~4.2W/mm (I_{DS} = 25 mA). The gate bias is independently controlled for each device to maintain the desired channel temperature T_{ch}, which is determined by a combination of infrared surface temperature measurement and SYMMIC (a thermal simulator software) thermal simulation. Regular down-point measurements are made in-situ at a lower temperature (80 °C) to assess device performance. A drop of 20% in I_{DSS}, which corresponds to about 1dB degradation in the device's output power capability from the initial value constituted a failure.

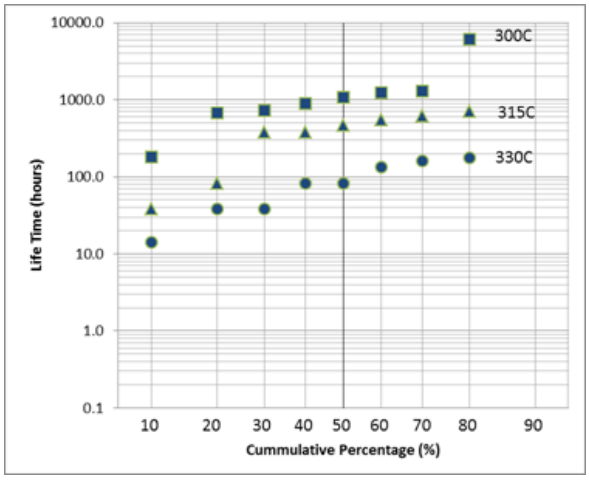

Fig. 1. Measured Lifetime on ALT samples at T_{ch} = 300, 315 and 330 °C at V_{DS} = 100 V, I_{DS} = 25 mA, resulting in a median time to failure of 1,080, 469 and 82 hours respectively.

At a channel temperature T_{ch} = 300 °C results indicate a lifetime of 1,080 hours; at T = 315 °C lifetime is 469 hours, and 82 hours at 330 °C. In Figure 1 the failure time of each device characterized is reported against the cumulative percentage in the sample. The measured lifetime at a 50% cumulative failure rate is then used in the Arrhenius plot to determine activation energy and most important lifetime extrapolated at T_{ch} = 200 °C. Arrhenius plot of the measured lifetimes at 100V for T_{ch} = 300 °C, 315 °C and 330 °C shown in Figure 2 yields an activation energy of 2.64 eV. For comparison, the plot also reports data taken at 50V on a baseline 50V GaN HEMT process, which yields an activation energy of 1.85 eV. At 200 °C channel temperature, both data sets extrapolate a lifetime in excess of 10 million hours which is indicative of a good reliability benchmark. Additionally, the results suggest that the design of the 100V GaN process has not introduced a new failure mechanism [7 - 8] which would have manifested itself in a shorter lifetime, or a statistically different activation energy. This aspect is extremely important and is supported by TCAD simulations which indicate the peak electric field in the channel and drift regions to be virtually identical in the 50V and 100V designs.

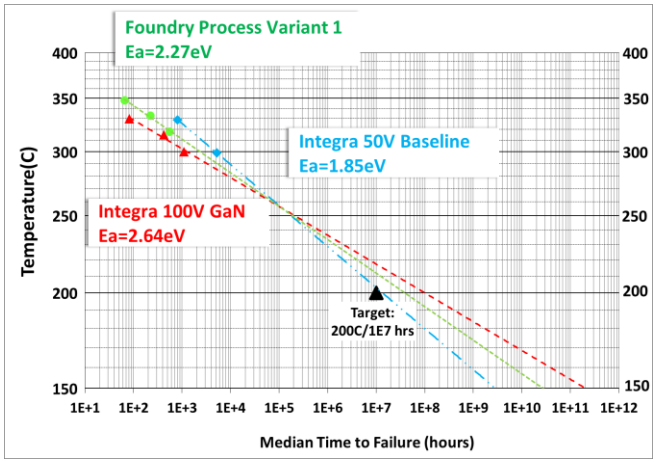

Fig. 2. 100 V Arrhenius plot compared to 50 V baseline. Activation energies are 2.64 eV and 1.85 eV, respectively. At T_{ch} = 200 °C both technologies exceed 10 million (10^7) hours.

Design Challenges

Failure mechanisms in GaN have been well documented in the literature over the last 15 years or more. A summary of the various identified mechanisms and where in the FET they occur is illustrated in Figure 3 [9]. The mechanisms of particular concern when operating at high voltages are highlighted and will be discussed further.

The design challenge is to keep the peak electric field below a critical value, E_{crit}, at which the combined stress from the designed lattice mismatch in the epitaxial layers and the induced stress from the inverse piezoelectric effect exceed the yield strength of the crystal, resulting in a crack. This translates into local stress relaxation along the drain edge of the gate, and a decrease in Ids at a given gate voltage. Electron trapping in the Silicon Nitride (SiN) above the drain access region can result from high electric fields generating hot carriers that can be injected and trapped in the SiN, forming a virtual gate (negative charge that interacts with the 2-DEG in much the same way as a negative voltage on the gate). This mechanism is best controlled by managing the SiN film quality and by appropriate surface preparation to control surface states. Minimizing E-field in the lateral dimension also reduces the energy imparted to hot carriers.

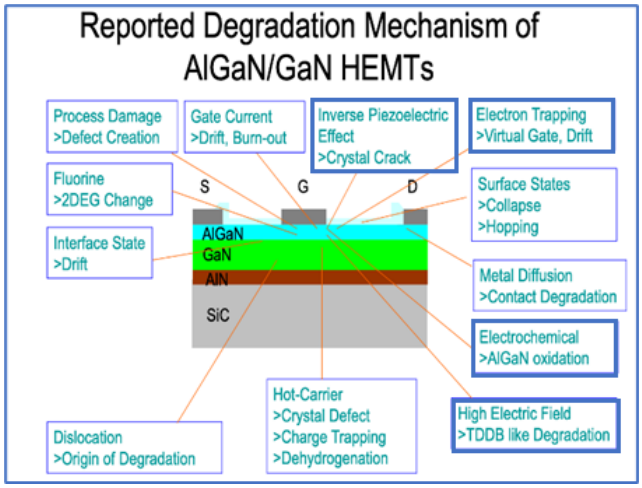

Fig. 3. Summary of identified failure mechanisms in AlGaN/GaN HEMTs [9].

Electrochemical oxidation of the AlGaN requires both electric field and the presence of oxygen of adsorbed water. The resulting defect behaves much like the crack formed from the inverse piezoelectric effect. The oxidation produces a local stress reduction at the gate edge and a reduction in Ids. Managing electric field in the FET design and process control are the primary levers to manage this failure mechanism.

The final mechanism of concern resembles the time dependent dielectric breakdown (TDDB) behavior of gate and capacitor dielectrics. The failure mode would manifest as sudden quantitative increases in gate leakage as breakdown occurs in local regions. Managing electric field and quality of epitaxial and deposited dielectric films are the primary levers to manage this failure mechanism.

We distinguish between these failure mechanisms by analyzing the time dependent behavior of the device under stress (e.g. degrading I_{dss} over time) followed by a detailed failure analysis and deconstruction of the failed device.

The levers available to a GaN FET designer in approaching operation at high voltages are epitaxial design, gate field plate design, and gate to drain spacing. If the peak electric field is managed such that the peak field in a 50 V

and 100 V FET design are similar, we would expect similar lifetime behavior in both cases.

TCAD simulations were used to compare peak field intensity for a 50 V GaN/SiC FET design and a 100 V GaN/SiC FET design. Figure 4 shows the critical electric fields for GaN and AlGaN for a 25% Al mole fraction. A less aggressive epi design (lower Al mole fraction) such as that used by Integra will have lower crystal stress and will be able to tolerate somewhat higher E-field, but these numbers will provide a useful reference. The simulation of electric field was carried out at twice the nominal V_{ds} to represent the RF swing the device will experience.

Fundamental Materials Capabilities	Conventional		Wide Bandgap				Ultra Wide Bandgap	
Property	Si	GaAs	4H-SiC	InN	GaN	$Al_{25}Ga_{75}N$	AlN	$In_{17}Al_{83}N$
Bandgap [eV]	1.1	1.4	3.3	0.7	3.4	**4.1**	6.2	**5.3**
Critical E-field [MV/cm]	0.3	0.4	2	?	3.5-4.0	**~7**	16	...
Thermal Conductivity [W/cm-K]	1.5	0.5	4.5	0.8	1.3	**2.35**	2	**1.8**

Fig. 4. Material parameters for nitride material systems.

Figure 5 illustrates the electric field intensity in the x (source-drain, or lateral) and y (normal) directions, and its magnitude, for the 100 V device biased at V_{ds} = 200 V and V_{gs} = -5 V. In this case the peak E_y field is -4.3 MV/cm at the gate edge. This is only 16% higher at twice the operating voltage of the corresponding 50 V GaN FET design and is well below the critical field of ~7 MV/cm for AlGaN. Given the similarity in peak electric field, it is reasonable to expect similar reliability performance when the devices are operated at their respective operating points.

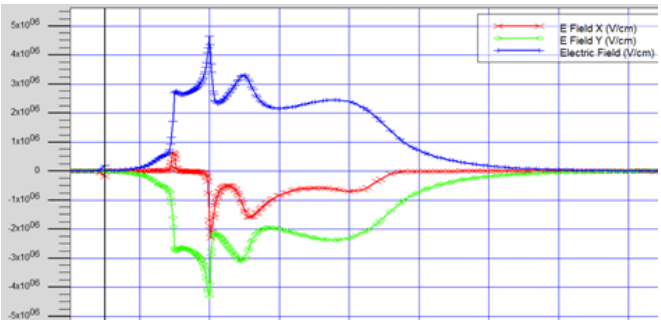

Fig. 5 E_x, E_y and E_{mag} for 100 V FET biased at V_{ds} = 200 V and V_{gs} = -5 V. Source is on the left; drain on the right.

Conclusions

ALT reliability characterization of a 0.5 µm AlGaN/GaN HEMT process designed for operation at 100 V has shown 10 million hours MTTF at 200 °C channel temperature. To the authors knowledge this is the first time that such groundbreaking result has been achieved.

Acknowledgements

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Acronyms

ALT: Accelerated Life Test
MTTF: Median Time To Failure