

# Dynamic $R_{on}$ in AlGaIn/GaN Structure with Different Layer Thickness

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## Abstract

The optimization of thickness for the undoped channel and carbon doped GaN layers in AlGaIn/GaN epitaxy are critical for improving the dynamic  $R_{on}$  characteristics in GaN power devices. We experimentally investigated the impact of changing the channel thickness using substrate bias measurements in short-loop fabricated device structures. It confirmed that a thicker undoped GaN layer/thinner carbon doped GaN layer can suppress the dynamic  $R_{on}$  characteristics, enabling rapid optimization of GaN buffers for GaN power device manufacturing.

## INTRODUCTION

GaN devices have been widely developed for use in high power switching applications due to their outstanding properties, such as wide energy bandgap, high breakdown voltage, and low on-resistance [1, 2]. However, dynamic  $R_{on}$  related to buffer trapping remains a major challenge which must be solved to reach the full potential GaN can offer for power devices. Although this phenomenon can be improved by various device design and fabrication methods such as gate formation [3], field plates [4], and  $\text{SiN}_x$  passivation [5], it is now critically necessary to optimize the epitaxy layer which remains the cause for most of dynamic  $R_{on}$  observed in commercially manufactured GaN power devices. Normally this requires the full processing of a GaN HEMT with all required field plates. Here we demonstrate that a short-loop process which only requires fabrication of a passivated Ohmic contact allows rapid assessment of the epitaxial sensitivity to dynamic  $R_{on}$  by using substrate ramp and transient analysis of simple TLM structures [6, 7]. We illustrate the effectiveness of this approach by varying the upper layer dimensions, since the buffer-related current collapse is mainly dominated by processes taking place in the upper undoped GaN and carbon doped GaN layers [8].

## EXPERIMENTAL DETAILS

Fig. 1 shows three power switching AlGaIn/GaN heterostructures used in this work. These differ only in the thicknesses of the undoped (U-GaN) and carbon doped (C:GaN) layers while the other layers were nominally identical. The total thickness of C:GaN and U-GaN was 1300 nm. This work was performed on a short-loop processed device structure which only used implant isolation,  $\text{Si}_3\text{N}_4$  passivation, and TiAl based Ohmic contact formation. With increasing U-GaN thickness, the sheet resistance decreased and 2DEG density increased ( $389 \Omega/\text{sq}$  &  $8.18 \times 10^{12} \text{ cm}^{-2}$ ,  $362 \Omega/\text{sq}$  &  $8.37 \times 10^{12} \text{ cm}^{-2}$ , and  $349 \Omega/\text{sq}$  &  $8.49 \times 10^{12} \text{ cm}^{-2}$  for wafer A, B, and C, respectively), which was extracted by measuring TLM and CV characteristics; all wafers exhibited similar vertical leakage current (not shown in detail). To confirm the buffer characteristics depending on the wafer structure, the substrate ramp and substrate stress current transient measurements were conducted [6, 9]. All the devices were tested on the large circular TLM pattern with a diameter of 1 mm and a contact gap of  $10 \mu\text{m}$  to reduce the impact of any lateral current flow effects within the epitaxy [10].

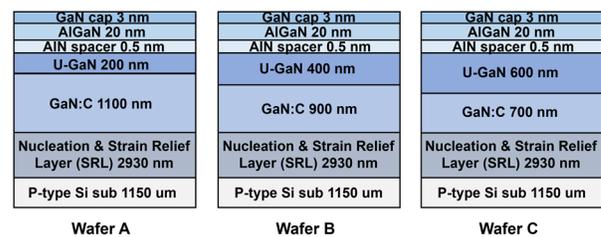


Fig. 1. Cross-sectional schematic of AlGaIn/GaN epitaxial structures for three wafers.

## RESULTS AND DISCUSSION

The substrate bias measurement shows the change in conductivity for the 2DEG channel by applying a substrate bias. This approach does not generate any change in electric field at the surface, but generates an electric field underneath the 2DEG, allowing the channel conductance to be surface insensitive and only affected by buffer-related transport and

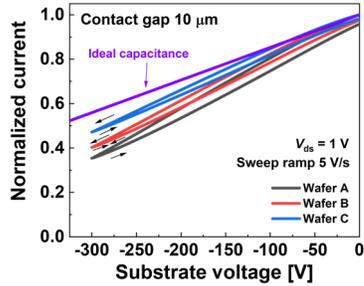


Fig. 2. Normalized channel current as a function of the substrate voltage of three wafers on the large circular TLM pattern with the contact gap of 10  $\mu\text{m}$ .

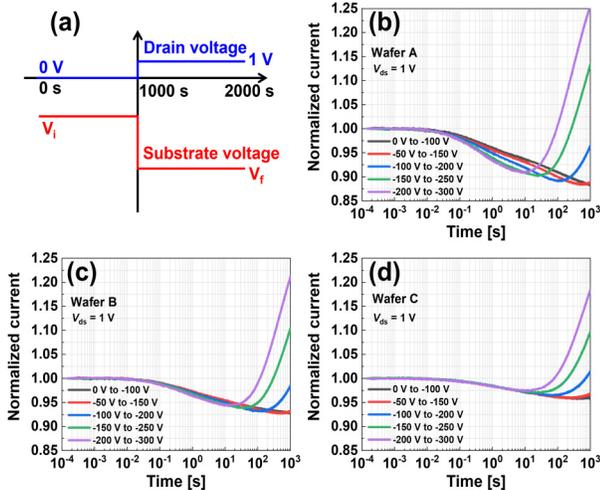


Fig. 3. (a) Measurement sequence for the stepped substrate transient. The transient characteristics for the bias points of constant potential difference for (b) wafer A, (c) wafer B, and (d) wafer C.

trapping effects [6, 7]. Therefore, this technique is a suitable technique to evaluate the actual epitaxy behavior under electrical stress.

Fig. 2 shows the substrate ramp characteristics of three wafers. Compared to an ideal capacitance line assuming the buffer is insulating, all curves lie below the line indicating negative charge storage in the buffer. The ramp characteristics with the thicker U-GaN layer were closer to the ideal line. This means that the thicker the U-GaN layer, the less negative charge in the buffer or less effect on 2DEG of trapped negative charges. Build-up of negative charge is directly linked to the dynamic  $R_{\text{on}}$  in power transistors [6].

Fig. 3 shows the results from stepped stress transients between two specific bias points with a constant substrate voltage step of -100V. This technique can be used to identify the dynamics of charge transport in the buffer [9]. This measurement shows an initial drop in 2DEG conductivity associated with negative charge (as also seen in Fig. 2), followed by a slow build-up of positive charge. This observation of negative/positive charging is normally observed in good quality power epitaxy, with the negative

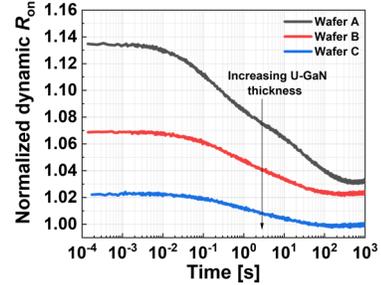


Fig. 4. Normalized dynamic  $R_{\text{on}}$  transients after switching from off-state ( $V_{\text{ds}} = 0 \text{ V}$  and  $V_{\text{sub}} = -150 \text{ V}$ ) to on-state ( $V_{\text{ds}} = 1 \text{ V}$  and  $V_{\text{sub}} = 0 \text{ V}$ ) of the samples.

charge associated with vertical transport in the GaN:C and the positive charge with leakage through the U-GaN layer. This result means that the charge redistribution in the GaN:C is more dominant at low voltage, but the band-to-band leakage occurs more easily as the voltage increases, resulting in a significant current recovery [8, 9]. We note that the magnitude of the negative charging reaches a maximum at around -150V for all epitaxies. The key new point here is that the magnitude of the undesirable negative charging is smaller for the thicker U-GaN/thinner GaN:C layers.

After changing the voltage, the magnitude of the current reduction was inversely proportional to the U-GaN thickness. It seems that the 2DEG channel of thin U-GaN is more affected by the vertical electric field in the buffer. The cause for this result might be related to the distance between the 2DEG and the trapped charge at the top of the C:GaN or the vertical electric field in the U-GaN, and it suggests the thick U-GaN layer reduces the buffer-induced current collapse.

In addition, all wafers show the current recovers during the measurement over -200 V, which means the dominant charge transport in the buffer changes from negative to positive at high voltage, and the dynamic  $R_{\text{on}}$  peaks at the substrate voltage of around -150 V. The behavior can be more clearly seen in the recovery transients in Fig. 4 (corresponding more directly to a conventional dynamic  $R_{\text{on}}$  measurement), where the normalized TLM conductivity is plotted following substrate bias stress with -150 V for 1000 s. Wafer A showed over 10 % increased dynamic  $R_{\text{on}}$  right after the stress and full recovery only occurred after 1000 s. On the other hand, wafer C exhibited little increased dynamic  $R_{\text{on}}$  and the channel was fully recovered around 100 s.

Based on these results, it is clear that the thick U-GaN/thinner GaN:C wafer exhibited good dynamic  $R_{\text{on}}$  characteristics under the stress. The 2DEG characteristics in wafer A were significantly affected under the stress, whereas wafer C suppressed the buffer-related current collapse with the thick U-GaN layer.

## CONCLUSIONS

Optimization of the layer thickness in the AlGaIn/GaN structure is necessary to control the impact of the buffer charge on the 2DEG channel, as basis for a GaN power device

manufacturing process. Using a short-loop process, and substrate back biasing, we demonstrated different dynamic  $R_{on}$  sensitivity in different epitaxy stack designs, and showed that a thicker U-GaN layer/thinner GaN:C layer is more effective in reducing dynamic  $R_{on}$ . This demonstrates the effectiveness of this approach in the optimization of power GaN epitaxy.

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#### REFERENCES

- [1] B. J. Baliga, *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074011, Jul. 2013.
- [2] K. J. Chen et al., *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779-795, Mar. 2017.
- [3] J. Möreke et al., *Phys. Status Solidi A*, vol. 209, no. 12, pp. 2646-2652, Dec. 2012.
- [4] W. Saito et al., *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1825-1830, Aug. 2007.
- [5] W. M. Waller et al., *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4044-4049, Oct. 2017.
- [6] M. J. Uren et al., *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2826-2834, Dec. 2017.
- [7] S. Stoffels et al., *IEEE International Electron Devices Meeting (IEDM)*, pp. 911-914, Dec. 2015.
- [8] M. J. Uren et al., *Jpn. J. Appl. Phys.*, vol. 60, no. SB, pp. 911-914, May 2021.
- [9] F. Wach et al., *IEEE Electron Device Lett.*, vol. 41, no. 12, pp. 1754-1757, Dec. 2020.
- [10] I. Chatterjee et al., *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 977-983, Mar. 2017.

#### ACRONYMS

(Al)GaN: (Aluminium) Gallium nitride  
U-GaN: Undoped GaN epitaxial layer  
C:GaN: Carbon doped GaN epitaxial layer  
2DEG: Two-dimensional electron gas  
Dynamic  $R_{on}$ : Dynamic on-resistance

