BiHEMT Idss Control for Yield Improvement

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Abstract

BiHEMT technology has achieved the goal of integrating heterojunction bipolar transistors (HBT) with pseudomorphic high electron mobility transistors (pHEMT). Advantages of BiHEMT include reducing the total size and cost of the chips as well as increasing design flexibility and circuit functionality. While probe yields have rapidly advanced to the point of maturity, there remain opportunities for yield improvements and understanding the basic science for enhanced process control. In this work a failure mode, high source-drain current (Idss) in the pHEMT structure of BiHEMT, has been systematically diagnosed, characterized, and eliminated. It was found that regions of high Idss were the result of an incomplete InGaP etch-stop removal beneath the gate, which provided an undesirable low resistance path from source to drain (Figs. 1-3). The issue was eliminated by integrating the GaAs gate layer (GL) etch with the subsequent InGaP etch-stop removal into a single multi-step process with superior within-wafer uniformity (Figs. 4 and 5). Eliminating the right-skewed tail of Idss gave rise to an increase in final yield of approximately 2.7% (Fig. 6). Potential mechanisms for the superior etch process are presented and discussed. The results show that etch quality, and resulting die yield, can in some cases be improved by combining separate processes into a seamless multistep process. Additionally, the integrated GL etch is at least 10% faster and is widely regarded as being more convenient to execute by fab personnel.

INTRODUCTION

BiHEMT technology has strongly delivered on the promise of integrating heterojunction bipolar transistors (HBT) with pseudomorphic high-electron-mobility transistors (pHEMT) [1]. Advantages of BiHEMT include reducing the total size and cost of the chips as well as increasing design flexibility and circuit functionality [1-3]. While probe yields rapidly advanced to the point of maturity, there are still opportunities for yield improvements as well as understanding the basic science for enhanced process control [1, 4].

GaAs-based devices, including BiHEMT, are commonly constructed by depositing a complex multilayer epitaxial stack and then essentially patterning down into the stack until the desired features are produced [1-5]. Accordingly, many critical steps are required to achieve consistently high quality and reproducible processes; and resulting devices. Material removal for microelectronics is typically categorized into dry and wet etch processes, both of which are indispensable for semiconductor manufacturing [6, 7].

Wet etching has some beneficial characteristics such as processing at atmospheric pressure, having high throughput, high material selectivity, and an absence of ion damage [7]. However, there are challenges as well such as surface wetting and reproducibly terminating etches with minimal feature variability [7, 8]. Suitable surface wetting is typically achieved either through the use of a surfactant, an oxygen plasma (to remove organics), or both [7, 9]. There are also some limited studies indicating that cyclical wetting (or prewetting) can render a surface more hydrophilic [10]. Lastly, feature variability can be minimized by incorporating etch-stop layers such as InGaP or AlAs into the multilayer epitaxial thin film [9, 11].

In this work a failure mode, high source-drain current (Idss) in the pHEMT structure of BiHEMT, has been systematically diagnosed, characterized, and eliminated. It was found that regions of high Idss were the result of an incomplete InGaP etch-stop removal beneath the gate, which in turn provided an undesirable low resistance path from source to drain. The issue was eliminated by integrating the GaAs Gate Layer (GL) etch with the subsequent InGaP etch into a single multi-step process with superior within-wafer (WIW) uniformity. Final yield increased by approximately 2.7% as a direct result of a 3.0% reduction in average Idss. This work demonstrates that high quality wet etches can in some cases be achieved not only with surfactants or oxygen plasmas, but potentially also by prewetting the substrates. Additionally, integrating the processes shows how both final yields and manufacturing productivity can be enhanced simultaneously.

Experimental Procedure

BiHEMT production was scaled to high volume at Skyworks Solutions Inc. and on-wafer test (OWT) parameters were subsequently reviewed. Particular attention was given to Idss as this is a critical parameter for device performance and yield [12]. A sample of wafers not meeting specification requirements were then cleaved and characterized with scanning electron microscopy (SEM).

After SEM was performed, the production line was segmented to determine potential sources of Idss yield loss. Once it was found that the Gate Layer etches were the source of the high Idss, experiments were performed to identify a suitable approach to eliminate the failure mode. Note that the GaAs etch is performed using a solution of H_2O, NH_4OH, and H_2O_2, while InGaP is etched with a solution containing H_2O and HCl. Wafers are mechanically rotated and agitated with N_2 during both processes.

Numerous lots were run with a newly developed integrated GL etch. The new process eliminates intermediate drying and inspection steps between the GaAs and InGaP etches. Lastly, probe data was collected so that the separate and integrated processes could be directly compared.

Results and Discussion

The results of ramping BiHEMT production using separate GaAs and InGaP etches showed intermittent "flare patterns" of high Idss, as shown in Figs. 1 and 2. Moreover, the orientation of these patterns could be controlled by changing the initial orientation of the wafers into the InGaP (HCl) bath. Cross-sectional SEM revealed that the InGaP etch-stop was not being fully removed during the HCl process, as shown in Fig. 3.

Fig. 1. Wafer map from separate GaAs and InGaP etch process showing characteristic "flare pattern" of high Idss (failing die shown in black).

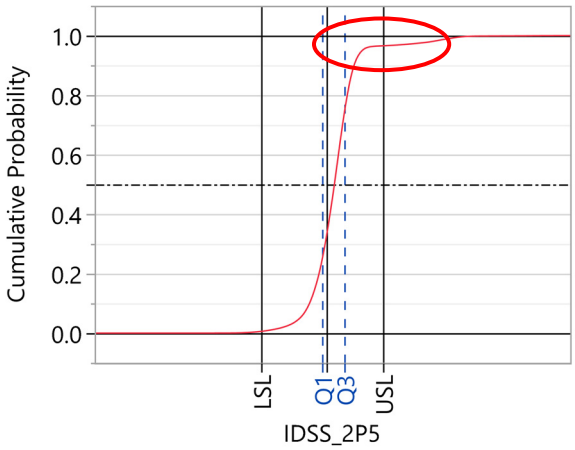

Fig. 2. Cumulative distribution of Idss for separate GaAs and InGaP etch process. Note the undesirable right-skewed tail beyond the upper specification limit. The percentage of die passing the spec limits is 96.1%.

Several hypotheses were developed and tested to determine the reason for the remaining InGaP. It was found that increasing dwell time of the wafers in the HCl bath by up to 50% did not reduce the under-etch issue. An alternative approach was attempted in which the wafers were neither dried nor inspected between GaAs and InGaP etches. Using the integrated approach, flare patterns of high Idss were eliminated as shown in Fig. 4.

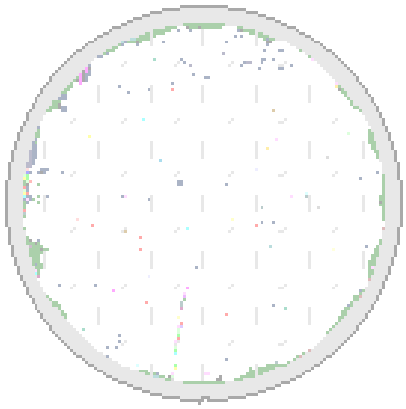

Fig. 4. Wafer map from integrated gate layer etch revealing elimination of "flare pattern" of high Idss.

The integrated GL etch was then scaled up to a larger volume and yield data was collected. On-wafer-test (OWT) showed a favorable reduction in average drain-source current of approximately 3.0% (Fig. 5), which corresponds to an improvement in probe and final yields of 3.6% (not shown) and 2.7% (Fig. 6), respectively. In addition to higher yield, productivity was also increased by 10% or more by eliminating intermediate drying and inspection steps.

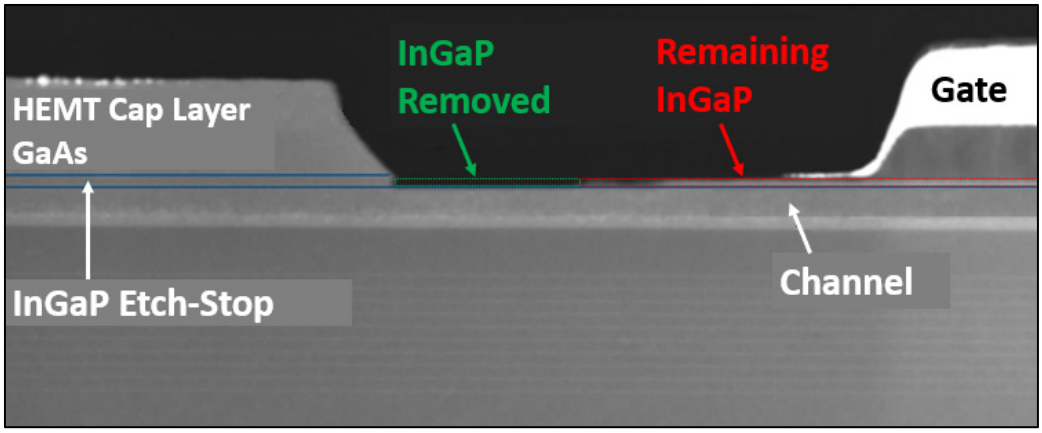

Fig. 3. Micrograph showing InGaP etch-stop undesirably remaining beneath pHEMT gate of BiHEMT device; providing low resistance path from source to drain.

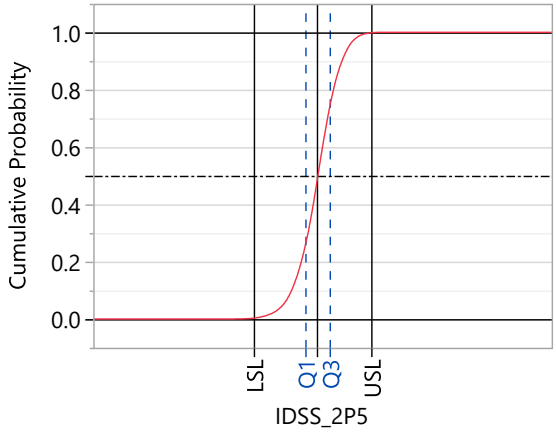

Fig. 5. Cumulative distribution of Idss for integrated GL etch process. The tail has been eliminated, as desired, by fully removing the InGaP etch-stop beneath the gates. The percentage of die passing the spec limits is 99.7% (an increase of 3.6 points).

It is thought that by immediately transferring the wafers from the deionized water rinse tank to the HCl bath, the wafers achieved more complete surface wetting due to a prewetting effect. After each etch step is completed (including the GaAs etch), the wafers are rinsed multiple times using a turbulent quick-dump-rinse (QDR) system. The turbulent spray of deionized water not only removes the etchant but also fully wets the wafers. This in turn reduces the surface energy and provides a favorable initial condition at the beginning of the InGaP etch. An alternative approach could be to add a surfactant to the HCl bath, although the integrated GL etch is still considered as the preferred option due to its simplicity, throughput, and surface cleanliness. It should be noted that after the InGaP etch is completed, the wafers are then metallized to produce the gates. Therefore, a pristine surface is critical for achieving excellent thin film adhesion and resulting device performance.

Conclusions

This study demonstrated that high source-drain current in pHEMT gates of BiHEMT devices could result from introducing dry wafers into an HCl bath for the InGaP etch-stop removal. End-of-line yield loss presented as “flare patterns” of high Idss due to InGaP remaining beneath the gates. The under-etch was eliminated by integrating the separate GaAs and InGaP etches into a single, multi-step process with superior WIW uniformity. Eliminating the right-skewed tail of Idss led to an increase in final yield of 2.7%, due to more die passing the specification limits.

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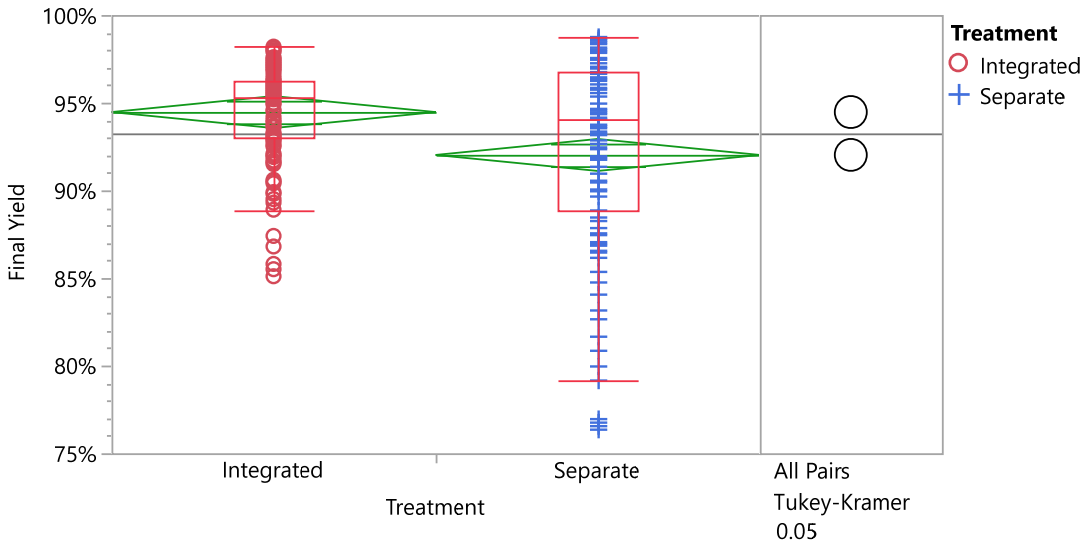

Fig. 6. Final yield (including die probe, PCM, and automated optical inspections) improvement arising from integrated gate layer etch process. The increase in final yield is approximately 2.7% and is statistically significant.

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ACRONYMS

BiHEMT: Monolithically Integrated Bipolar HBT and pHEMT
GL: Gate Layer
HBT: Heterojunction Bipolar Transistor
PCM: Process Control Monitor
PHEMT: Pseudomorphic High Electron Mobility Transistor
QDR: Quick Dump Rinse
WIW: Within Wafer