Characterization of Electrostatic Chuck (ESC) Performance with Changes in Wafer Warpage and Backside Cooling Conditions

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Abstract

Electrostatic chucks (ESCs) are used to clamp semiconductor wafers during processing and are integrated with back side gas (BSG) cooling to control the wafer temperature. The paired system has been designed with the assumption that the wafer is flat during processing, meaning that deviations in wafer bow can limit its performance. In the present work, ESC clamp quality is characterized by testing wafers with bow values in the range of 2 to 52 um under different chucking conditions. Results suggest a system to improve ESC/BSG performance with pre-process and in-process controls.

Electrostatic chucks (ESCs) are widely used to clamp semiconductor wafers during processing in various equipment such as dry etchers, vacuum based chemical-vapor deposition tools (CVD), and ion implantation tools [1-6]. An ESC clamp works by applying voltage to a dielectric layer between the wafer and a conductive electrode, which resembles a parallel plate capacitor. The bipolar electrostatic force clamps the wafer (top electrode) against the dielectric layer (insulator) [1,2]. Figure 1 shows a schematic diagram of the bipolar ESC in which an insulator layer is positioned on the bottom electrode.

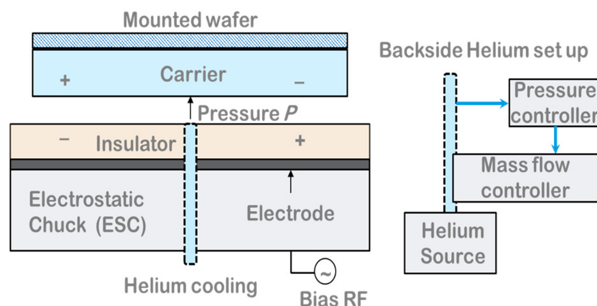

Fig. 1. Schematic Diagram of a Bipolar ESC

The ESC structure is integrated with back side gas (BSG) cooling to control the temperature of the wafer during processing. The cooling system introduces an inert gas with high thermal conductivity, such as helium, to the backside surface of the wafer. The cooling efficiency of the ESC system is determined by the heat transfer capability of the backside gas and the clamp uniformity across the wafer, which can be modeled by three energy systems: the electrostatic field of the charged ESC, the energy density due to backside pressure of the cooling gas, and the elastic strain due to wafer bow [1-4]. Thus, deviation in wafer bow is a limiting factor in the backside cooling of the chucked wafer. Semiconductor wafers might be bowed due to thinning or induced stress from previous process steps and it is critical to control the wafer flatness to obtain effective cooling at certain backside gas pressures.

To characterize the performance of the ESC/BSG system, full thickness wafers (150 mm in diameter) are mechanically bonded to two types of carriers (“A” and “B”) using a 50 um thermally curing adhesive layer, thinned to a thickness of 100 um with a grind process, then baked. The stack bow of these post-baked samples ranges from 2 to 52 um. The interaction of wafer flatness and ESC performance is studied by measuring the BSG flow during wafer clamping. Each sample is clamp tested multiple times by varying both the backside cooling gas pressure (ranging from 2 to 20 Torr) and the applied electrostatic voltage (5, 7.5, and 10 kV).

In ESC/BSG systems, leak-by flow of the cooling gas (helium) is measured as a gauge for clamp performance: a high amount of BSG leak-by flow means that the wafer is not properly clamped, and therefore the cooling gas is not reaching the wafer. Conversely, a low amount of leak-by flow represents a well chucked wafer with high cooling efficiency. In this case, He flow at or above 20 sccm represents complete clamp failure and tool fault. Figure 2 shows the leak-by flow of the cooling gas for the sample wafers prepared on type “A” and “B” carriers. At all applied voltages, the highest amount of BSG flow is seen for wafers with higher bow and the leak-by flow value has reached a maximum of 20 sccm. However, higher voltage conditions decouple the impact of bow on BSG flow, as long as the backside cooling gas pressure is low. In other words, BSG pressure needs to be derated to lower than ~10 Torr to clamp a bowed wafer, which results in tighter marginality of the backside cooling system and a higher chance of wafer overheating in high temperature processes such as plasma etch.

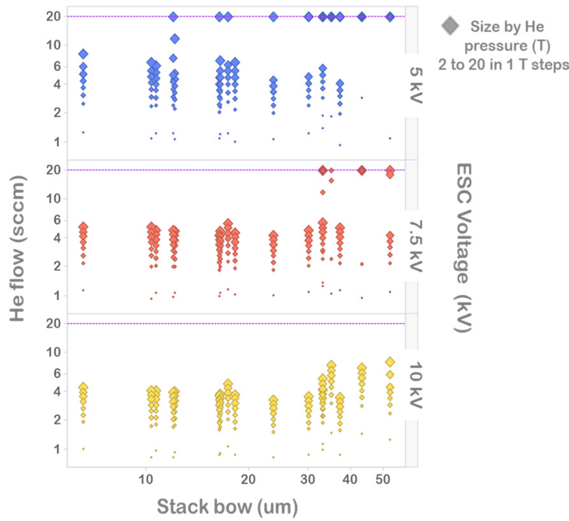

Fig. 2. Leak-by BSG Flow vs. Stack Bow at Various Clamp Conditions of Cooling Gas Pressure (2 to 20 Torr) and Electrostatic Voltage (5, 7.5, and 10 kV).

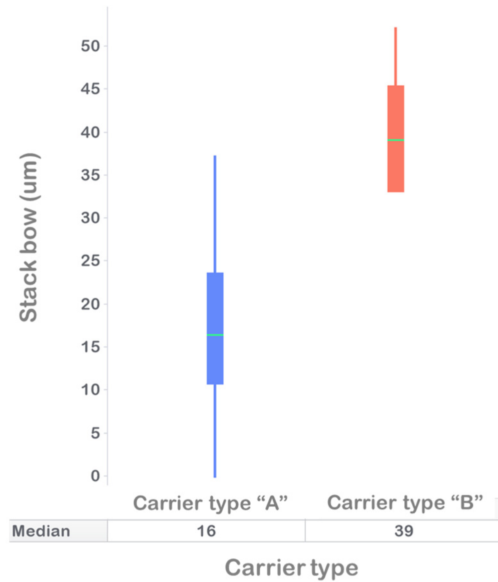

Fig. 3. Stack Bow vs. Type of Carrier

As stated, these proposed controls (i.e., varying clamp process parameters) to address highly bowed wafers will reduce process marginality. Therefore, methods to reduce stack bow were also investigated. It was noted during clamp testing that wafers mounted on type “A” carriers perform better than those mounted on type “B” carriers. In Figure 3, it can be seen the stack bow of wafers mounted on type “A” carriers is less than that of wafers mounted on type “B” carriers. The difference in stack bow between two carrier types can be attributed to the higher intrinsic Young’s Modulus value for type “A” carriers, meaning that they are less prone to warpage.

Although the rigid carrier is meant to maintain the planarity of the thinned wafer, the bow of the mounted stack will still vary throughout processing. Figure 4, consisting of type “A” carriers only, demonstrates this well. Due to the mismatch in coefficient of thermal expansion (CTE) between wafer and carrier, the high temperature bond process introduces stress to the bonded pair. The grinding process then introduces additional bow, attributed to the fact that the thinner wafer has increased flexibility, making the bow of the carrier the driving factor. A post-grind bake will reduce stack bow by initiating adhesive reflow to relive stress at the wafer, adhesive, and carrier interfaces.

In Figure 5, also consisting of type “A” carriers only, the final bow of the mounted pair is plotted against the carrier bow (pre-mount), uncovering an approximately linear correlation. It follows that choosing a carrier with lower bow will result in lower bow of the mounted pair.

Given these trends in stack bow, there are clear suggestions for bow reduction such as: choosing a carrier with higher Young’s Modulus value, adding a post-grind bake step to relieve stress, and limiting the bow of the carriers used in processing.

Investigating the impact of different bonding techniques on wafer bow is not included in the scope of this set of experiments, but it has been studied in the past. R. Trichur et al. reported that a thinner adhesive layer results in higher bow, and thus suggest a thicker adhesive layer to maintain the planarity of the wafer [7].

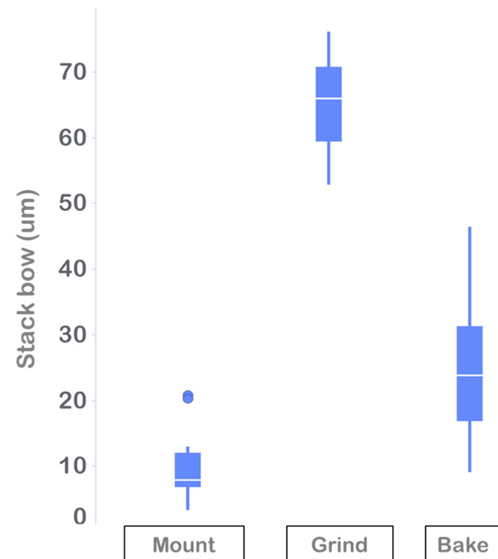

Fig. 4. Stack Bow Change vs. Process Step

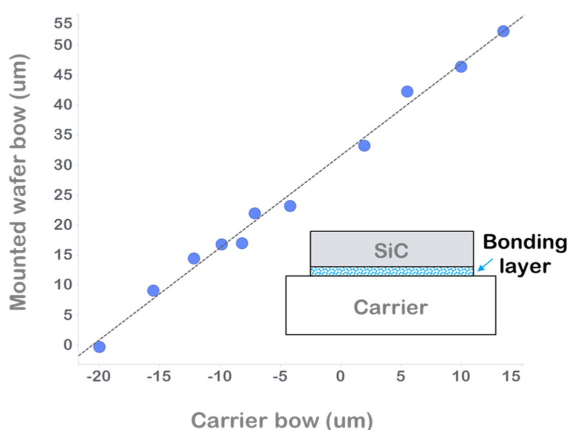

Fig. 5. Stack Bow Dependency on Carrier Bow

CONCLUSIONS

ESC/BSG systems are widely used in semiconductor equipment and therefore it is critical to identify control methods to protect against clamp failures and wafer overheating. The results of this study illustrate: (a) weaker performance of the clamping system as wafer bow increases, (b) higher electrostatic voltage applied to the chuck lowers the system's dependency on wafer bow, and (c) lowering the backside gas pressure will improve clamping under all bow conditions. The present work, focused on 150 mm wafers, demonstrates that wafers with high bow can be well chucked under certain conditions such as high ESC voltage and/or by reducing the BSG pressure. As noted, ESC parameter changes may diminish process marginality, so incoming wafer bow might also need to be controlled. For instance, mounting wafers on more planar carriers will result in lower bow of the final stack. Or, if the material of the carrier is already optimized, an added bake step can relieve stress from previous processes. The scope of this work includes only 150 mm wafers, and additional testing is required to evaluate ESC performance for wafers of different diameters. With several modes to address non-planar wafers, there is a clear path to improve system robustness of the ESC before applying the BSG.

REFERENCES

[1] Daniel L. Goodman, Journal of Applied Physics 104, 124902 (2008)

[2] Shu Qin, et al., Journal of Applied Physics 102, 064901 (2007)

[3] P. Kurkowski, et al., IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing 2005., 2005, pp. 127-129

[4] M. R. Sogard, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 25, 2155 (2007)

[5] K. T. Turner, et al., Journal of Applied Physics 92, 7658 (2002)

[6] M. R. Marks, et al., IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 4, no. 12, pp. 2042-2057, Dec. 2014

[7] R. Trichur et al., CS ManTech Conference, May 16th - 19th, 2016

ACRONYMS

ESC: Electrostatic Chuck
BSG: Back Side Gas
CTE: Coefficient of Thermal Expansion