Prevention of 1.2 kV SiC MOSFET from punch-through phenomenon by self-align channel process

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Keywords: self-aligned channel, mis-alignment, SiC, MOSFET, punch-through breakdown

Abstract

Shrinking the channel length is effective method to reduce the channel resistance, but the conventional SiC MOSFETs process wouldn't be suitable for short channel due to channel mis-alignment. Self-alignment channel process exhibits more advantages than a conventional process in aspect of a reliable device operation. We analyzed the effects of channel mis-alignment on 1.2 kV SiC MOSFETs compared to a device utilizing the proposed self-align channel process. Our results showed that the 1.2 kV SiC MOSFETs employing self-align channel process have stable V_T and BV values.

INTRODUCTION

SiC MOSFETs have known as attractive material for power device owing to high electric-field and thermal conductivity properties. It is a huge advantage of SiC MOSFETs to able to exhibit the identical blocking voltage with a thin drift layer than that of Si [1].

These properties of SiC MOSFETs provide its suitability for electric vehicle applications. Though their superior material properties, the device performance of SiC MOSFETs are limited by a low channel mobility and high amount of interface trap density between SiC and SiO_2 [2].

Due to the 4H-SiC MOSFETs have high densities of trapped electrons blow E_C which acts as negative fixed charges, electron mobility at inversion channel is typically degenerated [3]. Because low channel mobility cause deterioration of on-resistance at inversion channel, a short-channel structure is required for improving on-resistance of 1.2 kV SiC MOSFETs [4]. However, design of short channel may cause undesirable V_T and blocking characteristics [5].

In conventional procedure to form channel regions, alignment using two-different ion-implantation masks including p-base and n-source is carried out. Unintentional mis-alignment during process for channel formation cause an asymmetry channel length so that BV and V_T are considerably affected. Besides, the channel formation by alignment is one of reason for uniformity problems.

A self-aligned channel process is promising method to improve electrical characteristics and uniformity of 1.2 kV SiC MOSFETs. Several approaches have been reported to demonstrate self-aligned channel for SiC MOSFETs [6].

Cooper's group reported that SiC MOSFETs with short channels (≤ 0.5 μm) by applying a self-aligned channel shows low on-resistance [4]. In this paper, formation of SiO_2 spacer on a poly-Si ion-implantation mask is relatively simple method for formation of self-aligned channel compared to others so that identical channel length is obtainable at entire active area.

Our purpose is to figure out the failure mechanism of 1.2 kV SiC MOSFET with mis-aligned channel and the maximum allowable deviation of mis-alignment by analyzing the static characteristics such as V_T, R_{ON} and BV.

SIMULATION METHODS

Through Sentaurus TCAD Simulation, we constructed conventional device with consideration of mis-aligned channel and the proposed device employing self-aligned channel. Figure 1 shows cross section of the simulated 1.2 kV SiC MOSFET structure by Monte Carlo ion implantation and a thermal oxidation process. The lengths of the left and right channels were 0.5 μm, and the doping concentration and thickness of n-drift layer were 1×10^{16} cm^{-3} and 10 μm, respectively. Count doping was employed for control in the V_T with implantation conditions of N, 25 keV, 2×10^{12} cm^{-2}. P-base was formed with Al, 350 keV, 2×10^{14} cm^{-2}. Then, activation annealing was proceeded for 30 min at 1800 °C.

We simulated two types of devices with different processes for comparison analysis. Type 1 is a device applying a self-aligned channel process, and Type 2 is a device having a conventional process. The difference between these devices is the existence and nonexistence of channel mis-alignment.

In case of Type 1, channel was formed by etch-back process using deposited poly-Si implantation mask. For Type 2, channel was formed by twice patterning process for each p-base and n-source steps.

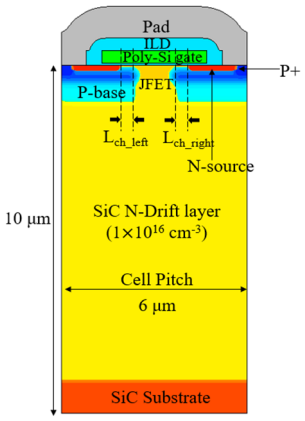


Figure 1. Schematic cross section of the 1.2 kV SiC MOSFET.

The channel mis-alignment of Type 2 devices were formed by intentional shift of the n-source mask, and the channel mis-alignment (ΔL) was defined as $|L_{ch\_left} - L_{ch\_right}|$. Channel mis-alignment (ΔL) was implemented from 0 to 0.35 μm.

Simulation Results

When the self-aligned channel process is applied, the channel deviation can be ignored, so that a device with a shorter channel can be manufactured. Therefore, we analyzed electrical properties, such as V_T, R_{ON}, and BV for Type 1 and Type 2 devices. In addition, we investigated the breakdown mechanism through distribution of electric field and E_C analysis.

Threshold voltage and On-resistance

Figure 2 and Table 1 shows the V_T and R_{ON} characteristics according to channel mis-alignment of Type 1 and 2. In the case of the V_T, the values tend to decrease as the channel mis-alignment increase. In particular, The V_T of channel mis-alignment of 0.3 μm and 0.35 μm are 2.19 V and 1.81 V, which are 21.5% and 35.1% lower than case of the self-alignment device, respectively. That is due to the charge sharing effect known as roll-off caused by the short channel. As the channel length decreases, the V_T decreases due to the increment of shared charge between the channel and the source. This unintentional reduction in the V_T may triggers a malfunction of the device [7]. Therefore, channel mis-alignment should be under 0.3 μm for stable operation.

In the case of R_{ON}, the values show irrelevant relation regardless of channel mis-alignment. As the short side of channel resistance decreases, the long side of channel resistance increases so that the total L_{ch} is constant as 1 μm. Therefore, the R_{ON} is not affected by the channel mis-alignment. It is not necessary to consider the R_{ON} in obtaining the maximum allowable deviation.

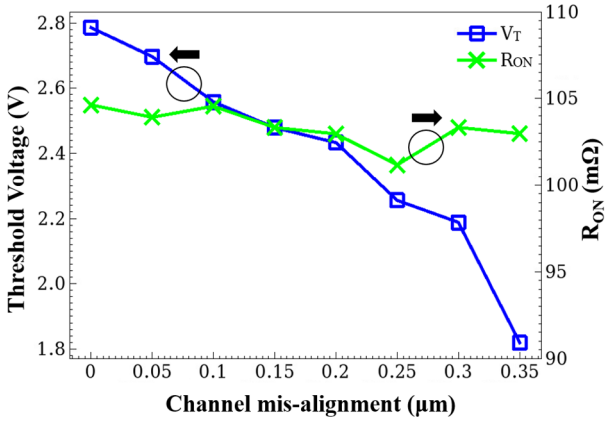


Figure 2. V_T and R_{ON} Characteristic according to misalignment

TABLE I
THRESHOLD VOLTAGE AND ON-RESISTANCE VALUES OF TYPE 1 AND 2

	Type	channel mis-alignment (ΔL)	V_T	R_{ON}
(a)	1	0 μm	2.79 V	104.01 mΩ
(b)	2	0.05 μm	2.70 V	103.92 mΩ
(c)	2	0.1 μm	2.56 V	104.56 mΩ
(d)	2	0.15 μm	2. 48 V	103.32 mΩ
(e)	2	0.2 μm	2.43 V	102.96 mΩ
(f)	2	0.25 μm	2.56 V	101.16 mΩ
(g)	2	0.3 μm	2.19 V	103.33 mΩ
(h)	2	0.35 μm	1.81 V	102.97 mΩ

Breakdown characteristics

Figure 3 show the BV characteristics according to channel mis-alignment of Type 1 and 2. The BV values are summarized in Table 2.

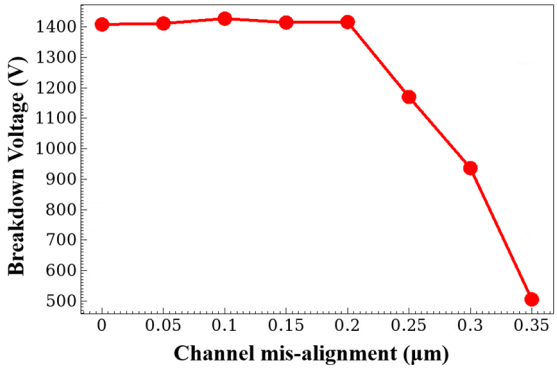


Figure 3. BV Characteristic according to misalignment

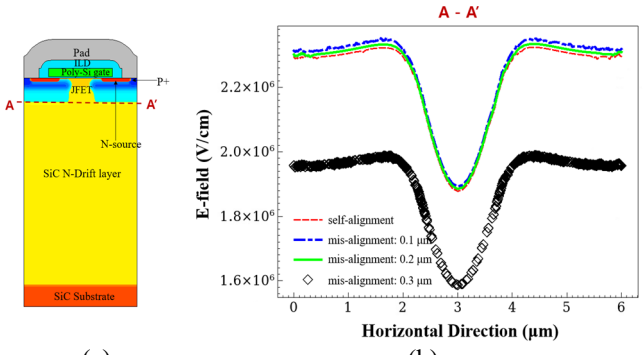
TABLE II
THE BREAKDOWN VOLTAGE VALUES OF TYPE 1 AND 2

	Type	channel mis-alignment (ΔL)	BV
(a)	1	0 μm	1408 V
(b)	2	0.05 μm	1411 V
(c)	2	0.1 μm	1427 V
(d)	2	0.15 μm	1414 V
(e)	2	0.2 μm	1416 V
(f)	2	0.25 μm	1170 V
(g)	2	0.3 μm	936 V
(h)	2	0.35 μm	505 V

The simulated SiC MOSFETs show BV over 1.4 kV when ΔL is less than 0.25 μm. However, it is significantly decreased above 0.25 μm. In case of the channel mis-alignment are 0.25, 0.3 and 0.35 μm, the BVs are 1170, 936 and 505 V which are 16.9, 33.5 and 64.1 % lower than those of the self-alignment, respectively. As a high voltage is applied to the drain region, an avalanche breakdown phenomenon occurs owing to carriers accelerated by a high electric field. In order to obtain reliable blocking in 1.2 kV SiC MOSFETs, the enough high BV over 1.4 kV is desirable (1.2 kV × 120 % = 1.44 kV). Therefore, considering the BV characteristics, the allowable channel mis-alignment is less than 0.25 μm.

ELECTRIC FIELD CHARACTERISTICS

Figure 4 shows electric field characteristics with cut-line of A-A' which is junction depth of p-base/drift interface when breakdown occurred. The highest electric-field was observed at p-base/JFET junction. When the channel mis-alignment was 0.3 μm, the peak value of electric field was under 2 MV/cm which is less than critical electric field of 4H-SiC. Therefore, the BV reduction with channel mis-alignment over 0.25 μm are not originated from impact ionization.

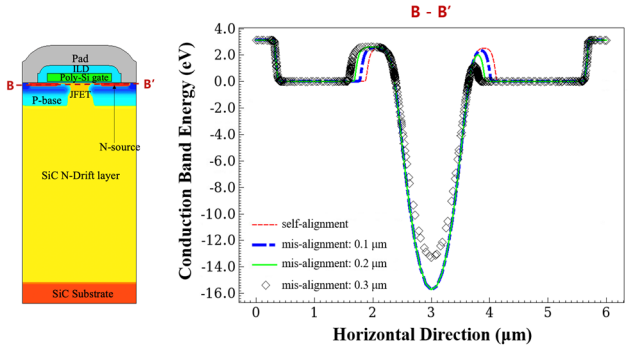


(a) (b)

Figure 4. Electric field characteristics when breakdown occur
(a) Schematic cross section of the 1.2 kV SiC MOSFET,
(b) electric field distribution at the A-A'

CONDUCTION-BAND CHARACTERISTICS

Figure 5 Shows E_C distribution of 1.2 kV SiC MOSFETs with cut-line of B-B' when the breakdown occurs. The energy barrier distribution shifts to the left owing to mis-alignment of p-base and n-source. As the channel mis-alignment increases, the energy barrier on the short channel decreases. In particular case of channel mis-alignment being 0.3 μm, energy barrier for electron was greatly decreased compared to self-alignment device.



(a) (b)

Fig. 5. Conduction-band energy
(a) Schematic cross section of the 1.2 kV SiC MOSFET,
(b) conduction-band energy distribution in the B-B'.

Referring to the results in Fig. 4 and Fig. 5, the BV reduction of the channel mis-alignment over 0.3 μm was result from the punch-through phenomenon. When the punch-through occurs, the short channel region is completely depleted. Punch-through causes the breakdown at a lower voltage than other cases where the avalanche breakdown occurs. Therefore, the maximum allowable channel mis-alignment that maintains electrical characteristics (V_T, R_{ON} and BV) without punch-through is 2 μm.

CONCLUSIONS

We analyzed electrical reliability of 1.2 kV SiC MOSFET with mis-aligned channel and evaluated the stability of the proposed device using self-align channel process. Our results showed that channel mis-alignment over 0.2 μm caused serious V_T deviation and punch-through breakdown so that the proposed device enables channel length to be shorten and potentially improve on-resistance in 1.2 kV SiC MOSFET.

ACKNOWLEDGEMENTS

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2021R1G1A1003487)

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ACRONYMS

SiC: Silicon Carbide
MOSFET: Metal-Oxide-Semiconductor Field-Effect -Transistor
BV: Breakdown Voltage
V_T: Threshold Voltage
R_{ON}: on-resistance
SCE: Short-channel Effects
TCAD: Technology Computer-Aided Design
E_C: Conduction-band energy
L_{ch}: Channel length