Hybrid Etching Process in Sub-micron Type-II GaAsSb/InP DHBT for 5G and millimeter-wave Power Amplification

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Abstract

A yield-enhanced process for Type II InP-based DHBT is presented with high controllability and uniformity. The process deploys systematic hybrid etching to form maximally-preserved BC mesa and complete isolation for the sub-micron device with complex epitaxial layers. High breakdown voltages (BV_{CEO} and BV_{CBO}) > 11V are achieved in a 0.4×8 μm^2 DHBT fabricated device. Excellent RF performance is also demonstrated for a 0.4×6 μm^2 device with f_T/f_{Max} = 135/245 GHz. The results indicate the promising capability of sub-micron InP DHBT for millimeter-wave power amplification.

Introduction

InP-based double heterojunction bipolar transistor (DHBT) has been widely used in high-speed mixed-signal integrated circuits due to its low turn-on voltage, high breakdown voltage, and superior transport properties [1, 2]. Generally, the InP DHBT can be categorized into two types (Type-I InGaAs/InP and Type-II GaAsSb/InP) based on the energy band alignments. Compared to Type-I DHBT, Type-II DHBT has a staggered base-collector (BC) heterostructure which eliminates current blocking and facilitates electron transport through the collector. The RF performance of Type-II InP DHBT can be further improved by reducing the transit time with vertical scaling of the base and collector epitaxial layers. Aside from reducing layer thickness, the device bandwidth can be increased by implementing compositional grading across the base. The parasitics due to thinner base and collector can be reduced to improve device speed by simultaneously downsizing the device topology. However, as the enhancement of RF performance is prioritized in many works, the breakdown voltage of DHBT has been compromised. In 2014, in collaborating with Dr. Berry Wu from Keysight technology, H. Xu at UIUC demonstrated a remarkable 0.5 THz performance of a type-II DHBT with a 0.38 × 5 μm^2 emitter and a 120-nm thin collector layer despite of a 6.5V breakdown voltage [3]. W. Snodgrass at UIUC also presented a record f_T = 670 GHz for a type-II DHBT with a 20-nm collector to reduce transit time yet at the expense of the breakdown voltage less than 5V [4].

While optimization for DHBT RF performance is intensively studied, approaches to enhancing its millimeter-wave power amplifying ability (which requires higher breakdown voltages with sufficient f_T/f_{Max}) need more research and development. Moreover, improving the manufacturing controllability becomes imperative, as DHBT scales down with a sub-micron emitter and yet possesses complex epitaxial layers. The lack of process uniformity during the traditional wet-etching attributes to performance degradation and even low yield. In this paper, we report a developed hybrid etching process to systematically address the existing issues. As a result, the fabricated sub-micron type-II GaAsSb/InP DHBT devices demonstrate breakdown voltages (BV_{CEO} and BV_{CBO}) beyond 11V as well as f_T/f_{Max} = 135/245 GHz, which make the devices viable for millimeter-wave power application.

Epitaxial Structure

The epitaxial structure of this work was grown on a 4-inch semi-insulating InP substrate by molecular beam epitaxy (MBE). The layers from the emitter cap to the substrate are summarized in Table 1, where T is the layer thickness. The emitter is designed with a 15-nm strained AlInP layer as an "emitter launcher" for hot electron injection at the emitter-base (EB) interface. The 40-nm carbon-doped GaAsSb base layer is compositionally graded to promote electron flow by a built-in field. The enhanced transport can significantly reduce the base transit time and increase device bandwidth. In addition, an InP collector with 450-nm thickness is used to achieve high breakdown voltages for device power handling capability.

Table I. Epitaxial layer structures of Type-II GaAsSb/InP DHBT

Layer	Material	Composition	T(nm)
9	$In_xGa_{1-x}As$	0.53	100
8	$In_xAl_yGa_{1-x-y}As$	x = 0.52 y = 0.19	35
7	InP	-	5
6	$Al_xIn_{1-x}P$	x = 0.1 → 0	15
5	$GaAs_{1-x}Sb_x$	x = 0.39 → 0.49	40
4	InP	-	450
3	$In_xGa_{1-x}As$	x = 0.52	10
2	InP	-	400
1	$In_xAl_{1-x}As$	x = 0.52	20
	InP	-	-

Device Fabrication Process with Hybrid Etching

The hybrid etching method is a combination of wet-etching and inductively coupled-plasma (ICP) reactive-ion-etching (RIE) to form the mesa structures, most importantly, to achieve isolation between the active device region and the base metal post. The detailed process of HBT mesa formations is discussed in the following sections. The metal contacts are defined using JEOL-6000FS/E E-beam Lithography System and deposited by electron beam evaporation. After the active device is fabricated, the sample is planarized and passivated with bencozyclobutane (BCB) followed by the etch-back process using Freon-based RIE to expose the post metal before the coplanar-waveguide metallization.

WET-ETCHING PROCESS ISSUES AND RESULTS

A) EMITTER-BASE WET ETCHING

The DHBT EB mesa under the emitter metal is formed using wet-etching with the emitter metal as the etching mask. The lateral undercut of EB mesa is critical as it needs to be minimized for lower base epitaxial resistance while still preventing the emitter from shorting to self-aligned base contact. Sulfuric-acid-based and hydrochloric-acid-based selective wet-etching is performed to treat the emitter cap and emitter layers respectively. Enhanced controllability of EB mesa etching is achieved by cooling the hydrochloric-acid-based etchants down to 0℃. A lower temperature can effectively reduce the etching rate and allow fine-tuning of wet-etching duration. The subsequent self-aligned base metal is precisely formed with nanometer overlay accuracy using E-beam lithography. Fig.1 (a) shows the device after EB mesa formation. The undercut gap is less than 0.1 μm. Fig.1(b) shows the device after the self-aligned base metallization.

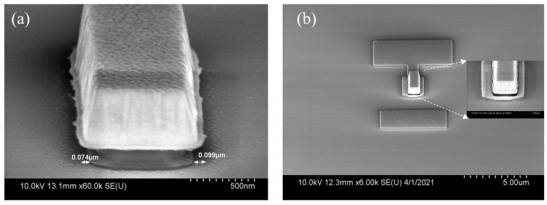

Fig. 1. SEM images of (a) fabricated device after emitter mesa wet -etching showing lateral undercut < 0.1μm, and (b) device after self-aligned base metal deposition

B) BASE-COLLECTOR HYBRID ETCHING

The preservation of BC mesa etch is crucial for the transistor to achieve high-voltage operation. A well-preserved BC area also reduces base resistance (R_B) at the expense of higher BC capacitance (C_{BC}). Therefore, lateral scaling by etching determines the trade-off between f_{MAX} and f_T. Traditionally, the BC mesa is formed by a wet-etching treatment which produces huge undercut and causes low yield. In this work, ICP-RIE dry-etching is developed as the alternative to maximally remain the BC mesa for power application as well as improve the process controllability. The InP collector can be etched by either chlorine-containing gases or CH_4/H_2 gas mixtures. The Cl_2-based dry-etching can result in surface roughness issues and nonvertical sidewalls due to the temperature-dependent nonvolatility of InClx etch products. On the other hand, the CH_4/H_2–based dry etching shows higher operationality at room temperature and produces smoothly etched surfaces and vertically etched profiles [5, 6], which is preferable for the DHBT device to maintain high breakdown voltages.

With the CH_4/H_2 plasma selected, the establishment of a reliable dry-etching process begins by tweaking ICP/RIE power/gas ratios and etching time in Oxford Plasmalab 100 ICP RIE etcher. The ratios are finely adjusted to ensure etching stability and surface quality without polymer byproducts. Once the ratios are fixed, the accurate ICP-RIE etching time is identified through a control experiment using three testing samples with the same epitaxial layer structures. As sample A (without any preprocessing) serves as a control subject, sample B and sample C have gone through wet-etching treatment to remove either only the emitter layer or both emitter and base layers before the ICP-RIE experiement. All three samples are etched under the pre-determined ICP/RIE power and gas ratios at 10 mTorr. The corresponding etching profiles are detected by the endpoint detector and plotted in Fig. 2. The exact etching time to arrive at a specific layer can be identified by aligning the peaks and valleys of the three curves. With the precise control of ratios and time, the BC mesa dry-etching on the formal device proceeds with SiNx as a hard mask. The surface smoothness

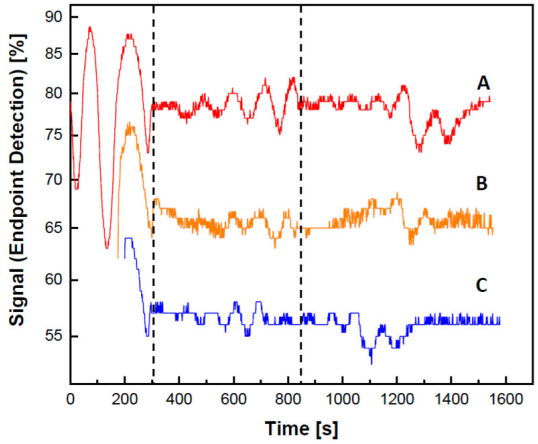

Fig. 2. The etching profiles detected by the endpoint detector of three samples: sample A (red, no pre-processing), sample B (orange, pre-processing to remove emitter) and sample C (blue, pre-processing to remove both emitter and base).

can be further improved with a subsequent dilute wet-etching to ensure the full removal of etching residuals.

As opposed to the traditional wet-etching which undercuts excessively into the collector, the hybrid-etching technique preserves the BC mesa for the device to retain a high breakdown voltage and also significantly increase the yield to more than 90%. The yield of the process is evaluated by both SEM checking after mesa formation and DC measurement after the device is finalized. Among the 97 devices tested in total from a 1.2-cm sample, 93 devices function properly. For comparison, another sample fabricated with the traditional wet-etching process was also evaluated in a similar method. The yield of the device fabricated by the hybrid etching turns out to be two times more than what the wet-etching mesa process can achieve. Fig 3 (a) shows the device fabricated through traditional wet-etching, and Fig. 3 (b) shows the device processed by the developed hybrid etching.

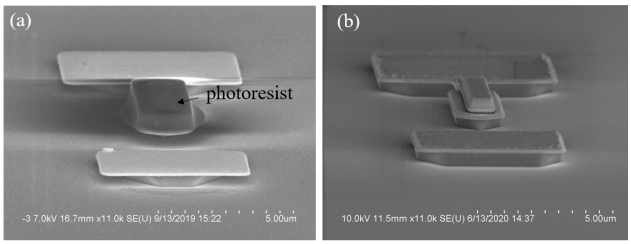

Fig. 3. (a) Fabricated device after the traditional BC mesa wet-etching. (b) Fabricated device after the BC mesa hybrid etching.

C) ISOLATION HYBRID ETCHING

Aside from the preceding EB and BC mesa formation, an etching process is required to isolate the active device from the base post to reduce parasitics. The isolation etching needs to clear all the conductive layers below the airbridge as depicted in Fig. 4 (a). Fig. 4 (a) illustrates the epitaxial layer structure of DHBT without isolation. Fig. 4 (b) also shows an SEM image of a fabricated device before isolation. The complex epitaxial layers increase the process difficulty of undercutting the narrow interconnect. When only wet-etching is involved, the fabricated sample has suffered from detrimental non-uniformity as the exposed metal catalyzes faster acid etching. The low controllability of the wet-etching rate could cause metal collapse due to the excessive lateral undercut [7].

To resolve this issue and make the isolation process more feasible and controllable, ICP-RIE dry etching with methane-based plasma is exploited to vertically etch down the extrinsic region. The sufficient vertical dry-etching isolates the device from one another as well as offers higher flexibility to laterally remove the InGaAs layer sandwiched between InP layers in the subsequent wet-etching. The selective wet-etching treatments are taken with alternations to partially etch InP for easier removal of InGaAs, which then allows further clear of InP. With well-controlled dry-etching followed by systematic wet-etching, isolation is achieved with improved uniformity. Figure 5 shows a DHBT device after isolation hybrid etching with the intrinsic region protected. It can be clearly seen that the external region is vertically etched down to the semi-insulating substrate and the airbridge at the interconnect is successfully formed via lateral undercut. This complete isolation removes extrinsic capacitances and eliminates the leakage path, enabling higher bandwidth performance for DHBT[8, 9].

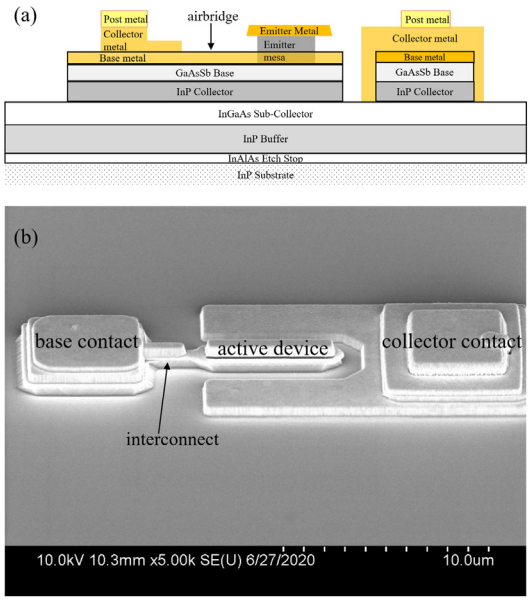

Fig. 4. (a) Side-view illustration with metal and epitaxy structures. (b) Tilted side-view SEM image of the fabricated device before isolation, with base contact, active HBT and collector contact indicated.

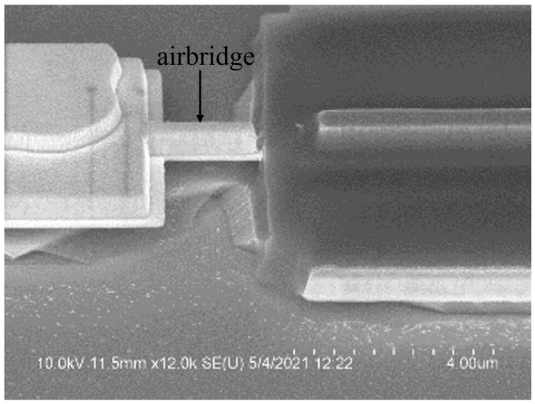

Fig. 5. Airbridge side view of the device after complete isolation with active region covered by photoresist.

The importance of isolation can be demonstrated by comparing the RF performance of devices with and without this process, Fig. 6 depicts the measured current gain ($|H_{21}|^2$) and unilateral power gain (U) of two devices under V_{CE} = 1.5 V: with isolation (solid-line) and without isolation (dashed-line). Both of the devices have the same emitter area (A_E =2.4 μm^2). A single-pole transfer function is then used to extrapolate the f_T/f_{Max} of the device: 135/245 GHz and 3/25 GHz, respectively. This comparison shows that the lack of isolation would result into severe performance degradation. Therefore, a well-tuned isolation process is vitally important and indispensable for the DHBT device to achieve high f_T/f_{Max}.

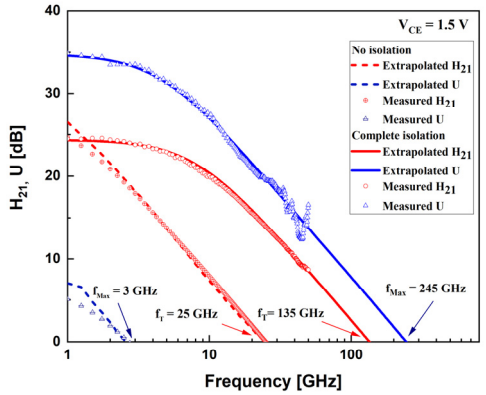

Fig. 6. Current gain H_{21} and unilateral gain U of a device without isolation and a device with complete isolation when both biased at V_{CE} =1.5 V.

The developed hybrid etching process also preserves BC mesa which helps maintain higher breakdown voltages. As shown in Fig. 7, a 0.4×8 μm^2 DHBT with a 450-nm collector layer demonstrates common-emitter breakdown voltage BV_{CEO} greater than 11.5V and collector-base open-emitter breakdown voltage BV_{CBO} greater than 13.5V at J_C = 1 kA/cm^2.

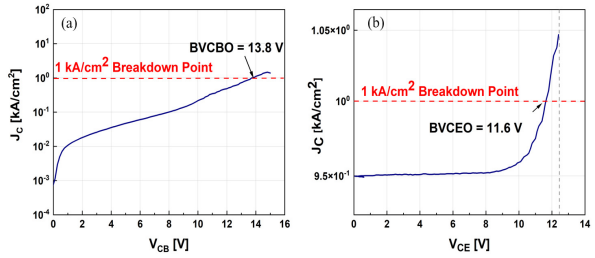

Fig. 7. Measured I-V characteristics for a 0.4×8 μm^2 DHBT with breakdown voltages (a) BV_{CBO} = 13.8 V and (b) BV_{CEO} = 11.6 V when J_C = 1 kA/cm^2

CONCLUSION

In this work, enhancement of process uniformity and controllability for submicron InP DHBT is demonstrated with a systematic hybrid etching method. The adoption of precisely-tuned dry-etching minimizes BC mesa undercut and helps achieve complete isolation, dramatically increasing yield beyond 90% over the whole sample. As the result, a 0.4 × 6 μm^2 the fabricated device exhibits excellent f_T/f_{Max} = 135/245 GHz. A 0.4×8 μm^2 device demonstrates breakdown voltages (BV_{CEO} and BV_{CBO}) greater than 11V. With improved manufacturability, the RF and voltage performances indicate a promising potential of the sub-micron GaAsSb/InP DHBT in millimeter-wave power amplification.

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