Fabrication of High-Performance Compound Semiconductor RF Circuits Using Heterogeneously-Integrated Transistor Chiplets in Interposers

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Abstract

Heterogeneous integration technologies can greatly reduce the cost and fabrication cycle time of RF integrated circuits that rely on compound semiconductor devices. We present a technology called MECAMIC (Metal-Embedded Chiplet Assembly for Microwave Integrated Circuit), which features highly-scaled III-V transistor chiplets (e.g., GaN devices) embedded in the volume of integrated passive wafers (e.g., interposers) using a metal bonding matrix. A process design kit was developed to support the layout and simulation of the RF ICs, and circuits up to W-band have been demonstrated.

INTRODUCTION

Leading edge compound semiconductor device technologies are typically developed in low-volume high-mix research laboratories and foundries using state-of-the-art processes on small-diameter substrates. Scaling up to demonstrate high-performance circuits poses significant engineering challenges, which generally translates to long fabrication cycle time and low yield. Additionally, the surface area utilized by transistors in monolithic microwave integrated circuit (MMIC) designs is very small compared to the circuit area (between 1 to 10%) – the remaining area being used for inter-stage matching networks, transmission lines, decoupling capacitors, and other passive elements. None of these passive elements are making effective use of the small-diameter exquisite substrates and epi materials grown in III-V semiconductor wafers for RF applications.

As a result of these factors, heterogeneous integration technologies can provide a disruptive manufacturing model for high-performance III-V RF ICs by decoupling transistor design, development, and fabrication, from the circuit manufacturing (Fig. 1).

HRL has developed a technology called MECAMIC, which stands for Metal Embedded Chiplet Assembly for Microwave Integrated Circuits [1, 2]. Based on the wafer-level multi-chip module integration platform named MECA (Metal Embedded Chip Assembly) [3], MECAMIC enables highly-scaled heterogeneous integration of III-V transistors chiplets with Integrated Passive Device (IPD) wafers (or interposers).

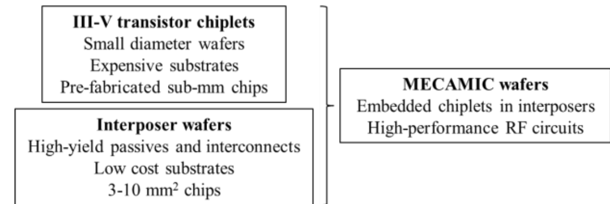

Fig. 1. Hybrid manufacturing techniques of III-V transistor chiplets such as the MECAMIC technology enables high-performance RF ICs with rapid fabrication capabilities.

Using heterogeneous integration techniques, high-performance RF ICs can be designed and fabricated using the best transistor technology for the function and combined with multiple device technologies on the same wafer. Further, hybrid manufacturing approaches such as MECAMIC reduce cycle time by pre-fabricating standards for the transistor chiplets and making them available off the shelf. Last but not least, the scaling of this technology result in comparable performance with monolithic circuits.

In this paper, we present an overview of the MECAMIC process flow, followed by key elements of the process design kit (PDK) in Microwave Office AWR, and some circuit demonstrators.

MECAMIC FABRICATION PROCESS

The MECAMIC heterogeneous integration process is shown in Figure 2 [1]. First, the interposer wafers are designed and fabricated using 2 metal layers, TaN resistors (50Ω/□) and SiN capacitors (300 pF/mm2) and a layer of BCB dielectric (εr = 2.65). The substrate (SiC or Si) is subsequently thinned down to target thickness (e.g., 50 µm). Backside vias and chiplet cavities are etched in parallel.

Third, the transistor chiplets are placed face down on a temporary substrate. The SiC (or Si) thinned interposer wafers with pre-fabricated interconnects and passives are also temporarily bonded on the temporary substrate. A backside metallization process is used to mechanically embed the chiplets into the interposer wafer and to provide DC and RF ground. The source of the transistor chiplets can be grounded either through backside chiplet vias or by interconnecting the source pad to the grounded metallic ring surrounding the

chiplets. Additionally, the metallized backside encapsulation provides thermal management due to the material's high thermal conductivity (> 300 W/m·K). The MECAMIC wafers are then demounted from the temporary substrate, flipped, and processed with wafer-level 5-μm-thick gold plated interconnects using an air bridge process (M3). The metallic interconnects provide electrical connectivity between the transistor chiplets and the circuitry.

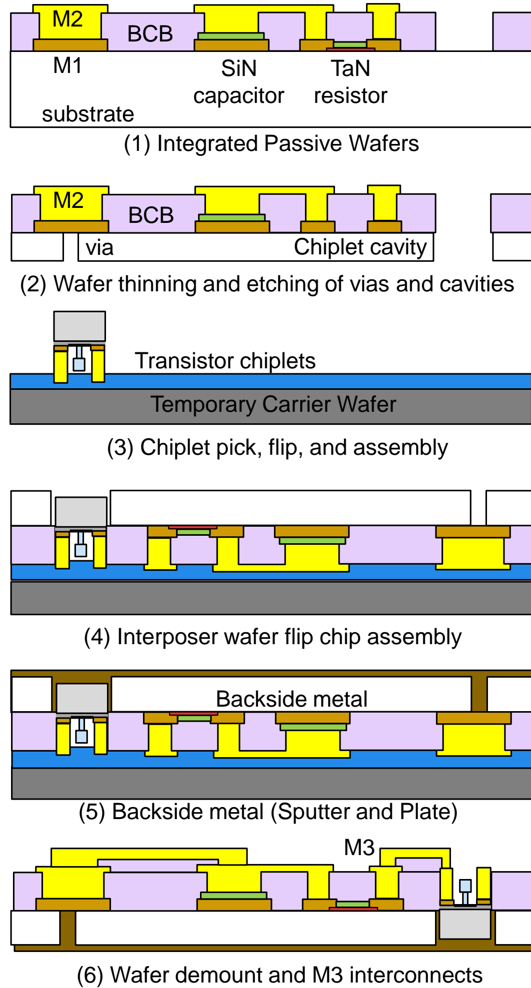

Fig. 2. MECAMIC Process Flow

The development of standardized 40 nm AlGaN/GaN HEMT chiplets to rapidly fabricate GaN circuits up to W-band are presented (Fig. 3). Such chiplets are realized by combining advances in e-beam gate processes and massively-parallel singulation techniques.

Specifically, we demonstrated a 5x decrease in e-beam cycle time through process optimization. GaN chiplets with fT > 110 GHz and Imax > 1.3 A/mm were fabricated in yielded quantities exceeding 50,000 per 4" wafer. The chiplets were singulated by plasma dicing (i.e., SiC etching) followed by a carrier-to-tape transfer approach. The chiplet design is based on HRL's scalable T3 GaN device model included in the T3 GaN PDK. Standardized off-the-shelf chiplets consist of device sizes ranging from 4x37.5 μm to 8x75 μm, which corresponds to gate peripheries ranging from 150 to 600 μm and can generally cover circuit frequency band from Ka- to W-band.

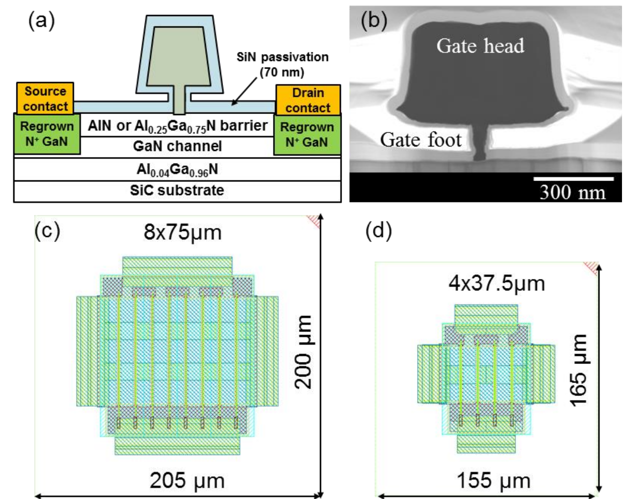

Fig. 3. T3 GaN chiplets: (a-b) 40 nm gate length T-gate structures on highly-scaled AlGaN/GaN epitaxial layer; (c-d) HEMT standardized chiplets.

Fig. 4 shows a large-area microscope image of a MECAMIC interposer wafer (Fig. 2(2)). The inset highlights the integrated passives, metal routing (M2), and chiplet cavities. The chiplet dimensional control is on the order of 2 μm, which enables accurate chiplet registration in the passive network. This process is currently being demonstrated on 3-inch-diameter high-resistivity silicon wafers (or SiC wafers), but can be scaled to large diameter wafers.

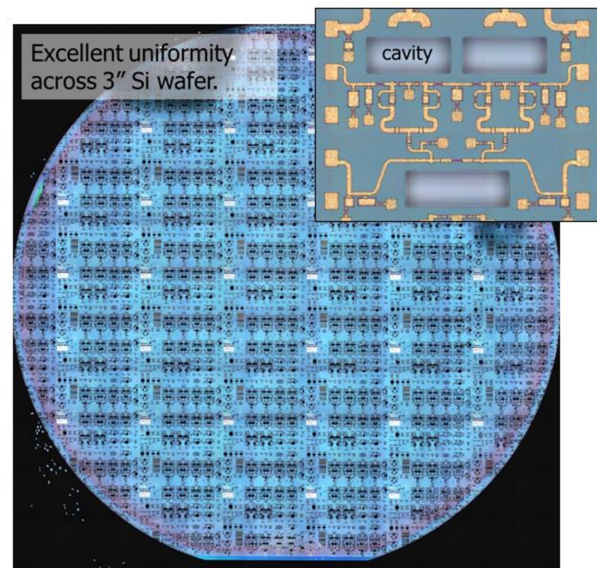

Fig. 4. MECAMIC integrated passive wafers before assembly.

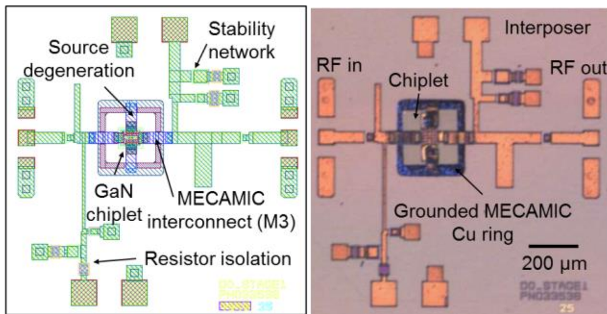

Fig. 5. MECAMIC single-stage 77 GHz circuit design and fabrication.

An example of a MECAMIC circuit with embedded GaN chiplets and MECAMIC interconnects (M3) is shown in Fig. 5. The chiplets are assembled using traditional pick and place tools. After the backside metal embedding process, the registration of the chiplet within the wafer is better than 5 µm, and the topography is comparable to the metal thickness, which is also on the order of 5 µm.

Using pre-fabricated transistor chiplets, the fabrication cycle time of GaN RF ICs was decreased by 5X when comparing the monolithic process to the heterogeneous integration approach.

Process Design Kit (PDK)

A MECAMIC PDK was developed in Cadence AWR Microwave Office (MWO) to provide a design flow for working with multi-technology integration. The MECAMIC PDK is equipped with a palette of tools to help designers construct a MECAMIC design with a standard circuit design workflow. As with other traditional circuit design PDKs, the MECAMIC PDK has components that are pre-defined and have passed Design Rule Checks (DRCs). The design rules are critical for the success of the design-fabrication-testing workflow.

The MECAMIC PDK allows designers to use device technology PDKs available from AWR to create chiplet assemblies. These assemblies are a hierarchical integration of the device technology PDK and MECAMIC PDK. Several chiplet assemblies have been constructed in digital version and physically (off-the-shelf chiplets), allowing designers to drag and drop a chiplet from the element pallet directly onto the schematic as shown in Fig. 6. In this example, the chiplet has grounded source vias. In the layout, the chiplet is surrounded by the MECAMIC cavity/metal ring. New chiplets can also be created using the device technology PDK and be compliant with the MECAMIC chiplet design rules.

The transistor chiplets are connected to other chiplets (from the same or from a different device technology) using the interposer with MECA interconnects, which are parameterized cells and available in the MECAMIC PDK palette as shown in Fig. 7. Optimization can be performed using AWR Analyst for more accurate Electro-Magnetic (EM) simulations.

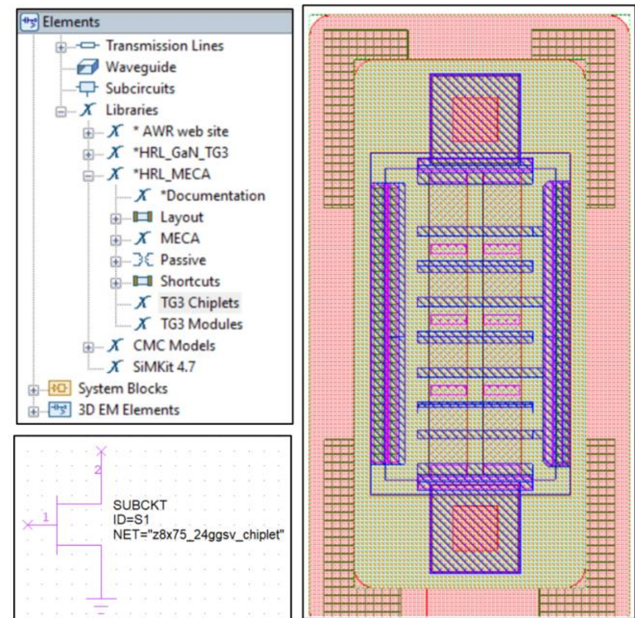

Fig. 6. Cadence AWR MWO MECAMIC transistor chiplet drag and drop from PDK palette to schematic with associated layout.

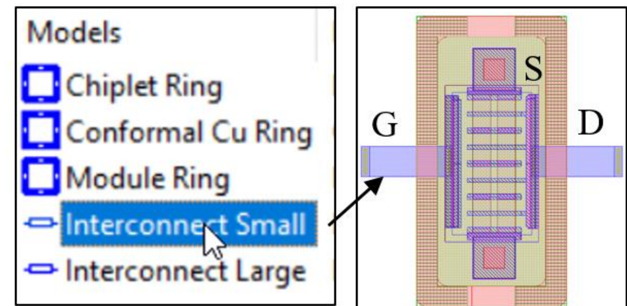

Fig. 7. Cadence AWR MWO MECAMIC transistor chiplet with added MECAMIC interconnects drag and drop from PDK palette to schematic with associated layout.

Using the MECAMIC PDK chiplet assembly library, circuit designers can use a traditional MMIC design workflow to construct and simulate heterogeneously-integrated circuits. Designers can build a schematic of their circuit with an associated layout and perform electrical simulations as shown in Figure 8. After initial electrical simulations, a designer can perform EM simulations using the MWO EM extract block to create EM structures from the elements in the schematic. The MECAMIC PDK provides a workflow that allows the extract blocks to extend to low levels in the hierarchy to accurately construct the needed EM structures. These EM structures are simulated, and the results are used to update the entire circuit performance.

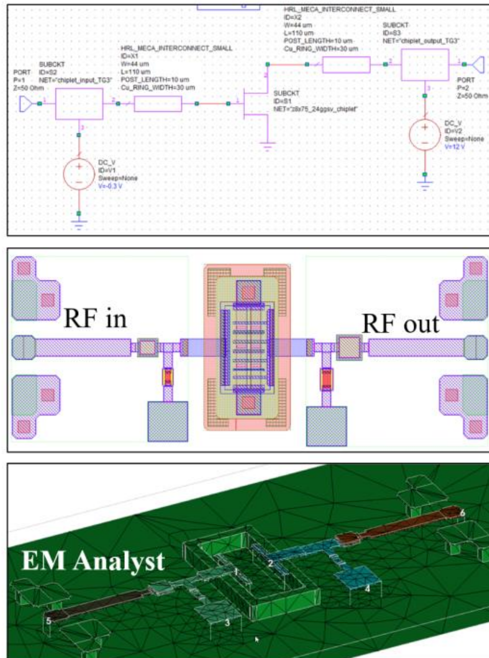

Fig. 8. Cadence AWR MWO MECAMIC transistor chiplet with added MECAMIC interconnects drag and drop from PDK palette to schematic with associated layout.

MECAMIC CIRCUIT DEMONSTRATION

S-parameter simulations and measurements of the single-stage circuit shown in Fig.5 were performed. The simulation used Microwave Office. Although higher gain was measured (6.5 dB vs. 5.5 dB for simulation), the measurements showed reasonable agreement with simulated values across the band of operation (70-80 GHz). This also compares well with the characteristics of a similar design in a T3 GaN MMIC process.

Further, a three-stage low-noise amplifier circuit was designed, simulated, fabricated and tested, and demonstrated a 4 dB noise figure at 77 GHz with a 16 dB gain. A microscope photograph, and S-parameter simluation and data are shown in Fig. 9 and Fig. 10, respectivley. The yield exceeded 66% across the wafer.

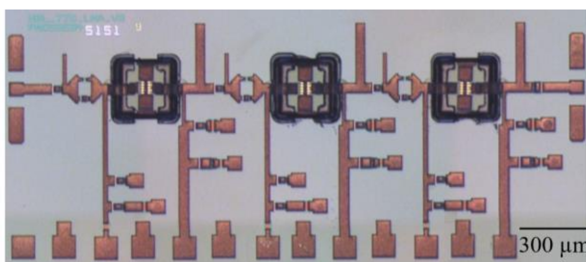

Fig. 9. Simulated and measured S-parameters of a heterogeneously-integrated single-stage RF MECAMIC circuit operating at W-band.

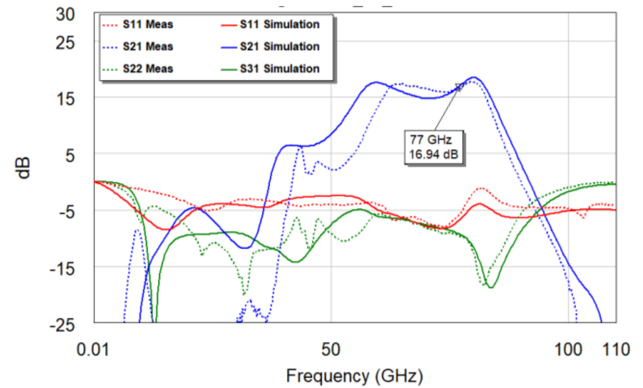

Fig. 10. Small-signal data of the 3-stage MECAMIC W-band LNA is in good agreement with simulated performance.

CONCLUSIONS

Hybrid manufacturing techniques such as MECAMIC enable rapid prototyping and manufacturing of high-performance III-V integrated circuits for mm-wave applications.

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