Wafer Breakage Reduction in Cu Bump Processing of GaAs Technologies

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Abstract

Efforts to reduce wafer breakage events during Cu bump manufacturing of GaAs technologies were discussed in this paper. Wafer backside residue and scratches formed during upstream processes were found to cause stress breaks at the Cu plating step. A correlation of wafer edge chipping at the lamination process and downstream finish processes was discovered. The fishbone diagram was used to investigate frequent wafer stress breaks at Cu field metal etch process. As a result, the overall wafer breakage rate was reduced by more than 50% in Cu bump processing.

INTRODUCTION

GaAs devices have been widely used in RF applications and the GaAs manufacturing wafer yield has been significantly improved over the last two decades [1-4]. One of the challenges with GaAs fabrication is high wafer breakage rate due to its brittleness. Many research studies have shown that the GaAs wafer breakage rate was reduced from up to 25% during the initial development to less than 0.5% in high volume manufacturing through equipment modification and process improvement [1-4]. With the increasing requirement of cost effectiveness, the goal of wafer yield of GaAs manufacturing has been continuously raised. At Qorvo, wafer breakage is the second largest contributor to wafer yield loss of GaAs technologies.

To understand the causes of high wafer breakage rate, the broken wafer scrap data was analyzed by process steps. Figure 1 shows the GaAs wafer breakage events at different manufacturing process steps. The data indicated baseline level wafer breakage across front-end-of-line processes, but wafer breakage occurred more often during Cu bump and fab finish process steps. Since wafers are more valuable at the backend of the process, this study is focused on reducing wafer breakage rate during Cu bump processing.

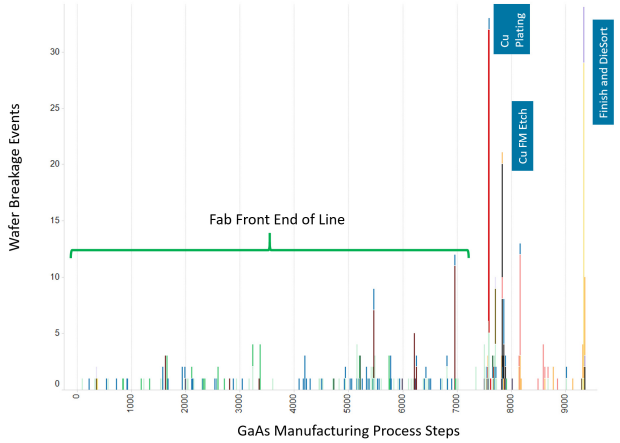

Figure 1. Wafer breakage scraps at different process steps during GaAs manufacturing

RESULTS AND DISCUSSION

Stress Breaks at Cu Bump Plating Step

As shown in Figure 1, the first high wafer breakage rate step in Cu bump fabrication is the Cu bump plating step. Wafers were normally found broken during handling into/out from the plating equipment. The frequent wafer breakage events have not only caused wafer yield issues, but also reduced the equipment availability, therefore impacting manufacturing cycle time. Adjusting tool parameters including robot handling and vacuum levels were attempted and reduced the wafer breakage rate.

However, frequent wafer breakage was still observed.

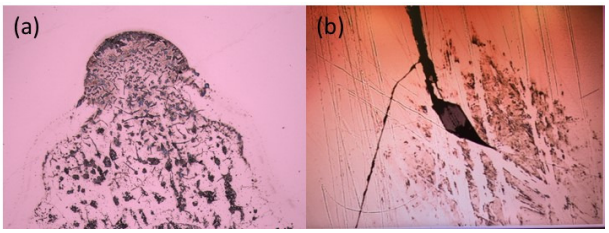

Figure 2. (a) Residues present on the backside of the wafer incoming to Cu bump plating step (b) Microcrack observed after removing the residue

Further investigation of the broken wafers indicated residues on the backside of the wafers makes the wafers more susceptible to breakage during Cu bump plating handling. The residue was normally found at the center of the wafer and could cause vacuum issues. The wafers may drop during handling or become misaligned inside of the tool. For the wafers that cannot be picked up by the tool and are still intact, manual scraping is required to remove the residue. However, microcracks will be introduced during manual residue removal and will lead to stress breaks later as shown in Figure 2(b).

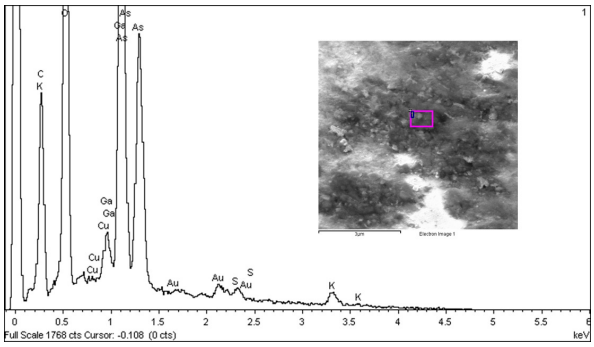

Figure 3. EDS analysis of wafer backside residue incoming to Cu bump plating process

EDS analysis of the wafer backside residue revealed the presence of K and Au elements. This indicated the residue was formed during an upstream sink process. Inline inspection was performed and confirmed the root cause of residue formation.

A combination of efforts to reduce wafer backside residue at upstream process steps and the subsequent residue removal process on the incoming wafers have reduced the wafer breakage rate at Cu bump plating step by > 70%.

Investigation of Wafer Stress Breakage at Cu Field Metal Etch Process

The second highest wafer breakage step during Cu bump fabrication is the field metal etch process. The broken wafers were found to have a specific stress break pattern. When the stress break was found, the broken wafers were always sitting in the cassette broken into two pieces with the breakage plane facing the top of the cassette. The wafers were not typically aligned at the field metal etch process, but the broken wafers were always the ones with 8 o'clock or 2 o'clock at the top of the cassette, as shown in Figure 4.

Figure 4. Pictures of broken wafers found at field metal etch process. Signature of 8 to 2 o'clock stress break with breaking plane always facing the top of the cassette.

This unique breakage pattern indicated two potential failure modes. One hypothesis is that there was excessive force applied to the wafer edge that caused stress break when the force was applied to 8 or 2 o'clock. This failure mode pointed to the slide transfer used at Cu field metal etch process. Multiple wafer transfers between PEEK and teflon cassettess are required during preclean and field metal etch processes. The wafer transfers are performed using a manual slide transfer. It was found that the handle of the slide transfer arm drifted down. If the handle was not lifted properly, there will be an angle between the pusher and wafers therefore cauing extra force

on the wafers. If the slide transfer was touching at the crystal plane of the GaAs wafers, the wafers were likely to break along the plane.

After replacing the slide transfer for Cu bump processing and refreshing slide transfer training, the wafer breakage rate was reduced at Cu field metal etch process. However, frequent breakage events still remained.

The other failure mode that could explain the 8 or 2 o'clock breakage was damage from a previous step that only broke after the slide transfer motion. The backend engineering team did a Fishbone analysis to identify possible steps/processes that could cause micro damage on the wafer, as shown in Figure 5.

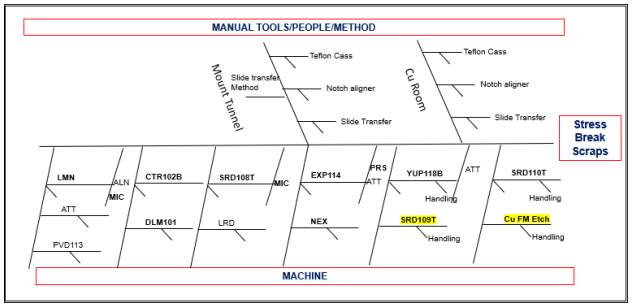

Figure 5. Fishbone diagram to troubleshoot root cause of stress break at field metal etch process.

During an extensive equipment handling check, it was found that a tool cover was slightly touching the wafer edge when the robot was moving the wafer into the tool as shown in Figure 6. The wafer did not break at this step and no obvious damage was observed, but if the wafer was rotated so that the 8 or 2 o'clock crystal plane touched the tool cover, the wafers were more likely to break during a later slide transfer process step. The tool cover was then modified to have more clearance during the wafer handling. With these combined improvements, the wafer breakage rate was significantly reduced at the field metal etch process.

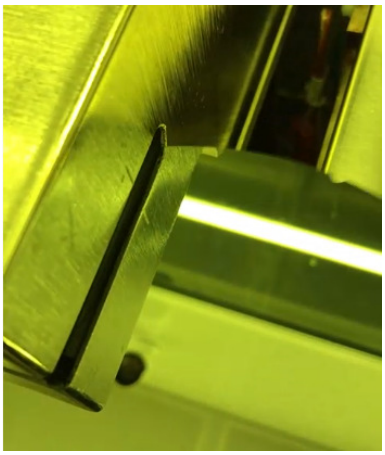

Figure 6. A tool cover was found touching the wafer edge when the wafer is moving into the tool.

Correlation of Edge Chipping and Wafer Stress Breaks at Subsequent Finish Processes

After Cu bump processing, wafers are sorted and then go to the finish process. It was found that some wafers were broken during the sort or finish processes without apparent root causes. The equipment in sort and finish areas were checked but no cause of the breakage was identified.

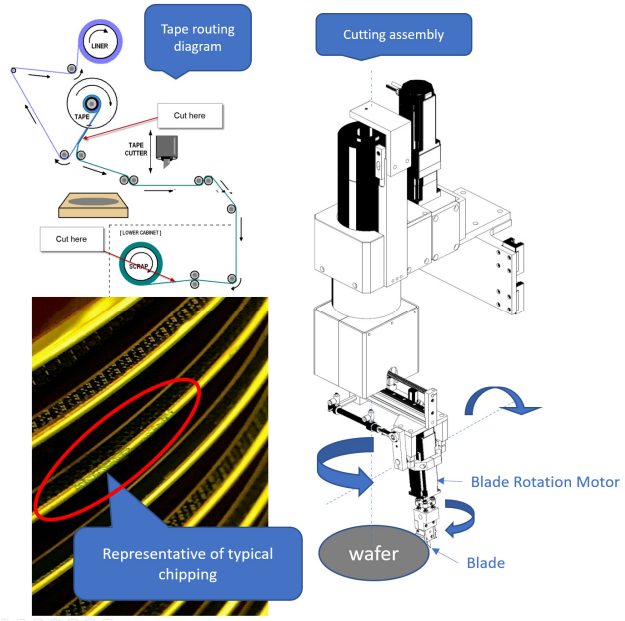

Figure 7. Wafer edge chipping formed during lamination cutting step. Equipment schematics is from Microcontrol Electronic.

During an investigation of multiple lots having wafer breaks, it was found that the broken wafers were from the same parent lot in the upstream process. A closer look at the broken wafers revealed commonality of wafer edge defects that contribute to the origination of the wafer breakage. The wafer edge was covered with metals, so the defects were hard to detect. Inline inspection was implemented at upstream processes to identify the source of wafer edge defects.

Upstream inline inspection showed that intermittent wafer edge chipping was observed after the lamination process, from particular lamination equipment. Minor edge chipping/scraping was found after the cutting step. The cutting blade also showed abnormal wear prior to a scheduled PM, validating the failure mode.

Tool matching work including cutting angle adjustment and PID setting optimization to reduce vibration of the cutting process was performed reducing wafer edge chipping at this step and wafer breakage in the sort and finish areas.

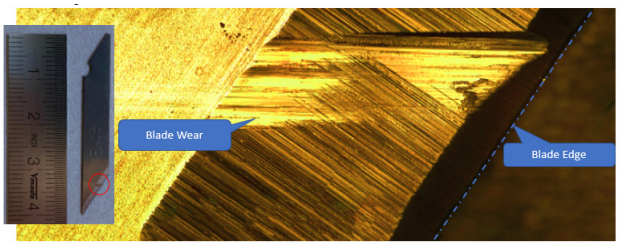

Figure 8. Wearing of the cutting blade indicated vibration causing wafer edge chipping.

CONCLUSION

In this paper, we discussed three wafer breakage reduction improvement projects in Cu bump process. With the implemented preventative actions, the wafer breakage rate of Cu bump fabrication has been reduced by more than 50%, and a new baseline with a lower wafer breakage rate was achieved, as shown in Figure 9.

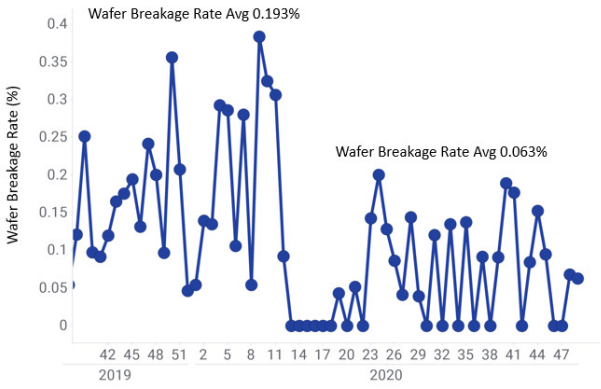

Figure 9. Wafer breakage rate of Cu bump process by work week. New low wafer breakage baseline was achieved after the improvement project.

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