**Self-Aligned Refractory Metal Gate Scaling in β-Ga2O3 MOSFETs**

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**Abstract**

**This work characterizes the effects of gate-length (LG) scaling in a self-aligned gate (SAG) β-Ga2O3 MOSFET process. Additional performance gains are expected by extending the SAG process from large LG to sub-micrometer dimensions. This data incorporates LG scaling down to 200 nm to improve device performance in Ga2O3 SAG MOSFETs using a stepper lithography process to define sub-micron gate lengths.**

INTRODUCTION

β-Ga2O3 (BGO) has recently sparked interest as a promising semiconductor for power applications. The bandgap of BGO is nearly 5 eV, and the estimated critical field strength (Ecrit) of ~8 MVcm-1 are both higher than GaN and SiC [1,2]. The high Ecrit of BGO can potentially realize advances in efficient power conversion and even RF devices. Recently, BGO was shown to possess the highest Ecrit ever measured in a lateral transistor [3] which has sparked BGO device research towards obtaining high Baliga Figure of Merit (BFOM) [4] and low dynamic switch power losses [5]. BGO RF power devices have also been reported in the low-GHz regime [6,7].

BGO has a relatively low mobility but higher Ecrit compared to GaN. The high Ecrit of BGO allows devices to be scaled laterally to a fraction of GaN based ones for a given breakdown voltage. Critical to laterally scaled BGO devices is developing a self-aligned gate (SAG) feature to remove parasitic access resistance between the source and gate electrodes (Rs) with the use of refractory metal gate-first processing [8]. Here, we report sub-micron LG scaling defined by stepper lithography and characterize the small-signal RF performance of SAG BGO devices.

DEVICE FABRICATION

A 65 nm Si-doped BGO channel layer was homoepitaxially grown on an Fe-doped (010) substrate by molecular beam epitaxy (MBE). Room temperature Hall measurements reveal a sheet charge density of 3.6x1012 cm-2 (estimated ND= 5.5x1017 cm-3 and Rsh= 23.7 kΩ/sq based on thickness) with 73.6 cm2/V·s carrier mobility. The first step in device fabrication was mesa isolation using a high-power BCl3 ICP/RIE (inductively coupled plasma/reactive ion etch) dry etch process. Aluminum oxide (Al2O3) was deposited using PEALD (plasma-enhanced atomic layer deposition) to serve as a gate dielectric as well as an implant cap. Source and drain implant regions were defined subtractively through W sputtering, followed by an SF6 RIE W dry etch process to achieve 1.75 µm source-drain distance. Si-implant was achieved using a shallow implant design with 35 and 85 keV implant energies targeting 1.0x1020 cm-3 Si ion concentration, followed by a rapid thermal anneal at 900oC for 120 sec in N2. Use of a refractive metal gate such as W is essential to a SAG process, as typical Au gates will not survive the high activation temperatures necessary for Si implantation. Ohmic contact was achieved using a

Ti/Al/Ni/Au evaporated metal stack, followed by a rapid thermal anneal at 470oC for 60 sec in N2. Gate scaling was accomplished using a stepper process to selectively remove W and achieving LG of 1.75 µm (no drift region), 0.75 µm, 0.5 µm and 0.2 µm using an additional SF6 RIE W dry etch. The region of removed W formed the drift region of the devices. Ti/Au interconnect metal was added via an evaporative deposition for device characterization. A cross-sectional schematic of the device is shown in Figure 1, as well as top-down SEM images showing sub-micron W gates in Figure 2.

Figure 2: Top-down SEM images of SAG Ga2O3 MOSFETs with A) LG = 1.75 µm, B) LG = 0.75 µm, C) LG = 0.50 µm, and D) LG = 0.20 µm

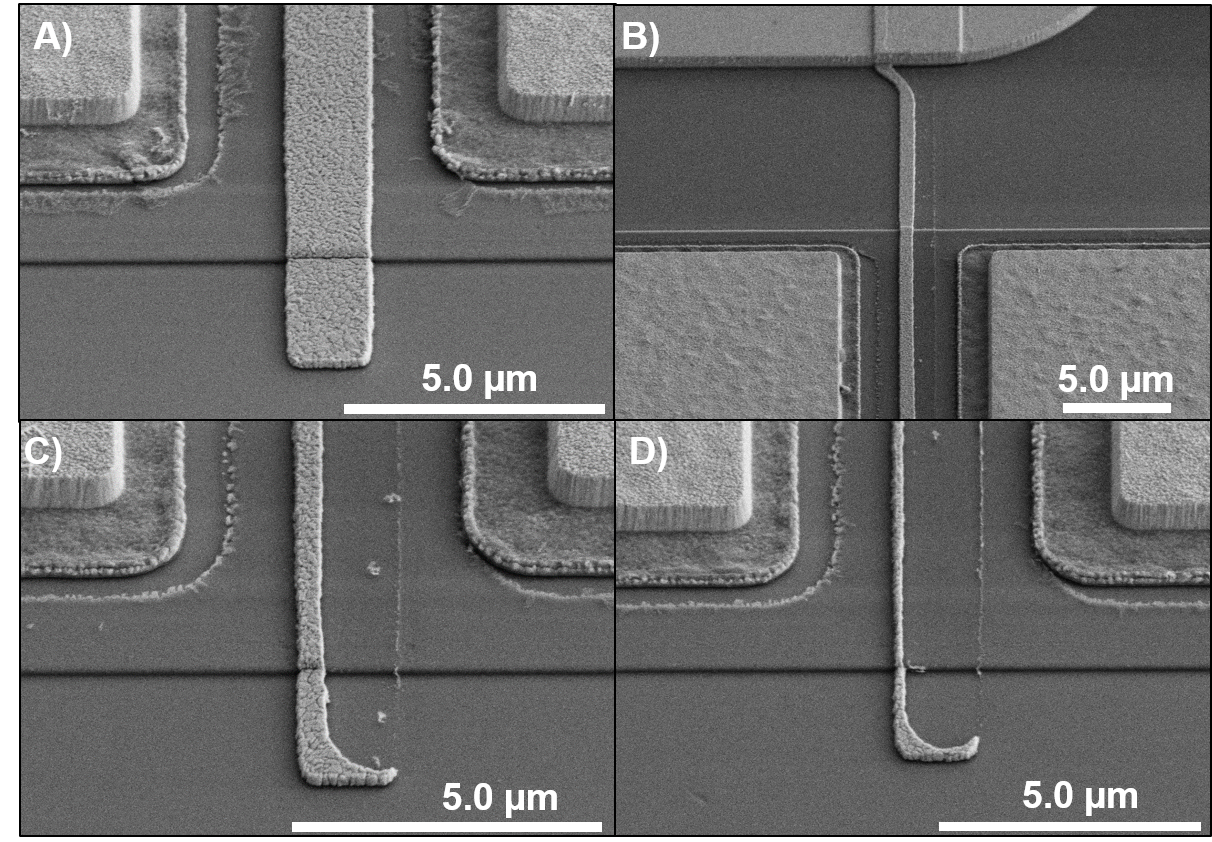
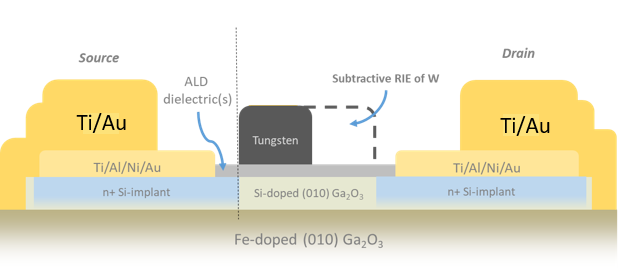


Figure 1: Self-Aligned BGO MOSFET schematic



DEVICECHARACTERIZATION

Standard DC I-V device characterization was performed and is shown in Figure 3(A-C). Figure 3A shows transconductance (gm) as a function of VGS at VDS = +15V for four gate lengths. A clear improvement in gm is demonstrated as LG decreases. The LG = 0.20 µm SAG MOSFET achieved a gm of 42 mS/mm, representing a record-high for β-Ga2O3 MOSFETs. Figure 3B shows Log transfer characteristics for four LG, showing loss of channel control as LG decreases. This can be improved by optimizing the Ga2O3 channel doping and thickness on future devices. Figure 3C shows the output family of curves for a scaled SAG MOSFET with LG = 0.75 µm from VGS = -6V to +6V and VDS = 0 to +14V, achieving a drain current density (IDS) of 315 mA/mm and on resistance (RON) of 32 Ω∙mm.

Small signal RF performance is shown in Figure 4(A-B) as a function of LG and VDS. The ft and fmax were recorded at gm,peak conditions over a VDS range of +5V to +14V and show increasing values with smaller LG as expected. The ft and fmax likely decrease from self-heating for the smaller LG devices that achieve higher current. A SAG MOSFET with LG=0.20 µm achieved ft and fmax of 7 and 11 GHz, respectively.

CONCLUSION

This study has reported the DC and RF performance as a function of LG using a self-aligned gate process for BGO MOSFETs. High current density (>300 mA/mm) and gm (>40 mS/mm) were obtained with laterally scaled SAG BGO MOSFETs despite higher channel sheet resistance. For short-gate SAG devices, good RF performance is reported while leaving substantial room for additional materials and device engineering improvements.

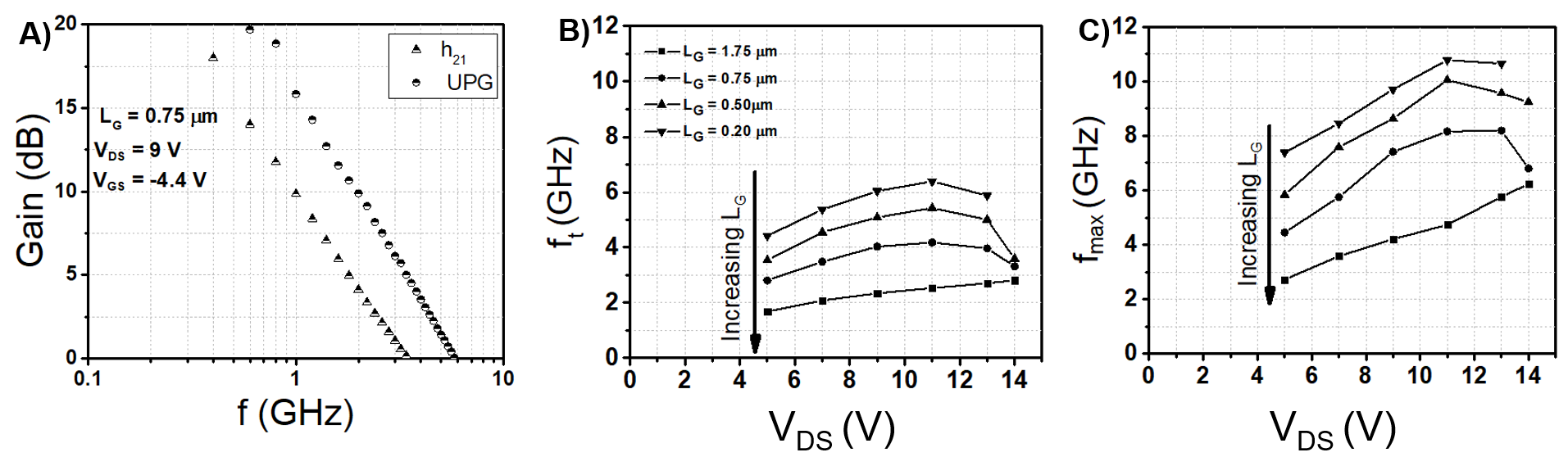
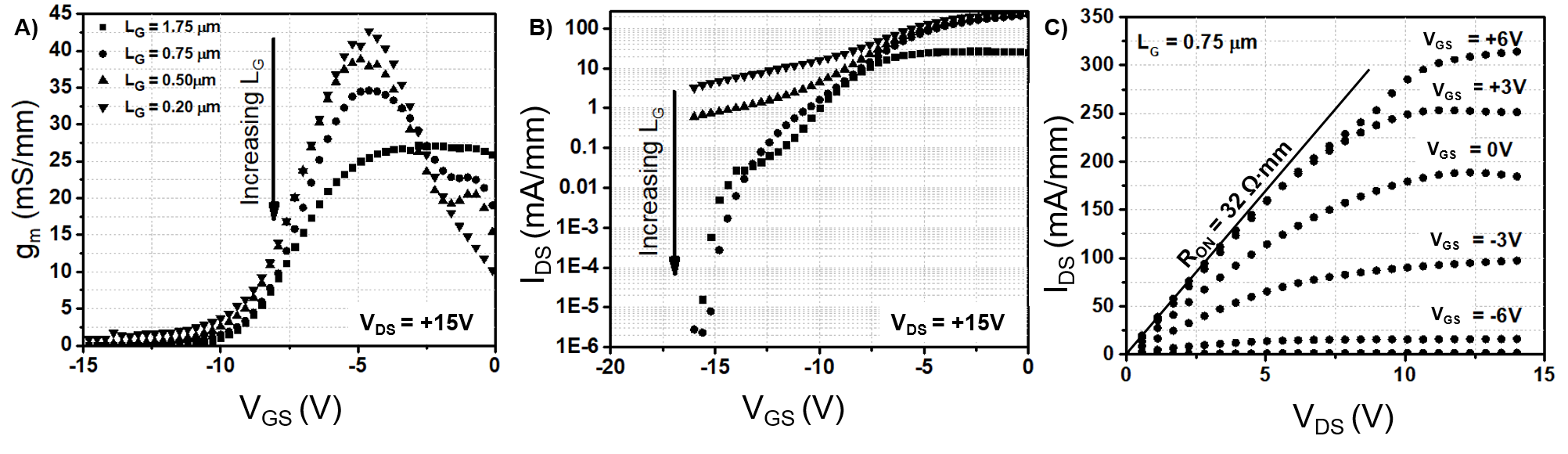


Figure 4: Small signal radio frequency performance at gm,peak as a function of LG and VDS.

Figure 3: A) Transconductance (gm) of SAG MOSFETs as a function of LG, B) Log transfer curve of SAG MOSFETs as a function of LG, and C) output family of curves for a SAG MOSFET with LG = 0.75 µm from VGS = -6V to +6V and VDS = 0 to +14V.



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ACRONYMS

SAG: self-aligned gate

MOSFET: metal-oxide-semiconductor field-effect transistor

BGO: β-Ga2O3

BFOM: Baliga’s Figure of Merit

RF: radio frequency

DC: direct current

MBE: molecular beam epitaxy

ICP: inductively coupled plasma

RIE: reactive ion etch

PEALD: plasma enhanced atomic layer deposition