Demonstration of High-quality GaN Epitaxy on 200 mm Engineered Substrates for Vertical Power Device Fabrication

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Abstract

Engineered substrates with a poly-AlN core, thermally matched to GaN, are promising to reconcile the use of high-yield GaN wafers with thick buffers on large scale substrates (≥ 200 mm). We demonstrate crack-free 5.4 µm-thick high quality GaN epitaxial layers grown on 200 mm substrates, with a good control of wafer bow and a PN-junction that reaches 440 V. A semi-vertical trench gate MOSFET device architecture has been used to demonstrate the excellent device performance in ON-state, reaching 1.2 kA/cm^2 and a low on-resistance of 5.7 mΩ·cm^2. A next generation epitaxial stack has been developed approaching 1.5×10^{16} cm^{-3} net doping concentration in the n-drift layer combined with a very good and uniform crystal quality, with the GaN <102> peak as low as 400 arcsec.

INTRODUCTION

Engineered substrates are promising to extend the voltage range beyond 650 V on large area substrates with thick GaN layers, while avoiding wafer breakage during device fabrication. Qromis Substrate Technology (QST®) has been a pioneer in this regard and commercially offers 200 mm engineered substrates with SEMI standard thickness. The QST® substrate consists of a polycrystalline ceramic core (poly-AlN), covered by several encapsulation layers, on top of which is a SiO_2 bonding layer and a single crystalline Si layer which serves as the nucleation layer for the MOCVD growth [1].

The fabrication of vertical GaN devices for high voltage applications has been reported on Si substrates up to 150 mm diameter [2]. To further scale up both the substrate size and GaN stack thickness on Si, is extremely challenging, due to the mismatch in thermal expansion coefficient and lattice constant between GaN and Si. With the use of these engineered substrates, the path towards vertical GaN device fabrication on large diameters is enabled, with scalability potential up to 300 mm. In literature, high quality GaN layers with vertical transistor and diode processing are demonstrated on GaN substrates [3-5], but only small area substrate sizes are available to date, with a very high substrate cost [6]. Compared to Si, the engineered substrate with poly-AlN core is a better candidate to grow high quality epitaxial GaN layers on large area substrates, since it is matched to GaN in the coefficient of thermal expansion. On engineered substrates, lateral pGaN gate HEMT devices have been demonstrated up to 650 V [7,8]. Scaling up this voltage will further increase the footprint of lateral HEMT devices, due to the need to increase gate to drain spacing, which will also affect the on-state performance of the fabricated devices. In vertical transistors, with the electric field vertically distributed over the GaN epitaxial stack the footprint of the device is independent of the target voltage, which makes this technology very suited for high voltage applications.

In this work, we demonstrate high quality GaN epitaxy on 200 mm engineered substrates for vertical device fabrication. In a first section, the GaN epitaxy is described showing also the voltage blocking capability of the PN-junction. Subsequently, the trench gate MOSFET device fabrication and ON-state performance of the device are reported.

GAN EPITAXY

Crack free 5.4 µm-thick GaN layers (Fig. 1.(a)) were grown by means of MOCVD using an AIX G5+ C Planetary Reactor® from AIXTRON, Germany. The 5×200 mm mini-batch reactor combined with cassette-to-cassette configuration allows for a high productivity while maintaining a very low number of particles for optimal yield. The stack consists of a 200 nm AlN nucleation layer, a strain-compensating buffer, a 1 µm uid GaN layer for defect reduction, a 750 nm n^+-GaN bottom contact, a 3 µm-thick n^- GaN drift layer, a 400 nm Mg-doped p-GaN layer and a 200 nm n^+-GaN top contact layer. Owing to the CTE-matched substrate and the choice of the epi stack, bow tuning below |50| µm can be achieved independent of the drift layer thickness. This is exemplarily shown in Fig. **1**.(b) for the stack depicted in Fig. **1**.(a). The good control of wafer bow enables device processing in a 200 mm process line, compatible with CMOS technology.

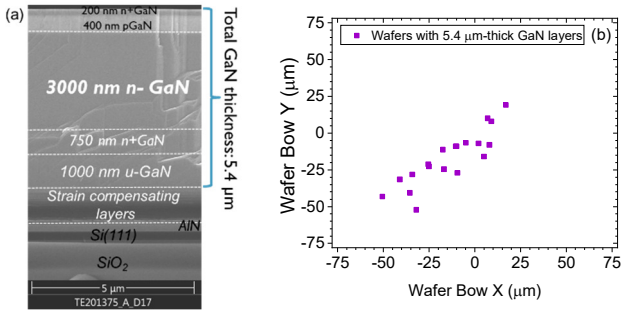

Fig. 1. (a) Cross-sectional SEM image and (b) wafer bow of 200 mm engineered substrates with 5.4 µm-thick GaN.

A SIMS analysis of the stack, depicted in Fig. 2, provides details on the chemical concentration of the individual layers. The n^+-GaN layers are doped with 5.5 $\times 10^{18}$ Si/cm^3. The pGaN layer has a 1.2×10^{19} Mg/cm^3 doping level, with a net p-doping of 2×10^{18} cm^{-3}. The drift layer has a Si doping level of 4×10^{16} cm^{-3} with a C background level of 1.5 $\times 10^{16}$ cm^{-3}.

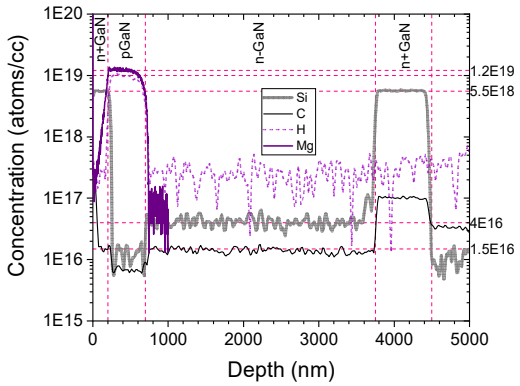

Fig. 2. SIMS analysis of doped GaN layers in grown GaN stack.

From Hall measurements an active n-type concentration of roughly 2.15×10^{16} cm^{-3} and a moderate drift layer mobility of around 473 cm²/ (V.s) was extracted (TABLE I). For the Hall measurements a test structure was grown with identical layers as the device stack up to the n^- drift layer, apart from the n^+-GaN buried layer, which was replaced by a uid-GaN layer, to make the Hall measurement possible.

TABLE I
CHARACTERISTICS n^- DRIFT LAYER, EXTRACTED FROM HALL MEASUREMENTS

n (cm^{-3})	ρ (Ω·cm)	µ (cm²/ (V.s))
2.15×10^{16}	0.62	473

For the epi stack as presented in Fig. **1** with an n^- drift layer containing a Si doping of 4×10^{16} Si/cm^3 and a good crystal quality, the PN-junction reaches ~440 V in reverse bias, as depicted in Fig. 3.

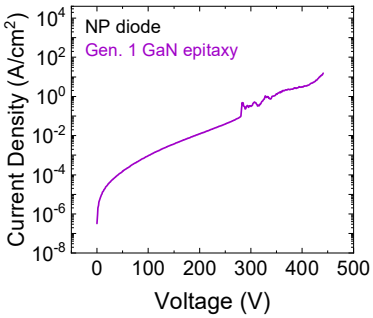

Fig. 3. Reverse J-V characteristic of PN-diode reaching 440 V, for the Gen.1 GaN layer stack.

Further work on GaN epitaxy has been executed, demonstrating a much-improved crystal quality and uniformity, illustrated by the XRD FWHM values in Fig. 4.(a), comparing 2 generations of GaN epitaxial layers, both with a 3 µm-thick drift layer, achieving a FWHM value as low as 400 arcsec for the GaN <102> peak, for the generation 2 stack. The amount of edge type dislocations in a stack is directly linked to crystal quality observed in the GaN<102> peak [9]. When comparing the generation 1 and generation 2 epitaxial stack, we were able to shrink the edge type dislocations by 30% in the center and 60% in both halfway and edge area of the wafer, resulting in an estimated amount of 4-5x10^8 cm^{-2}, as depicted in Fig. 4 (b). The improved crystal quality for the generation 2 epitaxy was obtained, by an adaptation of the Al containing strain compensating layers in the bottom of the stack. Furthermore, a decrease of Si doping level in the n^- drift layer to 2×10^{16} cm^{-3} was achieved, in combination with a very good suppression of the Carbon background doping, below 1×10^{16} cm^{-3}. These improvements are expected to further boost the voltage blocking capability of the PN diode in future work.

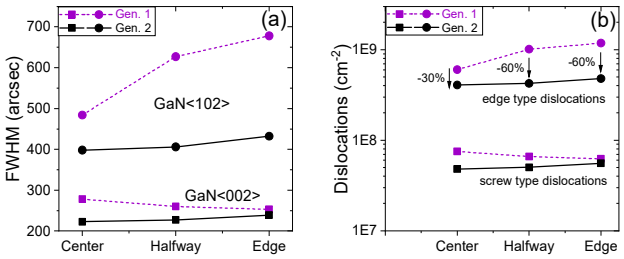

Fig. 4. (a) XRD FWHM of GaN <102> and GaN <002> peaks, (b) estimated number of dislocations for the Gen. 1 and 2 GaN layer stacks.

DEVICE FABRICATION

A semi-vertical trench gate MOSFET device was fabricated as test vehicle to demonstrate the device performance in ON-state. The electrons flow from the source to the inversion channel in p-GaN, through the n^- drift layer and are then collected via an n^+-GaN layer with a drain contact

at the frontside of the wafer. A schematic representation is given in Fig. 5.(a).

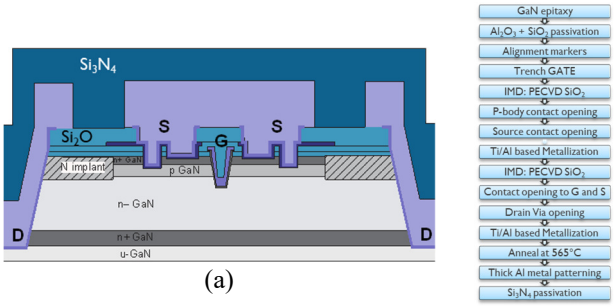

Fig. 5. (a) Pictorial representation and (b) process sequence order for trench gate MOSFET device.

First a thin Al_2O_3 and SiO_2 layer is deposited as surface passivation. The n^+-GaN and p-GaN top layers are isolated from the drain by an N implant. Next the trench gate is processed. The dry etch and wet etch steps have been optimized, resulting in a smooth gate trench sidewall [10], as depicted in Fig. 7.(a). The gate architecture is then further processed with a 2.5 nm Al_2O_3 and a 50 nm SiO_2 bilayer dielectric finishing with a TiN/Ti/Al based gate metal stack on top. The contacts to the source n^+-GaN, p-body and drain n^+-GaN layers are made using thin Ti/Al containing metal stacks. An anneal at 565°C is used for the Ohmic contact formation, after the drain metallization and patterning is processed, as shown in the process sequence in Fig. 5. The metallization is finished with a 4 µm-thick Al metal stack on top of the source and drain fingers and in the bond pad areas. By letting the thick power metal run over the gate, a minimum L_{SG} of 1.25 µm could be used in the design, which is beneficial for the ON-state performance of the devices. Finally, the device is finished with a 2 µm-thick Si_3N_4 passivation layer. In Fig. 6 a SEM image of the cross section of the active area of the processed device is depicted, with 2 source fingers and the trench gate architecture in the center. The buried n^+-GaN layer is connected from the frontside, which is depicted in a cross-sectional SEM image in Fig. 7.(b).

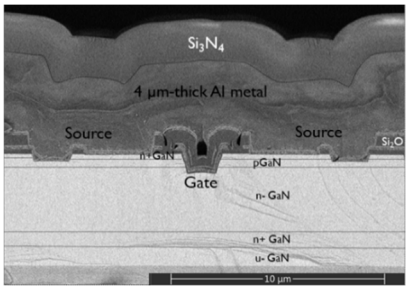

Fig. 6. Cross-sectional SEM image of the active area of the trench gate MOSFET device, depicting the gate and source regions.

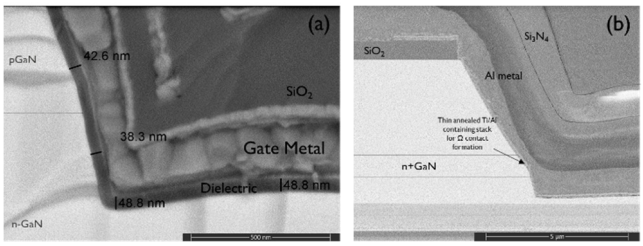

Fig. 7. Cross-sectional SEM image depicting (a) a zoom-in of the gate trench corner with a smooth GaN side wall, (b) a drain contact to the buried n^+-GaN layer, which is made from the frontside of the wafers.

ON-STATE PERFORMANCE

Multi-finger devices with a total effective gate width of 60 mm and an active area of 0.56 mm^2 were electrically characterized, and typical output and transfer characteristics are depicted in Fig. 8. The transistors exhibit a high drive current of 1.2 kA/cm^2 and a low on-resistance of 5.7 mΩ·cm^2 (normalized by the active area). The threshold voltage is 2 V.

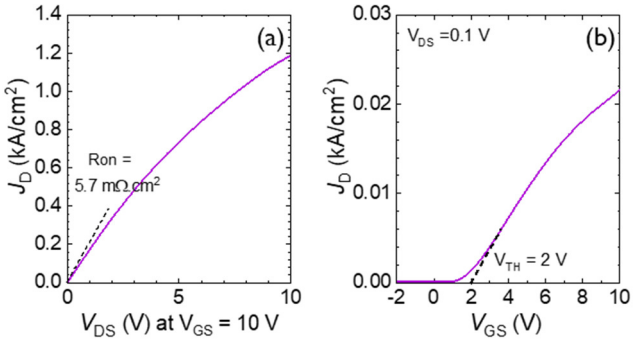

Fig. 8. Typical (a) output and (b) transfer characteristic of trench gate MOSFET device.

CONCLUSIONS

We demonstrated crack-free 5.4 µm-thick high quality MOCVD-gown GaN epitaxial layers on 200 mm engineered substrates, with a good control of wafer bow and a diode blocking capability of 440 V. A next generation epitaxial stack has been developed approaching 1.5×10^{16} cm^{-3} net doping concentration in the n^- drift layer combined with a very good and uniform crystal quality, with the GaN <102> peak as low as 400 arcsec. A semi-vertical trench gate MOSFET device architecture has been used to demonstrate the excellent device performance in ON-state, reaching 1.2 kA/cm^2 and a low on-resistance of 5.7 mΩ·cm.

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ACRONYMS

MOSFET: metal–oxide–semiconductor field-effect transistor
SEMI: Semiconductor Equipment and Materials International
CMOS: complementary metal-oxide-semiconductor
MOCVD: Metal-organic chemical vapor deposition
uid-GaN: unintentionally doped GaN
SEM: Scanning Electron Microscope
SIMS: Secondary-ion mass spectrometry
XRD: X-ray diffraction
FWHM: Full width at half maximum of XRD profiles
L_{SG}: Source-to-Gate Length