Evaluation of novel iron-free QuanFINE® structure by 100nm and 150nm AlGaN/GaN HEMT technology

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Keywords: Epitaxy, AlGaN/GaN, QuanFINE®

Abstract:

This work evaluates SweGaN's novel QuanFINE® structure with the UMS 100 / 150nm GaN-HEMT technology, in comparison to GH15-10 reference material based on AlGaN/GaN grown on a thick Fe-doped buffer. Characterizations focus on electrical DC- and RF-parameters obtained on process control monitors after front side processing and first robustness assessment by DC-step stress testing.

INTRODUCTION

Conventional AlGaN/GaN structures are typically grown on semi-insulating SiC substrates using a 1µm to 2µm C- or Fe-doped GaN buffer layer. The thick buffer layer is mandatory to reduce growth defects resulting from lattice mismatch to the substrate material. Isolation and therefore confinement of the 2DEG in the GaN channel is realized by the dopants forming deep acceptor traps [1,2]. Unfortunately, these traps have been identified as a source of DC- and RF-dispersion effects [3,4] such as drain- or gate lag which limits RF-performance as well as introduce unwanted memory effects with long time constants. SweGaN recently introduced a "buffer-free" GaN-on-SiC HEMT structure [5] demonstrating competitive RF-performance using a 250nm gate length HEMT technology. Here, the AlN nucleation layer acts as a back barrier of an unintentionally doped sub micrometer GaN layer.

In this work UMS has extended the evaluation of the QuanFINE® structure to reduced gate lengths of 100nm through comparison to conventional AlGaN/GaN structure based thick Fe-doped buffer material.

EXPERIMENTAL

Description

QuanFINE® features an iron-free HEMT hetero-structure with GaN channel (<250 nm), where electrons are confined in a 2DEG between the front-side and backside barrier formed by the AlN nucleation layer. To evaluate this structure for gate lengths down to 100nm, the channel thickness has been reduced from sample A to C. The barrier structure is similar to the reference sample in all cases. Table I summarizes the key electrical epitaxy properties, where QuanFINE® structures compare well to conventional AlGaN/GaN reference material based on a thick Fe-doped buffer.

Wafers were fabricated at UMS using the qualified high-performance GH15-10 GaN-HEMT technology. To assess the pinch off properties of HEMT devices, the gate length was varied between 150nm and 100nm using the UMS dielectric assisted gate technology to realize a slanted gate-foot profile.

TABLE I KEY EPITAXY PARAMETERS.

Sample	A	B	C	Ref
Rsheet (Ω/sq)	289.2 σ=0.8	294.7 σ=0.5	294.2 σ=1.1	295.8 σ=2.0
µ (cm²/Vs)	2090	2074	2138	1960
Ns (1/cm²)	1.1+e13	1.0e+13	1.0e+13	1.1e+13

Results

After front-side processing, manual and automatic electrical characterization was undertaken on process control modules uniformly distributed over the 4" wafer.

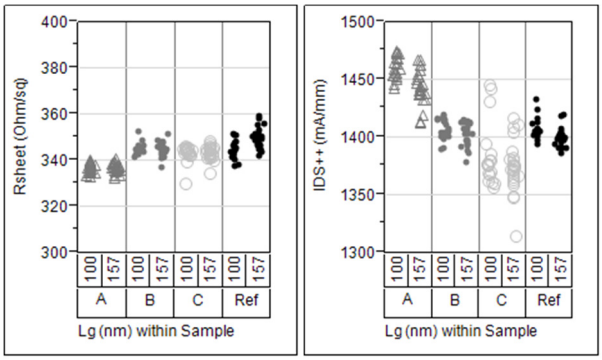

Fig. 1. Sheet resistance (l) and maximum drain saturation current (r) at VDS = 7V, VGS = +3V.

As shown in the left part of Fig 1, the sheet resistance from TLM measurements of QuanFINE® epitaxy is similar to the reference material. The maximum drain current density IDS++ depends on the QuanFINE® channel thickness and demonstrates a similar level for sample-B compared to the reference (Fig. 1, right).

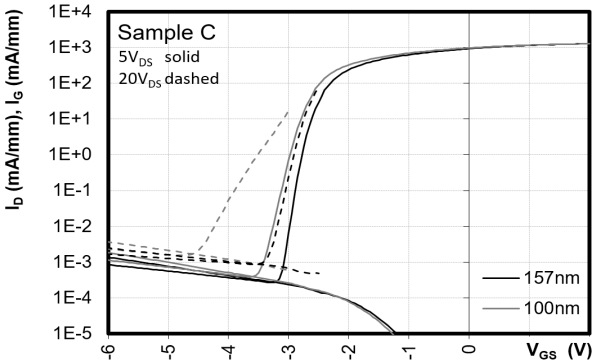

Fig. 2. Sub threshold characteristics of sample-C.

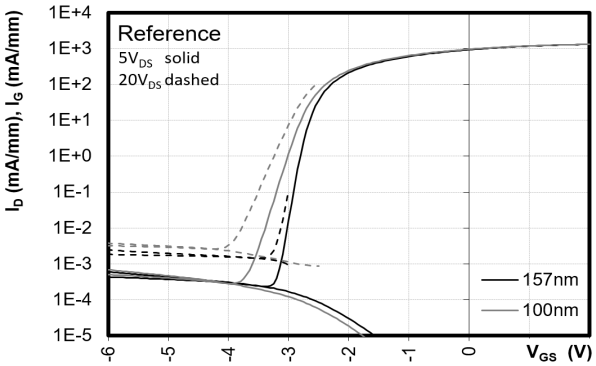

Fig. 3. Sub threshold characteristics of the reference.

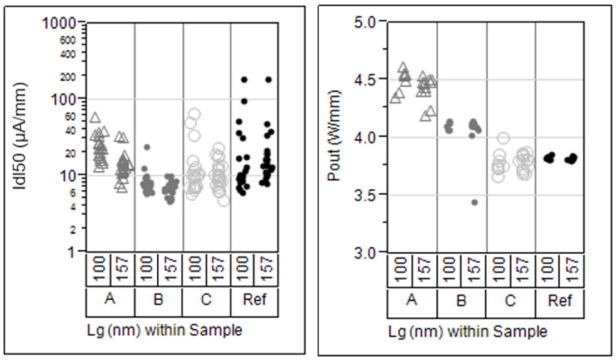

Fig. 4. Drain leakage (l) at VDS = 50V, VGS = -7V and 9GHz RF-output power density (r) on 8x75µm device operated at VDS = 20V.

The comparison of pinch off behavior for sample-C (Fig 2) with the thinnest channel and the reference (Fig 3) is shown for both gate lengths for VDS = 5V and 20V. While similar properties are observed for the nominal gate length devices, a clean pinch off behavior becomes difficult to achieve for sample-C for 100nm gate lengths. However, drain leakage density remains well below 100 µA/mm at Vds = 50V on all samples as shown in the left part of Fig 4. Transistor saturated RF-output power at 9GHz and 20V drain bias between 3.7 and 4.5 W/mm (Fig 4, right) shows a good correlation for samples A-C with the maximum drain saturation current in Fig 1.

Large-signal RF power sweeps in a 50Ω environment at VDS = 20V and low quiescent bias (Idq = 50mA/mm) are used to identify weak channel charge confinement, indicated by gain expansion between low (-5dBm) and high (+15dBm) input powers as shown in Fig 5 and Fig 6. Sample-B and C are stable for 150nm gate lengths, however sample-A with the thickest channel, shows gain expansion of approximately 1dB. For a 100nm gate length, sample-C shows more than 1dB gain expansion, confirming marginal charge confinement, as already expected from sub-threshold characteristics (Fig 2).

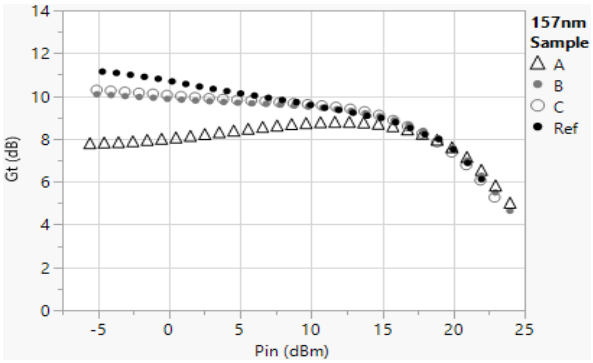

Fig. 5. 50Ω power sweep at 9GHz on 8x75µm FET with 150nm gate length operated at VDS = 20V/Idq = 50mA/mm.

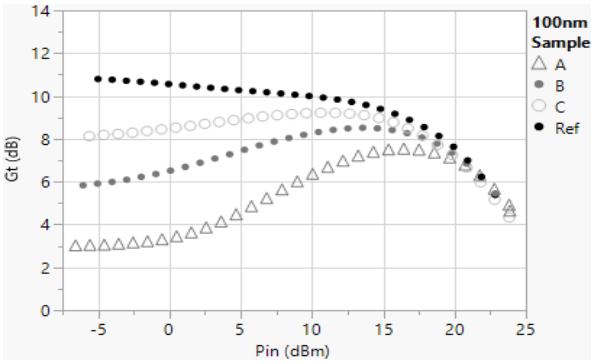

Fig. 6. 50Ω power sweep at 9GHz on 8x75µm FET with 100nm gate length operated at VDS = 20V/Idq = 50mA/mm.

To assess device robustness wafer level reliability tests on 150nm gate length at 150°C back plate temperature have been undertaken on 2x40µm devices operated in a pinched-off condition at VGS = -7V and application of an increasing VDS between 30V and 120V in 10V steps with intervals of 30 minutes for each step. Devices were characterized between each step. The evolution of the drain saturation current IDSS at VDS = 7V, VGS = 0V and the pinch off voltage VG100 at 1% of IDSS are shown in Figures 7 and 8, respectively for

this test. The reference device reveals a slight decrease in drain saturation current and positive shift in pinch off before failing at Vds = 100V, which is in accordance to the limitation of the thick Fe-doped buffer for the given device geometry of the test structure. All QuanFINE® devices pass the step stress test until the limit at 120V without failure and independent of channel thickness, indicating improved device robustness due to the novel epitaxial structure. Drift of the drain saturation current and the pinch off voltage are similar for samples A-C, where absolute values correlate with the channel thickness. However, drift of the pinch off is more pronounced on the QuanFINE® devices and may relate to charging effects in the AlN nucleation layer. Anomalies in pinch off voltages at Vds = 80V and 110V on sample A and B were not found to be systematic on the four stressed devices per wafer. No such behavior was observed on sample C with the thinnest channel or the reference material. Additional statistics for device robustness and life tests in package are required for better understanding of device stability.

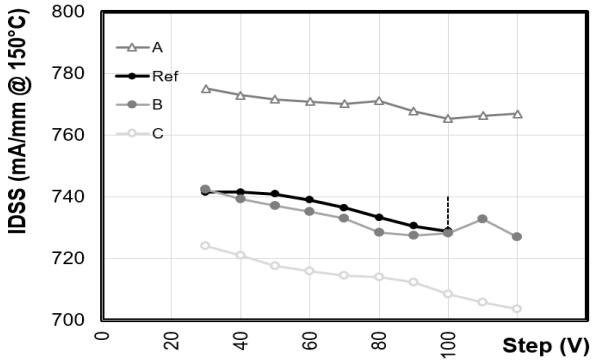

Fig. 7. Drain saturation current IDSS at VDS = 7V, VGS = 0V at 150°C after each step of DC-step stress testing in pinched conditions at VGS = -7V and 30min per VDS-step.

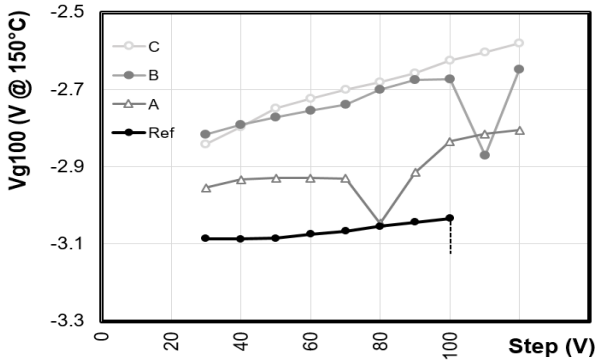

Fig. 8 Pinch off voltage VG100 at 1% of IDSS at 150°C after each step of DC-step stress testing in pinched conditions at VGS = -7V and 30min per VDS-step.

CONCLUSIONS

This paper reports first HEMT device performance using SweGaNs novel "iron-free" QuanFINE® material in conjunction with the UMS high performance GH15-10 (150nm gate length) technology [6, 7]. Medium channel thickness material demonstrated excellent performance compared to conventional AlGaN/GaN reference material based on a thick Fe-doped buffer on SiC substrate. Initial indications show improved device robustness under high Vds and pinched-channel conditions. Charge confinement could be further improved by reducing the channel thickness; however, further material optimization is necessary to reduce RF gain expansion for very short gate lengths devices (100nm). Although more analysis is required to compare the RF-performance at 30GHz, memory effects and the long-term performance of packaged devices, SweGaN material QuanFINE® is seen as a very promising alternative to the conventional thick Fe-doped buffer layers in next generation GaN HEMT design.

ACKNOWLEDGEMENTS

Part of this work was financially supported by the ECSEL JU under grant agreement No 783274, project 5G_GaN2. This project is part of the European Union's Horizon 2020 Research and Innovation Program. The content is to the responsibility of the authors.

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ACRONYMS

DC: Direct Current
2DEG: 2-Dimensional Electron Gas
HEMT: High Electron Mobility Transistor
Ref: Reference sample
RF: Radio Frequency
UMS: United Monolithic Semiconductors