# Thin $Al_{0.5}Ga_{0.5}N$/GaN HEMTs on QuanFINE® Structure

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**Abstract**

**The performance of HEMTs fabricated on a thin $Al_{0.5}Ga_{0.5}N$/GaN heterostructure with a total barrier thickness of 6.5 nm is presented and benchmarked to the epi-structure with a 13 nm thick $Al_{0.3}Ga_{0.7}N$ barrier on an identical QuanFINE® structure. DC transfer characteristics on both samples with a gate length of 100 nm demonstrate a high current above 1 A/mm. A higher extrinsic $g_m$ of 550 mS/mm is measured on the sample with a thinner high Al content barrier. Moreover, low trapping effects with a 12-14 % buffer-related dispersion at a $V_{DSQ}$ of 25 V are characterized for both samples, which indicate the advantage of the iron-free QuanFINE® heterostructure.**

## Introduction

GaN HEMTs are gaining attention in the applications of high-frequency devices due to high breakdown voltage and high electron mobility, which yield a high power density with good efficiency. AlGaN barrier with a thickness above 10 nm and the Al composition beneath 30 % is commonly utilized for GaN HEMTs [1]. However, the transconductance ($g_m$) is limited due to the thick barrier layer. Therefore, a thinner AlGaN barrier with higher Al content (>30 %) is proposed to improve gate response [2]. Lattice-matched InAlN barrier is another approach to reduce the barrier thickness, which has a higher 2DEG density than the AlGaN barrier thanks to a stronger polarization force. However, plausible Indium aggregation in the barrier might limit the reliability of devices [3].

The buffer is conventionally Fe or C doped to render good isolation [4]. However, devices made on Fe- or C-doped buffers suffer from trapping effects. Recently, a novel QuanFINE® heterostructure, which has a thin UID-GaN layer sandwiched in between a barrier and an AlN nucleation layer, potentially allows the AlN nucleation layer to act as a back-barrier and to reduce the trapping effects [5, 6].

In this study, the first demonstration of a high Al-containing thin $Al_{0.5}Ga_{0.5}N$ barrier on a QuanFINE® structure was investigated. Device fabrication with DC and pulsed-IV characterization will be presented.

## Epi-Growth

The epitaxial layers were grown on a semi-insulating SiC substrate utilizing a MOCVD by SweGaN. Using SweGaN proprietary epitaxial growth process, a low thermal-boundary-resistance AlN nucleation layer was grown and followed with a 250 nm UID-GaN layer [5, 6]. On top of this, a 5.0 nm $Al_{0.5}Ga_{0.5}N$ layer (1.5 nm AlN exclusion layer and 3.5 nm $Al_{0.5}Ga_{0.5}N$ layer), and a 1.5 nm GaN cap layer were grown as the active layers (denoted as $Al_{50}$, Fig. 1a). A $n_s$ of $1.22 \cdot 10^{13}$ $cm^{-2}$ and a $\mu_e$ of 1700 $cm^2/V \cdot s$ were characterized by contactless Hall measurements (Lehighton) and $R_{sh}$ of 315 $\Omega$/sq was characterized by Eddy current measurement after epitaxial growth. These values demonstrate the good 2DEG properties achievable with a thin $Al_{0.5}Ga_{0.5}N$ barrier on QuanFINE®-structure. The other epi-structure which has an 1 nm AlN exclusion layer, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2 nm GaN cap layer with a $n_s$ of $1.16 \cdot 10^{13}$ $cm^{-2}$, $\mu_e$ of 2030 $cm^2/V \cdot s$, and $R_{sh}$ of 286 $\Omega$/sq was grown on nominal QuanFINE®-structure (denoted as $Al_{30}$, Fig. 1b) to benchmark to $Al_{50}$. [6]

## Device Fabrication

The epi-wafers were cleaned by the RCA cleaning process followed by a passivation-first 60 nm thick SiN layer deposited by LPCVD before device processing. Mesa etching was defined for device isolation and the ohmic contacts were achieved by deeply recessed Ta-based metal stacks [7]. A low $R_c$ of ~0.3 $\Omega$mm for both samples is characterized by TLM measurements. Two-fingers gates with passivation-assisted field plates, which have an $L_g$ of 100 nm and a gate width of 2x50 µm were defined by e-beam lithography with metal evaporation followed by lift-off process (Fig. 1).

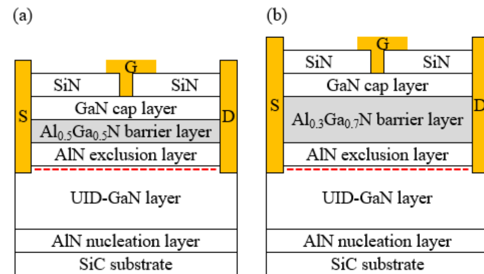


Fig. 1. Schematic of device layout for (a) $Al_{50}$ and (b) $Al_{30}$.

## HEMTs Results

Different I-V measurement windows ($V_{GS}$) were performed on two samples due to the shifting of $V_{TH}$. HEMTs on both samples show a high $I_{DS}$ of ~1.1 A/mm (Fig. 2). A higher extrinsic $g_m$ of 550 mS/mm and a $V_{TH}$ of -0.9 V were measured on $Al_{50}$ as compared to that on $Al_{30}$ with a $g_m$ of 500 mS/mm and a $V_{TH}$ of -1.8 V (Fig. 3) [6], which are mainly caused by a thinner AlGaN barrier. Short channel effects are revealed on $Al_{50}$ and $Al_{30}$ at high drain bias with an average DIBL shifting of 82 mV/V, and 50 mV/V, respectively, extracted at the $I_{DS}$ of 1 mA/mm, while over the range of measured $V_{DS}$ from 1 to 25 V (Fig. 4). A higher leakage current was measured on $Al_{50}$, which might be caused by a thinner barrier with a different Schottky barrier condition. These results indicate that further buffer confinement and mitigation of leakage currents are required for short gate length devices.

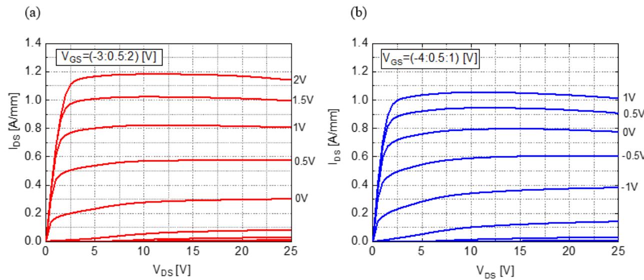


Fig. 2. I-V measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

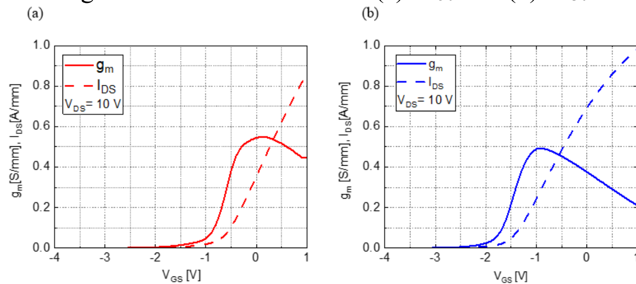


Fig. 3. $g_m$ measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

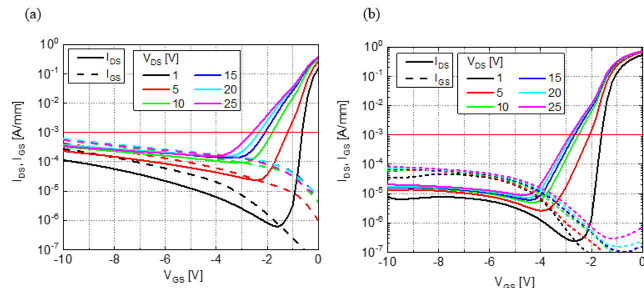


Fig. 4. DIBL measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

A low surface-related current collapse of 0.5 % and 4 % were measured on $Al_{50}$ and $Al_{30}$, respectively, which indicate that the LPCVD SiN passivation is compatible with different barrier design (Fig. 5). Moreover, low buffer-related dispersion of 12 % and 14 % for $Al_{50}$ and $Al_{30}$, respectively, highlight the advantage of using QuanFINE®, which removes the intentional iron and carbon dopants in GaN.

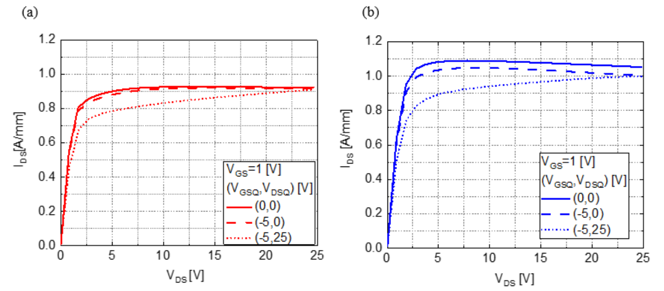


Fig. 5. Pulsed-IV measurements for (a) $Al_{50}$ and (b) $Al_{30}$.

## Conclusions

A 50% Al content thin AlGaN barrier is successfully grown on QuanFINE® heterostructure with excellent 2DEG properties. High $I_{DS\text{-}sat}$ and $g_m$ combined with low trapping effects can potentially translate to a better large-signal RF performance. Further improvements of the 2DEG confinement from the backside such as inserted AlGaN back-barrier and/or reduced UID-GaN layer thickness of QuanFINE® are required for highly down-scaled HEMT technologies.

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## ACRONYMS

HEMTs: High electron mobility transistors
$L_g$: Gate length
$I_{DS}$: Drain-source current
$I_{DS-sat}$: Drain-source saturation current
$R_c$: Contact resistance
$R_{sh}$: Sheet resistance
$n_s$: 2DEG concentration
$\mu_e$: Electron mobility
2DEG: Two dimensional electron gas
UID-GaN: Unintentional doped-GaN
LPCVD: Low pressure chemical vapor deposition
$V_{GS}$: Gate-source voltage
$V_{TH}$: Threshold voltage
DIBL: Drain induced barrier lowering