**Silicon Photonics and Hybrid Silicon Laser Technology**

Ranju D. Venables

Silicon Photonics Product Division, Data Platforms Group, Intel Corporation, 3600 Juliette Lane, Santa Clara, CA 95054.

ranju.d.venables@intel.com

## **Keywords: Silicon Photonics, Compound Semiconductor, Lasers, Indium Phosphide, Photonic Integrated Circuits**

## **Abstract**

**Intel’s Silicon Photonics (SiPh) platform combines two significant technical achievements of the 20th century—CMOS processing and the semiconductor laser. SiPh provides a disruptive approach to design and build high speed optical transceivers for datacom and other applications with the potential of lower cost and higher scalability than traditional discrete or III-V monolithic approaches. The high refractive index of silicon allows for low loss optical waveguides with small radius of curvature, enabling integration of wavelength multiplexers, multi-mode interference couplers, tap couplers, Bragg gratings and other optical functionalities used in photonic integrated circuits (PICs). The ability to leverage well established equipment and processes used in the microelectronics industry allows for the mass-production of photonic chips with tight process control, high yield, integration, and wafer-level testing which may be difficult to achieve in traditional compound semiconductor (III-V) optoelectronic semiconductor foundries.**

**The main challenge with traditional SiPh is the hurdle to fabricate and integrate an efficient laser due to the indirect bandgap of silicon. Intel’s process uses wafer bonding to combine III-V based compound semiconductor materials on SOI wafers. Light from the silicon waveguides can be evanescently coupled to an active III-V material bonded onto the silicon to provide active optical functionalities such as gain, photodetection, and phase/amplitude modulation. The active material is composed of compound semiconductor materials, such as Indium Phosphide (InP) and InP based alloys, which are the traditional materials of choice for high-performance, long wavelength, lasers. This heterogenous integration approach, in a way, allows for the best of both worlds to be combined: Low loss, low cost silicon passive components and high-performance light emission of III-V compound semiconductor materials. Bonding optically active III-V materials does not require precise alignment and further III-V processing does not adversely affect the silicon components. Intel is currently shipping 100G products in high volume and starting high volume shipment of 200G & 400G SiPh products in 2020.**

## Introduction

Within the past decade, Silicon Photonics (SiPh) has experienced an explosive development and deployment into datacom and telecom sectors and more recently is also entering new markets such as automotive (LIDAR), optical switches, artificial intelligence, gyroscopes, sensors, and computing. The recent growth of silicon photonics has been driven by the ever-increasing demand from the hyperscale data centers, high-performance computing and sensing applications. Silicon photonics is a disruptive technology as it leverages existing CMOS fabrication infrastructure for high volume manufacturing at low cost. Hundreds or thousands of photonic components can be integrated to create photonic integrated circuits (PIC) on the silicon platform. Fig. 1 [1] shows the rapid increase in integration of the number of components as a function of time.

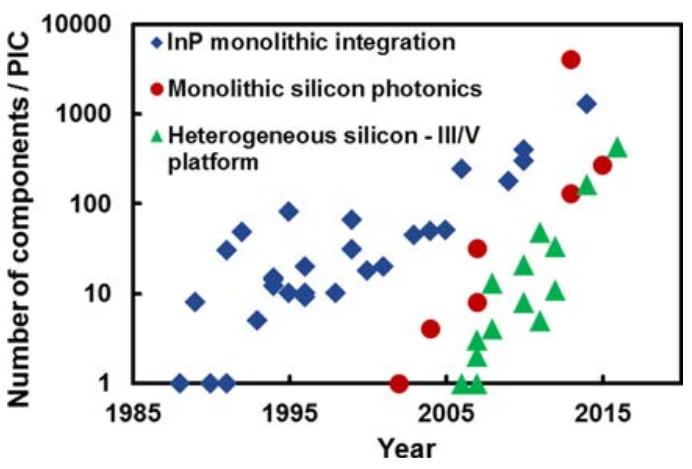


Fig. 1. Integration of the number of components in photonic integrated circuits. [1]

SiPh promises to revolutionize the photonics industry similar to what CMOS technology did in the microelectronics industry: by driving down chip cost and enabling higher levels of integration and functionality. Silicon photonics not only has the advantage of established and scalable CMOS manufacturing but also optimizes on the benefits from the high refractive index contrast from stable silicon dioxide which enable smaller waveguides and denser optical chips. Being transparent at wavelengths greater than ~1100nm, allows its application to the C and O-band communications space. However, Si is an indirect bandgap semiconductor and therefore not capable of efficient radiative recombination. Historically, multiple approaches using optical pumping and Ge-based structures were pursued to create optical emitters, but these were unable to achieve commercialization [2]. Approaches that have been commercially successful are based on the integration of compound semiconductor material in the Si platform.

## Heterogenous integration on silicon platform

Multiple approaches to integrate compound semiconductor-based lasers and/or material on Si exist, though each have their own advantages and disadvantages. Examples of approaches that have found their way to commercialization include pure compound semiconductor / III-V based PICs (specifically on InP for telecom/datacom applications), SiPh combined with external laser, and heterogenous integration of III-V on Si or SOI (Silicon on Insulator) wafers [3]. In addition, approaches are being pursued for direct epitaxial growth on Si [4] for the future. Plasma assisted bonding successfully demonstrated in 2006 [5] is an approach to directly bond III-V to Si. A schematic of this process is shown in Fig.2. The ability to combine compound semiconductors with Si leverages the optimal properties of both materials on a single chip – optically active III-V compound semiconductor materials combined with low loss Si photonic passive and high speed components. The optimal approach is utilization of combining compound semiconductors for performance benefit, while minimizing area used to reduce cost and leveraging the cost and performance benefits from Si photonics components.

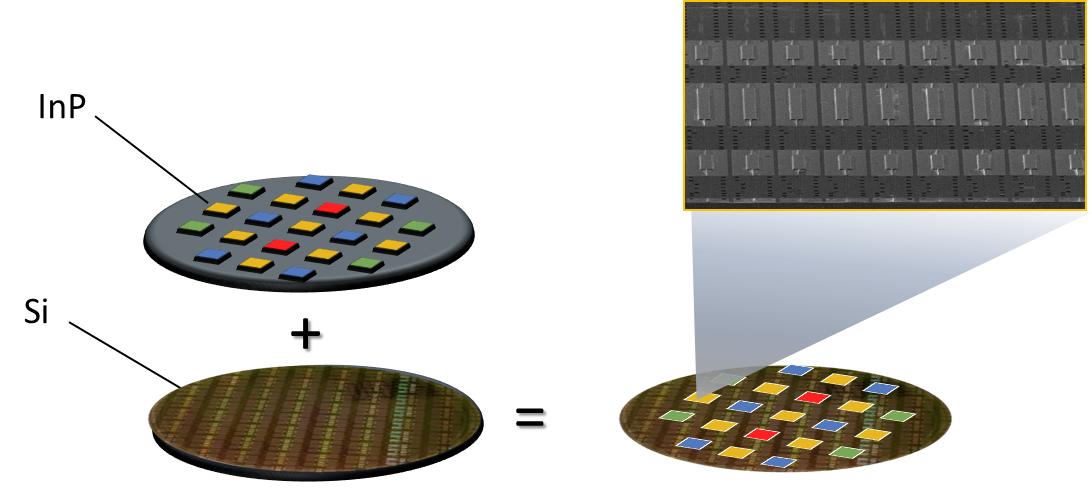


Fig. 2. Schematic of heterogenous integration of compound semiconductor on silicon platform.

The plasma assisted bonding approach was pioneered by the University of California, Santa Barbara and Intel, and has achieved traction with many demonstrations for lasers, as well as other devices such as amplifiers, modulators, etc. [6]. As outlined in Fig.3, Intel’s hybrid laser fabrication process includes leveraging well established lithography capability to define a rib waveguide with grating and O2 plasma assisted bonding of compound semiconductor to Si. Pieces of compound semiconductor (specifically, InP) dies are bonded to SOI wafer. After bonding the III-V to the SOI the bulk compound semiconductor substrate is removed leaving the epitaxially grown layers for device fabrication. Subsequently, lasers are fabricated from these bonded pieces by standard methods of etching, implantation, metallization and testing.

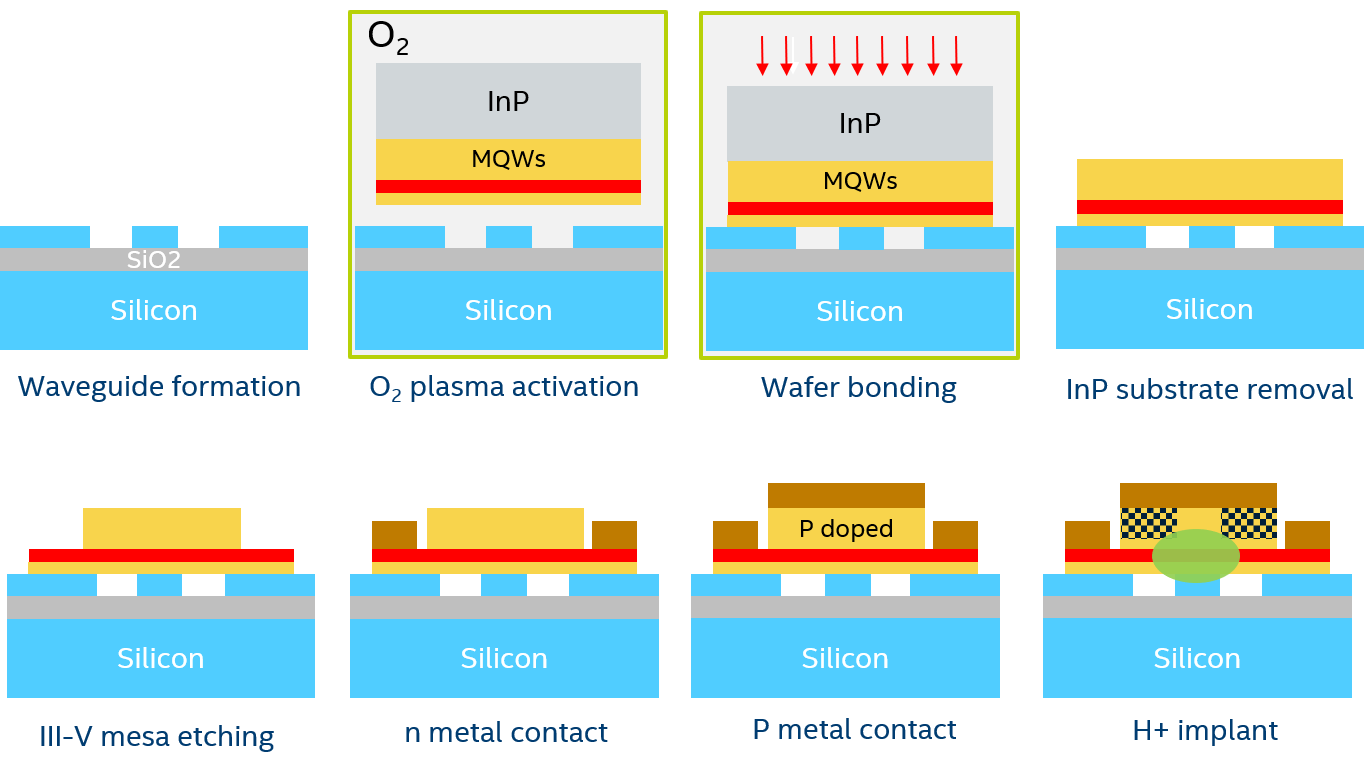


Fig.3. Schematic of plasma assisted bonding of epitaxial III/V based materials on Si / SOI wafers.

The plasma assisted bonding of III-V to Si does not require critical alignment steps as it is done with un-patterned compound semiconductor / III-V based wafers. In addition, the compound semiconductor wafer size to Si process is scalable and wafer size agnostic. A single III-V die with epitaxial layers, can be bonded over several waveguides to create multiple lasers from a single bond. Further, different epitaxial designs can be bonded on different areas of the Si photonic chip to obtain different functionality in various parts of the SiPh chip. Also, this approach allows us to leverage decades of existing commercially established gain material growth techniques such as MOCVD (Metal Organic Chemical Vapor Deposition). These MOCVD grown epitaxial materials can be fully characterized to determine material properties and then integrated in selected locations on the SOI wafers. Intel has successfully demonstrated the commercial implementation of this approach in their CWDM4 (Coarse Wavelength Division Multiplexing) products which have now shipped in millions in the field.

## Performance and reliability of intel hybrid laser

Intel’s 100G CWDM4 products are comprised of 4 heterogeneously integrated InP-based gain elements for the fabrication of hybrid lasers on the 300mm Si platform. These lasers can operate over a temperature range of -20C to 95C, with transmitters supporting reaches up to 10km. CWDM4 laser arrays are challenging to fabricate due to the large optical bandwidth needed with channel separation of ~20 nm – therefore, a single optically active compound semiconductor gain material is unable to meet the entire CWDM band requirements. The wafer bonding capability to integrate multiple different compounds semiconductors on the SiPh platform, however, allows multi-wavelength scaling. Well established optical lithography is used to define grating periods which can be tuned and optimized for different laser wavelengths on different waveguides in the multi-wavelength laser array. An example of laser output optical power over temperature of Intel’s hybrid laser technology is shown in Fig. 4.

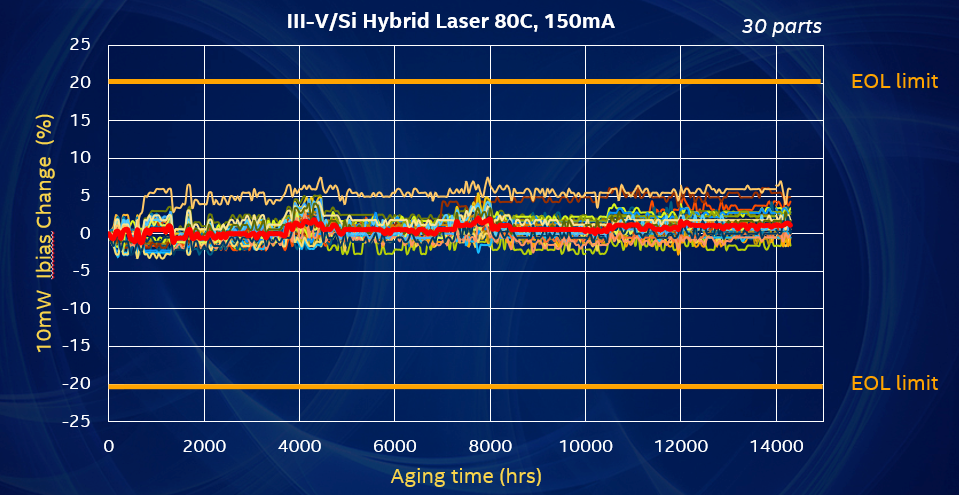


Fig. 6. Excellent long-term stability of Intel’s hybrid laser with average drift of ~1% bias change over 15K hours.

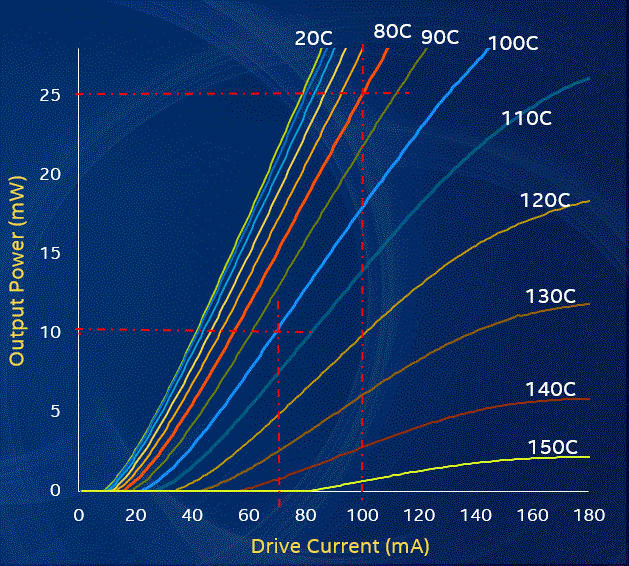


Fig.4. Output optical power (coupled in the Si waveguide) versus current characteristics of 1310 nm III-V-Si DFB laser from 20C to 150C by 10C step.

Fig.5 shows output optical power as a function of bias current for 4 different wavelengths/channels.

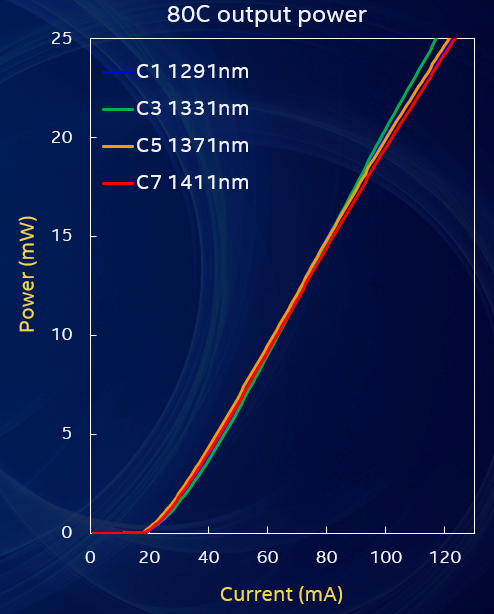


Fig. 5. Output optical power from 4 DFB lasers at 80C showing cross wavelength uniform performance.

Intel has shipped more than 10 million lasers in CWDM4 pluggable transceiver modules for data centers. The hybrid lasers used in the modules meet all Telcordia requirements. As a result of the hybrid laser architecture, Intel’s lasers do not suffer from facet failure or facet degradation. Also, Intel’s hybrid laser design has the added advantage of a smaller junction temperature increase and ~5X lower current density compared to other typical III-V based directly modulated lasers resulting in exceptionally low field failure rate. HTOL (High Temperature Operating Lifetime) data of 30 units is shown in Fig.6. The data shows excellent long term stability with an average drift of ~1% over 15K hours at 80C and 2X typical operating current.

## Conclusions

Intel has successfully demonstrated and deployed millions of optical transceiver modules leveraging integration of compound semiconductors on a silicon platform. The versatility of this platform can be further extended to developing higher performing optical devices, enhanced integration and on chip co-packaging, and integration of a variety of materials to the Si platform. In addition, approaches related to direct epitaxial growth on Si are also being pursued for specific applications [4, 7].

## Acknowledgements

The author would like to thank Richard Jones, Yuliya Akulova and Robert Blum for their support and Silicon Photonic Product Division, F11X (Rio Rancho, New Mexico), and Quality and Reliability engineers at Intel Corp who made the results discussed in this article possible.

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Acronyms

CWDM: Coarse Wavelength Division Multiplexing

InP: Indium Phosphide

HTOL: High Temperature Operating Lifetime

MOCVD: Metal Organic Chemical Vapor Deposition

PIC: Photonic Integrated Circuits

Si: Silicon

SOI: Silicon on Insulator

SiPh: Silicon Photonics