A Study of Wafer-Scale Breakdown Characteristics of Vertical GaN PIN Rectifiers

Minkyu Cho[1], Matthias A. Daeumer[2], Jae-Hyuck Yoo[2], Marzieh Bakhtiary-Noodeh[3], Qinghui Shao[2], Zhiyu Xu[1], Theeradetch Detchprohm[1], Russell D. Dupuis[1, 3], and Shyh-Chiang Shen[1, *]

[1]College of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
[2]Lawrence Livermore National Laboratory, Livermore, CA, USA
[3]College of Material Science and Engineering, Georgia Institute of Technology, Atlanta, GA, USA
[*]POC email: shyh.shen@ece.gatech.edu

Abstract

We report the development of vertical GaN PIN rectifier fabrication processing using an ion implantation isolation technique to create floating field guard ring (FGR) structures. With proper engineering in implantation profile and FGR geometries, fabricated devices demonstrated uniform blocking voltage (BV) for 1.2-kV-class devices across a 2-inch free-standing GaN substrate. A material analysis technique that can quickly detect bulk defects in the wafer scale was developed using a confocal photoluminescence under sub-bandgap photon excitation at λ = 400 nm. The wafer-mapping capability was used to investigate the correlation between bulk impurities and the BV performance.

Keywords: High power switches, GaN, photoluminescence, rectifiers, wafer-level characterizations.

Introduction

Gallium Nitride (GaN) is a wide-band-gap semiconductor that is widely used in optoelectronics and power electronics. For GaN devices to reach theoretical power switching limits with reliable operation, it is crucial to mitigate field crowding effects [1] [2]. This may be achieved with effective electrical field termination at the edge of the active device region.

In this paper, we report the development of a novel floating field guard ring (FGR) field termination technique for vertical GaN PIN rectifiers. The FGRs were formed by alternating the p-type GaN layer and highly-resistive GaN layer in the lateral extent of the devices. The highly-resistive GaN layer were created by selective-area ion implantation with nitrogen ion species. The nitrogen ion implantation creates controlled number of donor-like nitrogen vacancies and formed a compensated semiconductor in the implanted region. With proper choices of implantation schedule, we achieved effective field termination for vertical GaN PIN rectifiers for 1.2-kV-class applications. The developed processing technique implemented on a 2" free-standing GaN substrated exhibited uniform and reliable breakdown characteristics on the wafer scale.

To understand the impact of as-grown defects in GaN on device performance, a confocal photoluminescence under a sub-bandgap photon excitation at λ = 400 nm was used to investigate the correlation between bulk impurities and the BV performance as well as the effect of different floating guard ring (FGR) designs on device performance.

Material Growth and Device Fabrication

GaN p-i-n APD epitaxial structures were grown on a 2-inch free-standing GaN substrate using an AIXTRON 6×2" close-coupled showerhead (CCS) metalorganic chemical vapor deposition (MOCVD) reactor. The epitaxial layers consists of 1000-nm *n*-type GaN:Si layer ([*n*] ~ 7×10^{18} cm^{-3}), a 8-µm undoped GaN drift layer ([*n*] ~ 2×10^{16} cm^{-3}), and a 450-nm *p*-type GaN:Mg layer ([*p*] ~ 2×10^{18} cm^{-3}).

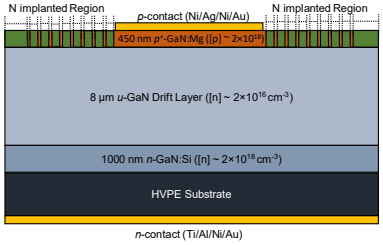

Figure 1. A schematic cross-section drawing of a vertical GaN *p-i-n* rectifier with nitrogen-implanted isolation and FGR design. Nitrogen implanted area is the green-colored region.

In this study, FGRs were designed specifically for a blocking voltage of 1.2 kV. These designs were performed in a TCAD Sentaurus™ simulation package and were reported earlier in [3]. Proper choices of the nitrogen ion-implantation energy and doses were chosen following the design strategies as reported in [4] to achieve effective device isolation and for the FGR formation. A schematic cross-sectional view of the vertical GaN PIN rectifiers with the FGRs is shown in Figure 1. Figure 2(a) shows a typical FGR design that effectively mitigate the electric field distribution by extending the depletion regions throughout the FGR. By properly choosing the gaps of the p-GaN guard rings, (e.g., < 2 µm for 1.2 kV of BV), Figure 2(b) shows uniform potential gradient along the FGR. As a result, the field crowding effect and premature surface breakdown can be effectively mitigated.

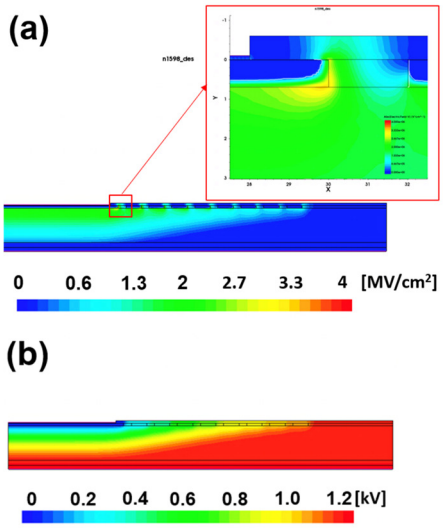

Figure 2. TCAD simulation of the vertical GaN p-i-n rectifier with 8 FGRs (FGR gap=2µm, width=4µm) at reverse bias -1200V: (a) Electric field distribution, (b) Potential distribution.

The device fabrication processing started with a backside *n*-type metallization with Ti/Al/Ni/Au stack followed by a nitrogen ion implantation for device isolations A three-step ion implantation schedule was implemented with energies of 45 keV, 140 keV, and 290 keV, respectively, to achieve flat implantation profile and to form an "isolation" layer by compensating the Mg dopants in the *p*-GaN and for the formation of FGRs. After the ion implantation, the *p*-contact was formed by Ni/Ag/Ni/Au metal stacks and the devices are passivated with SiO_2. A picture of completed vertical GaN *p-i-n* rectifiers on a 2-inch HVPE substrate is shown in Figure 3.

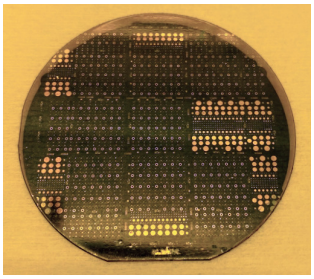

Figure 3. Fabricated vertical GaN p-i-n rectifiers grown on a 2" free-standing GaN substrate.

Device Performance Discussions

Figure 4 shows the forward bias characteristics of the devices. The ideality factor was 2.1, and the turn-on voltages were ~4.3 V at 100 A/cm^2. Typical specific-on resistance ($R_{on}A$) was 1.31 mΩ·cm^2 at 1.1 kA/cm^2. The $R_{on}A$ could be further reduced by driving the device to higher current density, as shown in the graph. Figure 5 shows a cumulated reverse-biased I-V curves of 120 randomly selected devices measured across the 2-inch wafer. Among these devices under tests (DUTs), 112 devices exhibited BV of greater than 1.1 kV. The devices that showed low BV < 1.1 kV were subject to further study. The majority of the low BV devices (6 devices) have apparent surface textures near or on the devices area. Some devices were intentionally fabricated on "dot-core" sites on the wafer (not shown in Figure 2), which resulted in premature breakdown less than 200 V. There were also 2 devices that we could not find reasons with visible indications for low BVs and will be subject to further investigation.

Figure 6 shows the correlation of the BV as a function of the device's diameters. Devices of the same diameters but with different number of FGRs were also populated in the plot. Except for devices sitting on the "dot core" site, the BV of the devices were around 1.2 kV regardless of the device diameters. This result may imply high-quality epitaxial layer growth and effective ion-implantation isolation technique was achieved in this work. In such device design, a buried junction structure that suppresses premature breakdown mechanism such as surface breakdown or field crowding effects. As a result, the breakdown voltage is predominantly dictated by the bulk material properties. It is concluded that the uniform device performance can be attributed to high-quality substrate, optimized epitaxial growth, and robust device fabrication on a wafer-level scale.

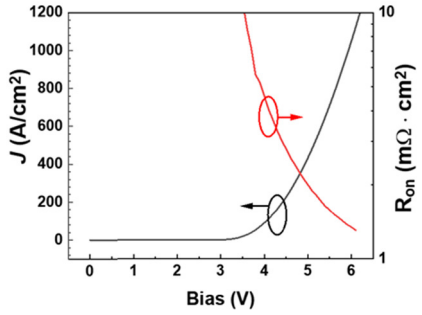

Figure 4. A forward I-V curve in linear scale with specific-on resistance ($R_{on}A$).

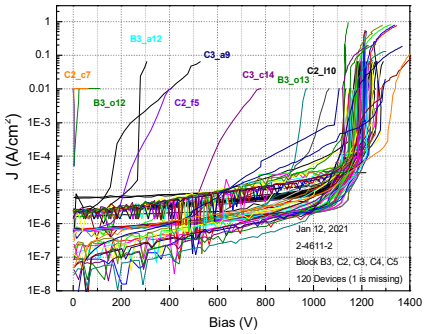

Figure 5. Reverse I-V characteristics of vertical GaN p-i-n rectifiers of randomly chosen 120 devices across a 2-inch wafer. The IDs of the devices with BV < 1.1 kV are marked in the plot.

WAFER-LEVEL SUB-BANDGAP CONFOCAL PHOTO-LUMINESCENCE STUDY

A confocal PL intensity imaging system was used to scan the 2-inch round GaN device sample. PL intensity associated with each device was compared to the device performance to understand how the bulk defects impact on the device leakage current, BV, and reliability. Surface defect-induced premature BV can be easily ruled out with an optical microscope as shown in Figure 7. Other defect-related early BV will be investigated further with the confocal PL. In the current PL system, a pulsed laser with 400 nm excitation wavelength is used, and broad band PL signals with wavelengths greater than 450 nm are collected. The PL signals are sensitive to point defects and their related defect complexes as they serve as radiative recombination centers. A higher PL intensity indicates a locally higher impurity level.

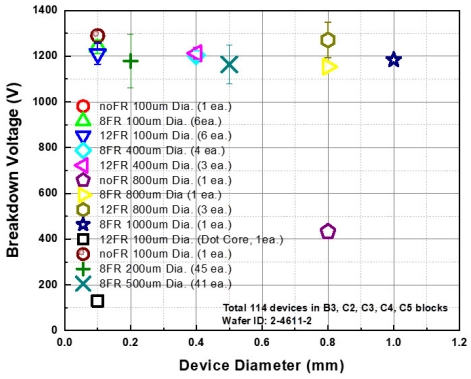

Figure 6. Breakdown voltage versus device diameters from 100 µm to 1 mm with different FGR designs.

Figure 8 shows PL intensity comparison of a 2-inch free-standing GaN substrate before and after *p-i-n* epilayer growth. The identical feature of periodical high PL intensity regions suggests that the impurities originate from the substrate, instead of epi-growth process. The HVPE substrate was presented with periodically positioned domains "cores" to concentrate the dislocations below the cores and reduce dislocation density elsewhere. During the epitaxial lateral over-growth, the impurities (e.g., oxygen) are incorporated to the semipolar planes and the process ends up with a higher impurity level at the coalescence region (dark red in PL map).

The HVPE substrate used in the study exhibited arrays of dot cores throughout the wafer with a 1-mm pitch. An interest of study may arise regarding the device performance variation relative to the presence of these cores. Figure 9 shows a study of the BV versus the distance of a 100-µm-dia. device to the nearest dot core sites. While most of the devices have BV greater than 1 kV, the devices fabricated on dot cores had BV less than 200 V. The results seemed to indicate that the areas outside of the dot cores could reliably yield high-performance electronics, while any devices ran across the core sites would result in premature breakdown features. For devices fabricated on the HVPE substrate, the BV is limited by dislocation density given that an optimized device design which prevents premature failure. The lowest PL signals were found in dot-core area. A threading dislocation can be modeled as a negatively charge cylinder which repels adjacent electrons to form a depletion region. The generated e-h-pairs are quickly separated, and no carrier recombination is represented in its vicinity [5-8]. However, the devices with distances to the dot cores greater than 200 µm did not show clear dot-core-dependent BV characteristics. This might be due to the reduced dislocation density in these regions [9].

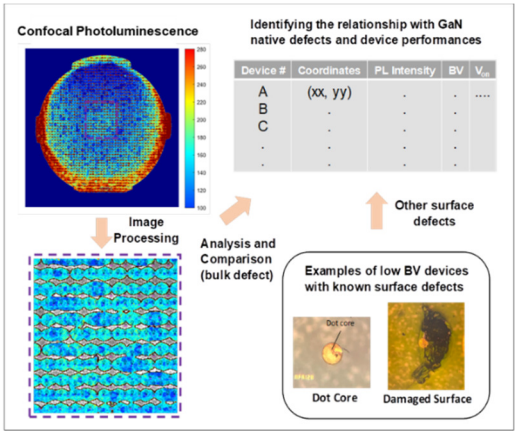

Figure 7. Schematic diagram of the material analysis and device characterization to identify the correlation between devices performance and defects. Surface defects can be easily identified with an optical microscope. Bulk defects could be identified with time-resolved confocal photoluminescence and image processing.

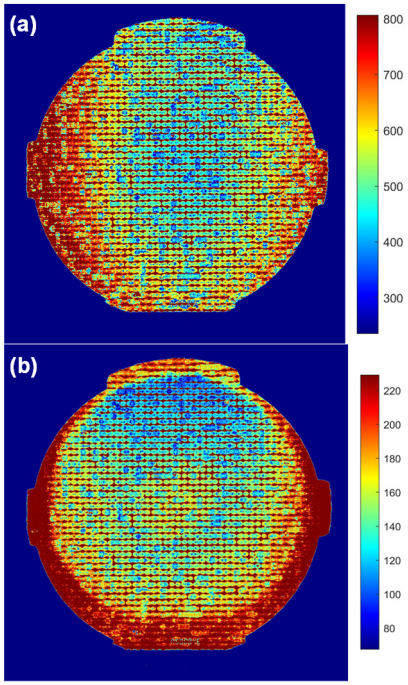

Figure 8. Confocal PL intensity maps (400 nm excitation) of a 2-inch GaN wafer (a) prior to epilayer growth and (b) post epilayer growth.

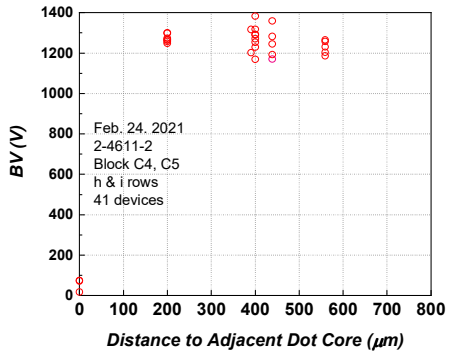

Figure 9. BV vs the distance to adjacent dot cores of 41 devices with 100 μm diameter.

The correlation between PL intensity and device BV was investigated related to data in Figure 9. However, there is no clear relationship discovered between impurity levels and the device breakdown voltage in this study. The impurity related defects are typically associated with device degradation. To understand the impact, high-temperature reverse bias (HTRB) and high-temperature operating life (HTOL) tests will be performed on selected devices in high PL and low PL intensity regions in future study.

CONCLUSIONS

Vertical GaN p-i-n rectifiers were fabricated on a 2-inch HVPE substrate. Proper ion implantation conditions using nitrogen ions were chosen to provide effective device isolation and novel ion-implantation enabled FGR designs. The TCAD device simulation was performed to optimize such FGR design and the device performance was experimentally validated. The fabricated devices demonstrated uniform and reliable operations of 1.2-kV BV that facilitate further study of device failure mechanisms related to the wafering and epitaxial material quality. A confocal PL was used to investigate the origin of premature BV devices associated with bulk defects. The result showed that the devices fabricated on dot core sites had significantly low BV. The location of dot core could also be identified with low PL signals. However, the devices with a distance to the adjacent dot cores are not impacted by high dislocation density concentrated in the dot cores. Further studies on bulk defects in the substrate, and its impact on long-term device reliabilities will be studied in the future.

ACKNOWLEDGEMENT

This work was supported by the U.S. Department of Energy (DOE), Office of Energy Efficiency and Renewable Energy (EERE), Advanced Manufacturing Office (AMO) and performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. DE-AC52-07NA27344, LLNL-ABS-820651.

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ACRONYMS

MOCVD: Metalorganic chemical vapor deposition
BV: blocking voltage
PL: photoluminescence
FGR: floating guard ring
HVPE: hydride vapor phase epitaxy
HTRB: high temperature reverse bias
HTOL: high temperature operating life