**The Effect of Delay Between Pre-metal Clean & Metal Deposition on the
Forward I-V Characteristics of Schottky Devices**

Debdas Pal, Lorain Ross, Sean Doonan and Eric Finchem

Skyworks Solutions Inc.,20 Sylvan Rd, Woburn, MA 01801

eric.finchem@skyworksinc.com, Phone: 781-376-3588

Keywords: GaAs, Schottky devices, ideality factor, series resistance, barrier height, thermoionic emission

Abstract

 **Schottky devices play an important role in modern electronics. The forward biased current-voltage characteristics of such devices are linear on a semi-logarithm scale at intermediate bias voltages. However, the curve deviates from linearity at higher voltage primarily due to series resistance. The applied forward voltage on the device is equal to the sum of the voltage drops across the (1) junction, (2) series resistance, (3) depletion layer and (4) any parasitic resistive layer between the Schottky metal and the semiconductor. Therefore, the interface between the metal and the semiconductor plays an important role in determining the critical parameters of Schottky devices. In this investigation a controlled delay was introduced between the pre-metal clean and Schottky metal deposition steps of the fabrication process to study the effects of naturally grown oxide on the forward characteristics of the Schottky devices. The results of the investigation indicate such delays cause significant increases in series resistance and ideality factor, as well as a decrease in barrier height.**

Introduction

 Schottky devices play an important role in modern electronics. Due to their relatively low turn-on voltages and low recovery times, they’re often preferred over PN junction devices in applications such as RF mixers/detectors, rectifiers and voltage clamps. Variation in process factors, such as the timing between consecutive process steps, can cause significant undesirable shifts and variability in device characteristics. The effects of a controlled delay between the pre-metal clean and the Schottky metal deposition in the fabrication of Schottky devices are the subject of this paper.

Experimental

 Planar Schottky devices were fabricated using a standard GaAs production process and MOCVD grown epitaxial wafers. The typical process routing includes a wet pre-metal clean (to strip any oxide from the semiconductor surface) immediately prior to high vacuum deposition of the Schottky metallization. In this work, a controlled delay of 4 hours was introduced between the pre-metal clean and Schottky metal deposition to investigate its effects on the Schottky device parameters. The area of the Schottky diodes on n type GaAs was approximately 8.32 µm2. After finishing the process, the forward Schottky characteristics at multiple sites on each wafer were measured using a semiconductor parameter analyzer.

Results and Discussion

 Figure 1 shows the forward I-V characteristics of multiple devices on two wafers. The curves are labeled and color coded to indicate the treatment the wafers received (i.e. Delay versus No delay). It is evident that the characteristics of the devices without delay are more tightly distributed than the characteristics of the devices with delay.



 The ideality factors of the devices were calculated from the derivative of the plot ln(I) versus V at different currents. Figure 2 shows the ideality factors of multiple devices at different locations on the wafers as a function of the forward current. The increase of ideality factor with forward current is likely due to series resistance of the devices. The wide variation of ideality factor in devices with the 4 hour delay indicates a large variation in series resistance and surface states. For the devices without delay, the ideality factor is approximately 1.05 at currents below 1 µA. In contrast, the devices with delay exhibit ideality factors between 1.2 and 1.8 for the same currents. The ideality factors near 1.0 for the devices without delay indicate the dominant current transport mechanism is thermionic emission.

Fig. 1. I-V characteristics of Schottky diodes with and without delay between pre-metal clean and Schottky metal deposition.



An extrapolated linear fit of the I-V curve provided I0, which is 2.0×10-14 A (Figure 3a) for a device with delay. For a device without delay, I0 is 1.1×10-15 A (Figure 3b). The barrier heights were calculated using the Richardson constant of approximately 8.2 A/cm2-K2. Barrier heights of approximately 0.75 eV and 0.82 eV were observed for the devices with and without delay, respectively.

Fig. 2. Ideality factors at different currents for devices with and without metal deposition delay.

 The series resistance of a Schottky diode consists of three components i) resistance from the un-depleted epi-layer, ii) resistance from the contact layer, and iii) contact resistance. The following Cheung functions [1] were used to estimate Rs (series resistance), n (ideality factor) and φbn (barrier height).

 (1)

 (2)

 (3)

The plot of dV/d(ln(I)) versus I will be a straight line with slope Rs and Y intercept nKT/q. The plot of H(I) versus I will also be a straight line and the slope will provide a second estimate of Rs, which can be used to prove the consistency of this method. Furthermore, using the value of n found from the dV/d(ln(I)) versus I plot, φbn can be calculated.



Fig. 3a. Measured and calculated I-V characteristics of a device with delay.



Fig. 3b. Measured and calculated I-V characteristics of a device without delay.

 From the linear fit of dV/d(ln(I)) versus I of a device with the 4 hour delay, the ideality factor and Rs were found to be 1.34 and 80.4 Ohms, respectively. In contrast, for a device without delay, the ideality factor and Rs were found to be significantly lower at 1.1 and 31.4 Ohms, respectively. From the plot of H(I) versus I, the Rs was determined to be 81.4 Ohms and using n = 1.34, the φbn was calculated to be 0.74eV. This barrier height aligns very well with the value calculated from the reverse saturation current (Figure 3a) of the device with the 4 hour delay. Similarly, for the device without delay, Rs was calculated to be 37.5 Ohms. Using n = 1.11, the φbn was found to be 0.79 eV, which aligns well with the calculated value from the reverse saturation current (Figure 3b). Similar Rs values found from the plots of dV/d(ln(I)) versus I and H(I) versus I for devices with delay and without delay indicate the consistency of the Cheung functions.

 In order to justify the values obtained from the plot of Cheung functions, the forward I-V characteristics were calculated using similar values of n and Rs. Figures 3a and 3b show the calculated and experimental curves of the devices with and without delay, respectively. The pink I-V curve in Figure 3a was calculated using I0 = 2×10-14 A, n = 1.315, and Rs = 83 Ohms. The pink I-V curve in Figure 3b was calculated using I0 = 1.1×10-15 A, n = 1.07, and Rs = 34 Ohms. A good agreement between the calculated and experimental curves indicates that the values of n and Rs obtained from Cheung functions are justified. The lower series resistance (~34 Ohms), lower ideality factor (~1.07) and higher barrier height (~0.82 eV) indicate a higher quality interface for the devices without delay.

 A proposed model for the phenomena described above is based on natural oxidation of the exposed semiconductor surface that occurs during the delay between the pre-metal clean and the Schottky metal deposition. The oxide is presumed to be non-uniform and of poor quality, resulting in undesirable effects like a lower barrier height, an additional series resistance, and an increased and more variable ideality factor.

Conclusions

 Delays between pre-metal clean and Schottky metal deposition play an important role in fabricating high quality Schottky devices. The devices with delay revealed a large variation in series resistance and ideality factor. The devices without delay exhibited more tightly distributed I-V characteristics, lower ideality factor, lower series resistance and higher barrier height.

Acknowledgements

 The authors wish to acknowledge Ed Burke for his continuous support and encouragement.

References

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