**Exploring the Challenges of Gallium Arsenide Plasma Dicing**

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**Abstract**

**Plasma dicing of silicon wafers is beginning to move from pilot scale into mainstream production. Attention is now focussing on other market sectors which may benefit from a similar dicing approach. The fragility of GaAs wafers leads to issues (such as wafer breakages, damage to die edges) during conventional wafer saw dicing. Although LASER techniques have been developed, they also have their own drawbacks – specifically sidewall quality. A systematic investigation of the current capabilities of plasma dicing of GaAs substrates has been performed, developing technology which is both practical and economically viable. Preliminary results show smooth vertical sidewalls of trenches suitable for dicing thinned GaAs substrates at etch rates up to 23μm min-1.**

INTRODUCTION

Replacement of conventional saw dicing with plasma dicing of silicon wafers delivers improved sidewall quality without chipping and micro-cracks, leading to higher yields and improved die strength. Additionally narrower dicing lanes are possible compared to saw dicing allowing potential increases in die per wafer at no frontline cost [1]. Plasma dicing of silicon was the first market sector to be developed, as silicon represents the largest market sector in terms of substrate numbers. In addition, deep silicon etching using the well-established ‘Bosch process’ [2] time multiplexed silicon etch technique gives an extensive library of fast, vertical etches with good control that could be repurposed for silicon wafer dicing.

Gallium Arsenide (GaAs) is another obvious candidate for the next step in plasma dicing; its fragile nature leads to significant yield loss in wafer sawing processes. This is normally combatted by using low saw travel speeds to reduce pressure applied by the blade. However, since GaAs wafers are commonly used at small die sizes, this leads to very low wafer throughput [3, 4]. The process also produces large amounts of waste water contaminated with Arsenic that requires expensive management [5]. In contrast to silicon plasma etching, deep GaAs etching is not as technologically advanced. For instance, there is no equivalent to the Bosch process or advanced library of etch recipes for this type of feature in GaAs materials. Thus, this work presents the development of high rate trench etch processes for GaAs.

INVESTIGATION

A specially commissioned plasma etch module has been designed, which is capable of handling much higher power and gas flows than a typical ICP tool used for GaAs etching. The module also has modifications to handle dicing frames with additional measures to withstand the resulting high energy, chlorine plasma generated. The module is attached to a single wafer manual load lock for testing but is fully compatible with a production orientated automated handler.

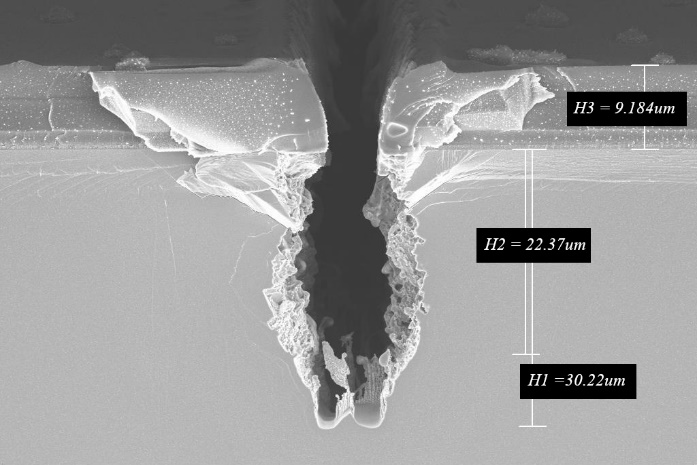
TABLE I

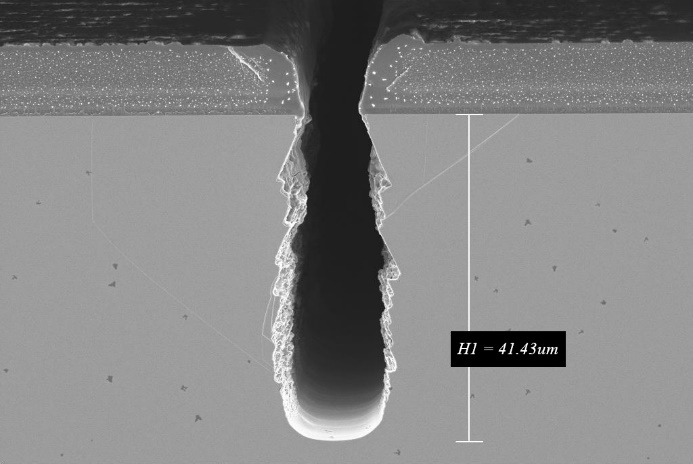
Explored tool parameter range

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Temp range (°C)** | **Coil power range (W)** | | **Platen power range (W)** | | **Pressure range**  **(mT)** |
| -10🡪10 | 2200🡪3500 | | 150🡪300 | | 15🡪50 |
| **BCl3 range (Sccm)** | | **N2 range (Sccm)** | | **Cl2 range (Sccm)** | |
| 100🡪300 | | 0🡪50 | | 600🡪850 | |

Preliminary testing using a non-optimised high flow and high power regime showed no visible signs of degradation of either polyolefin based dicing tape or the PEEK wafer frames. Because traditional GaAs etches derive their sidewall passivation from polymer contributions of eroded mask material, a comparison test was performed.

This test compared a bare exposed dicing tape surface to a mask polymer coated tape using the same non optimised recipe (Figure 1). This showed evidence of reduced sidewall passivation with the tape exposed surface. Consequently, all subsequent tests were carried out with the dicing tape surface outside of the etch samples covered by mask coating.





(b)

Fig 1: Electron micrographs of etched GaAs wafer with non optimised recipe (a) - recipe with dicing tape surface exposed to plasma, and (b) – Tape surrounding sample covered with mask polymer

Now that the experimental approach was established, a screening experiment matrix was performed based on an ICP GaAs via etch recipe. The assumption was made that overall etch rate would be critical to the success of the project, with the highest etch rate considered likely to be achieved at higher gas flows and coil powers. Experience drawn from GaAs via etching also suggests that faster etch rates are achieved at higher pressures, although sidewall quality can suffer under these conditions. Thus, a baseline process similar to the standard ICP GaAs via etch was used with pressure, coil power and gas flow parameters increased from this point. Evaluation of the larger operating window enabled by the new chamber was therefore explored. Design and results analysis was performed using Minitab18 software.

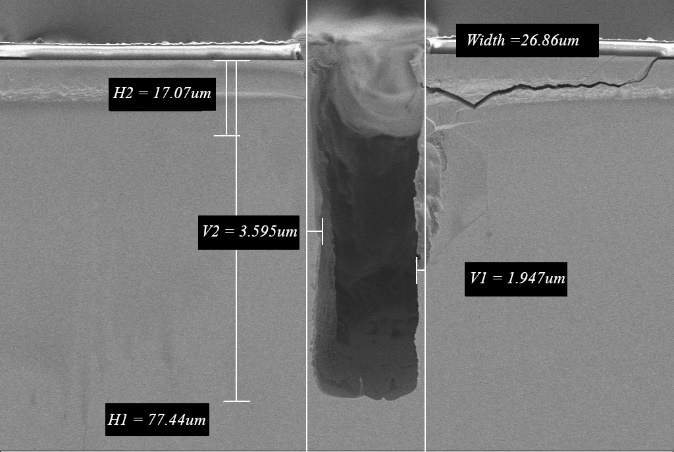
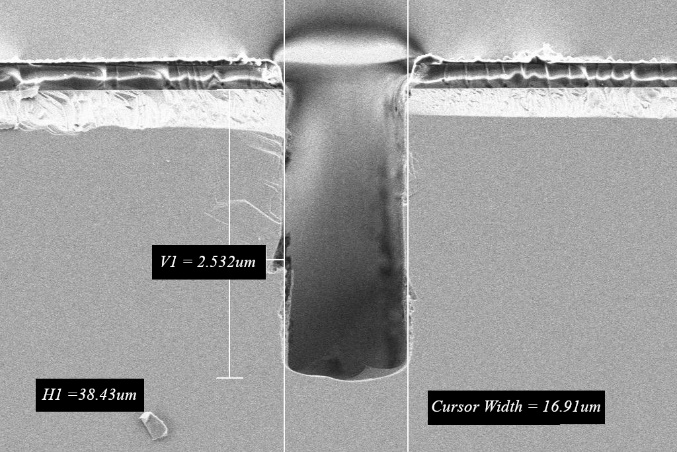
(b)

TABLE II

Initial screening matrix

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Run**  **Order** | **Temp**  **(°C)** | **Coil**  **power**  **(W)** | **Platen**  **power**  **(W)** | **Pressure**  **(mT)** | **BCl3**  **(Sccm)** | **N2**  **(Sccm)** | **Cl2**  **(Sccm)** |
| 1 | - | - | + | - | + | + | + |
| 2 | - | + | - | + | - | - | + |
| 3 | + | - | + | + | + | - | - |
| 4 | + | + | - | - | + | - | - |
| 5 | - | - | - | + | + | + | - |
| 6  (a) | + | - | + | - | - | - | + |
| 7 | + | - | - | + | - | + | + |
| 8 | + | + | - | - | + | + | + |
| 9 | + | + | + | + | - | + | - |
| 10 | - | + | + | - | - | + | - |
| 11 | - | + | + | + | + | - | + |
| 12 | - | - | - | - | - | - | - |

Two of the experimental process windows tested gave vertical etch profiles (Figure 2) at etch rates up to 23μm min-1 (30μm trench feature) - significantly faster than a typical deep GaAs etch process [6]. Some compromise in etch rate is expected as the process window is tuned for optimum sidewall quality.

(a)

Fig 2: Electron micrograph of etched GaAs wafer (a) (PR Mask) – 15.5μm min-1and (b) (PR Mask) – 23.5μm min-1

The conditions that yielded the fastest etch rate were selected for further optimisation using a focussed DOE

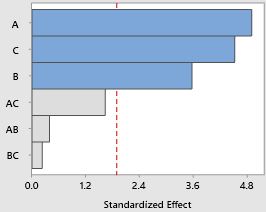
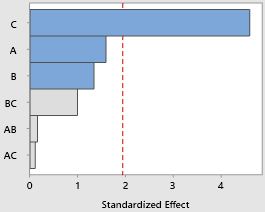
TABLE III

Detailed DOE

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Run**  **Order** | **Std Order** | **Factor A**  **Pressure**  **(mT)** | **Factor B**  **Platen**  **power**  **(W)** | **Factor C**  **BCl3**  **(Sccm)** |
| 1 | 8 | + | + | + |
| 2 | 1 | - | - | - |
| 3 | 9 | 0 | 0 | 0 |
| 4 | 7 | - | + | + |
| 5 | 2 | + | - | - |
| 6 | 4 | + | + | - |
| 7 | 5 | - | - | + |
| 8 | 3 | - | + | - |
| 9 | 11 | 0 | 0 | 0 |
| 10 | 10 | 0 | 0 | 0 |
| 11 | 6 | + | - | + |

This experiment yields the following Pareto charts;

(a)Etch Rate (b)Quality



(c)Peak temperature

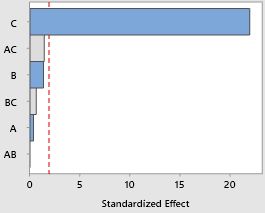


Fig 3: Pareto charts showing the significance of various process factors against process response, dotted line show the boundary level of statistical significance

Etch rate is clearly dominated by BCl3 flow and the availability of Chlorine reaching the etch front. Etch quality has been defined as the maximum variation, from vertical, of any point in the trench. This is measured by drawing a vertical line from the mask edge downwards and measure the distance from the die sidewall to this line. The most critical factors identified as impacting sidewall quality are a reduction in pressure, high BCl3 flows and platen bias. The final factor investigated is peak temperature, as measured by SentinelTM, SPTS’s remote pyrometer system[7]; the dominant parameter here is BCl3 flow. These results show clear responses within this space but also show conflicting considerations. At the optimum recommended high flow high/high bias window the temperature of the wafer is hard to control. It has also been shown that attempting to extend these process trends even further leads to potential thermal tape failures[8]. Figure 4 shows the condition from the DOE suggested as optimum within the tested space. This has etched a 30μm width trench to a depth of 88.7μm at a rate of 17.7μm min-1. The high bias and BCl3 concentration produce increased mask erosion rates and although some photoresist (PR) pull back damage is visible at the top, this is correctable with thicker PR coverage. The small amount of grass seen on the base of the feature is probably related to initial surface cleanliness. Use of pre-etch descum step may remove this grass.

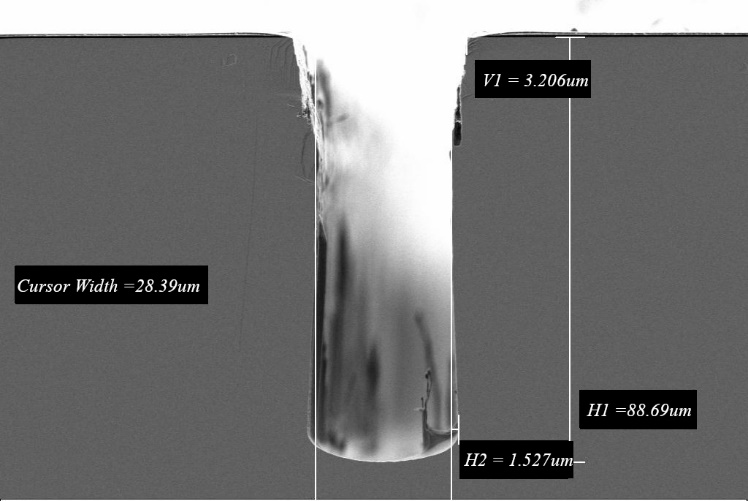


Fig4: Electron Micrograph of Run 4 – suggested by DOE results as optimum condition.

Analysis of results from different trench widths allows evaluation of how Critical Dimension (CD) can affect etch rate. The resulting curve, [Fig5], demonstrates the reduction in effective etch rate with smaller CD. This can be considered analogous to the relationship with aspect ratio. Since mask etch rate remains constant while etch rate decreases with CD, the thickness of the wafer will be the limiting factor when considering the minimum CD for dicing trenches

Fig5: plot of CD against feature etch rate for the same process

Experiments have also been performed using water soluble coatings as the etch mask instead of photoresist. These coatings are designed for surface protection during LASER grooving of dielectric and metal layers in the dicing lanes, removal of such layers may be required for some integration schemes. The water soluble coatings have the advantage that no chemicals are required for their removal post process (only water) and therefore there are no compatibility issues between the stripper and the dicing tape or adhesive layer.

It has been found that the quality of the LASER groove and, in particular, the profile angle of the resulting mask has a critical effect on achievable etch quality. If the grooving process results in a tapered mask angle, there is a significant risk of mask pull back leading to top damage and deflection of incident ions resulting in sidewall bow and undercut [6]. Despite similar selectivity to photoresists such coatings do produce a significant variation in the etch process due to the different chemical nature of the material, producing different polymerisation than a standard PR resin when used in the same etch recipe. Etch recipes therefore require tuning to account for the type of coating used.

CONCLUSIONS

The work demonstrates the feasibility of vertical GaAs trench etches, at a rate fast enough to be economically viable for plasma dicing of thinned GaAs substrates. A significant amount of characterisation is currently being performed to optimise the sidewall quality at an initial target etch depth of 100μm. Additional testing is needed to determine the practical depth limitations pertaining to etching of thicker GaAs wafers. It is also anticipated that the techniques developed will be applicable to improve Cost of Ownership (CoO) in GaAs TWV etching.

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REFERENCES

[1] R. Barnett, O. Ansell, and D. Thomas, "Considerations and benefits of plasma etch based wafer dicing," in *2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013)*, pp. 569-574.2013

[2] F. Laermer and A. Schilp, "Method of anisotropically etching silicon," 1996.

[3] M. Notarianni, R. Westerman, T. Lazerand, and C. Johnson, "Plasma Dicing On Tape for GaAs based devices," presented at the CS Mantech 2017.

[4] R. Fox, "Dicing improvements: Yield enhancement, Throughput increase and Die Size reduction in MA-Com's GaAS Fab," *CS MAntech,* 2001.

[5] M. Cooke, "Scribe and dice," *III-Vs Review,* vol. 19, no. 4, pp. 20-24, 2006.

[6] D. S. Rawal, V. R. Agarwal, H. S. Sharma, B. K. Sehgal, R. Muralidharan, and H. K. Malik, "Study of inductively coupled Cl2/BCl3 plasma process for high etch rate selective etching of via-holes in GaAs," *Vacuum,* vol. 85, no. 3, pp. 452-457, 2010.

[7] R. Barnett, O. Ansell, M. Hanicenic, and J. Hopkins, "Novel end-point solution for improvement in die strength and yields with plasma dicing after grind in volume production," in *2017 IEEE 19th Electronics Packaging Technology Conference (EPTC)*, pp. 1-4,2017

[8] S. Fulton, O. Ansell, J. Hopkins, T. Umemoto, and T. Nishida, "Dicing Tape Performance in a Plasma Dicing Environment," in *2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)*, pp. 229-236, 2018.

ACRONYMS

PR: Photoresist

GaAs: Gallium Arsenide

TWV: Through Wafer Via

DOE: Design of Experiment

CoO: Cost of Ownership

CD: Critical Dimension