**100nm, Three-Dimensional T-Gate for SLCFET Amplifiers**

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## **Keywords: GaN, Amplifier, MMIC, Fabrication, T-gate**

## **Abstract**

**This report describes the first demonstration of a 100nm T-gate for the Superlattice Castellation Field Effect Transistor (SLCFET) amplifier. The SLCFET amplifier device utilizes a superlattice of GaN/AlGaN channels, which enables a high charge density and low source resistance. A three-dimensional T-gate structure provides electrostatic control of the channels while maintaining high gain. Improvements to the T-gate process have allowed for the scaling of the gate down to 100nm while maintaining excellent gate control, with an on to off current ratio exceeding 107. This gate scaling allows the device to reach FT / FMAX of 70/110 GHz with full passivation to maintain compatibility with the productionized SLCFET switch process.**

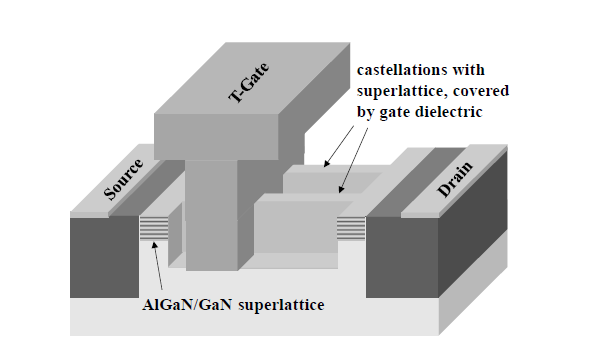


Fig. 1. Perspective view of SLCFET amplifier device structure. This structure combines a superlattice epitaxial structure with a three-dimensional T-gate to allow for electrostatic control of epitaxial channels.

## Introduction

The SLCFET technology has a proven and mature world-class switch with a switch figure of merit FCO of >1.8 THz [1-3], while also showing great potential as an amplifier [4,5]. The SLCFET devices utilizes a superlattice of GaN/AlGaN two-dimensional electron gas (2DEG) channels that are controlled by a three dimensional gate structure. The superlattice provides low parasitic resistances and a low knee-voltage, both of which are critical to achieving high power added efficiency [5]. The structure of the SLCFET amplifier device is shown in Figure 1. This paper reports advancements made to the scaling of the SLCFET amplifier 3D T-gate and the first demonstration of devices with a nominal stem length of 100nm.

## Gate Length Scaling

In order to improve amplifier performance beyond that of the baseline device, gate length scaling was identified as a key process improvement task as this can increase key amplifier metrics.

The gate length of an amplifier is inversely proportional the transconductance (gm) as shown in equation 1.

Eqn. 1

Unity current gain, FT is proportional to transconductance and therefore inverse gate length

Eqn. 2

Unity power, FMAX, is proportional to and therefore inverse gate length

Eqn. 3

## 100nm T-Gate Development

Previous demonstrations used a trilayer resist process to create T-gates on the SLCFET amplifier devices. During this process, a wafers is coated with three resists and then the stem and hat patterns are written with electron beam lithography at different doses to expose different layers of the resist stack and developed together to form the T-gate structure outline. This resist pattern is then metallized to form the T-gate. This process was sufficient to fabricate T-gates for short gate lengths on planar surfaces, which is shown as a cross section in Figure 2a. For the SLCFET structure, resist pools in the trench of the 3D castellated structure, as shown in Figure 2b. This created a processing challenge for SLCFET amplifiers, as the resist is significantly thicker than it would be on a planar surface. The thicker resist could be cleared with an increased electron beam dose and this proved sufficient for longer gate lengths (>175nm), but as processed development efforts moved to reducing the gate lengths, the dose necessary to clear the resist increased the critical dimensions of the gate, thus counteracting the process improvements. If the gate was resolved at 100nm, the baseline process was unable to clear the stem opening into the topography of the SLCFET device, leading to poor metallization and gate control, which counteracted any possible improvements to Gm.



Fig.3. a) EDS mapping of castellation trenches comparing gate metallization achieved using our baseline process and b) similar analysis of the new 100nm T-gate process. The 100nm process shows a significant improvement in gate metallization compared to the baseline.

A new three-dimensional T-gate fabrication process was developed that uses a sacrificial process to define the gate stem dimension through the entire castellation trench. This process maintains the stem length dimension through metal deposition, and has achieved the first demonstration of 100nm T-gates that are fully defined into the 3D structure of the SLCFET device. Figure 3 shows an elemental mapping using Electron Dispersive Spectroscopy (EDS), which highlights the metallization of T-gates made with the former baseline process and the new 100nm T-gate process**.** In the baseline process, shown in Figure 3a, the gate metal only consistently reaches about halfway into the castellation trench, which leads to poor control of the lower channels. The improved 100nm T-gate process, shown in in Figure 3b, demonstrates successful metallization to the bottom of the castellation trench.





Fig. 2. a) Cartoon resist cross of a T-gate pattern made using a trilayer resist process on a planar surface, such as a planar GaN HEMT, and b) cross section of the same profile on SLCFET. The 3D geometry of the SLCFET castellation causes resist to pool inside the trench, making it challenging to fully expose and develop the resist to the bottom of the trench.

Figure 4 shows the ID-VG transfer characteristics of the first 100nm SLCFET T-gate devices plotted on a logarithmic scale. In this test the gate voltage was swept from -14V to 1V and VDS held constant at .1V. In this plot it can be seen that the 100nm T-gate demonstrates an on to off state current ratio greater than 107. This is a major improvement over the devices fabricated with the baseline process targeted at 130nm nominal gate length. The baseline devices had poor gate control as exhibited by the on to off ratio of <101. This demonstrates that the 100nm T-gates created with the new process provide excellent gate control and indicates the compatibility of the process with creating a short gate length amplifier.



Fig. 4. ID-VG transfer curves for smallest T-gate devices achieved using the baseline and new 100nm T-gate process. The baseline process demonstrates minimal gate control with an on/off current ratio of <101 at nominal 130nm gate length while the new process demonstrates an on/off current ration >107 at a nominal 100nm gate length

## Results of RF Characterization of 100nm T-Gates



Fig. 6. Comparison of FT and FMAX between 150nm and 100nm gate length amplifiers which were both fabricated with the new T-gate process. The 100nm T-gate demonstrates a higher FT than the 150nm T-gate confirming the benefits of gate length scaling.

Devices fabricated with the 100nm T-gate process were small signal tested with a PNAX to determine the impact of the gate length scaling on previously stated amplifier metrics. During this testing, small signal gain was measured while the bias was swept on the gate to find the peak Ft/Fmax for the device at a constant drain bias. The FT and FMAX were extracted and are plotted in Figure 5, which shows a comparison of parameters between the baseline T-gate process and the new T-gate process. It is clear from this plot that moving from the baseline to the new T-gate process shows a significant improvement in performance, with FT increasing from 55 to 70GHz and FMAX increasing from 87 to 110GHz.



Fig. 5. Comparison of FT and FMAX between the baseline SLCFET amplifier process, shown in black and the new T-gate process, shown in red. The new process clearly demonstrates superior amplifier characteristics compared to the previous baseline.

In order to look directly at the impact of gate length scaling, devices were fabricated at different gate lengths utilizing the new T-gate process. The devices for this comparison were fabricated simultaneously on the same wafer and were identical with the exception of the T-gate dimensions. By doing this direct comparison, it is possible to isolate the gate length scaling from other processing factors to get the clearest view of device changes. In the data shown in Figure 6, the 100nm T-gate shows a FT of 70 GHz, while the 150nm T-gate reaches a maximum FT of approximately 60 GHz, indicating that gate length scaling had the intended impact on device performance.

It should be noted on that while the gate length scaling improves FT that a similar improvement in FMAX is not observed between the new process devices. This is due to FMAX being limited primarily by gate resistance. As the stem of the T-gate is scaled shorter, the gate resistance is expected to increase. This can be appropriately counteracted by scaling the T-gate hat larger, which is a focus for future work in order to improve the device FMAX.

## Comparison of 100nm T-Gate with Previous SLCFET Amplifiers

Several iterations of the SLCFET amplifier have been created so it is of use to compare the previous iterations and improvements made over time, which are shown in Table 1.

## Table i

## Comparison of RF Characteristic From Iterations of the SLCFET Amplifier

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Reference | T-gate process, nominal length | FT (GHz) | FMAX (GHz) | Fully Passivated |
| Chang, et al [4] | POR, 200nm | 47 | 124 | No |
| Nagamatsu, et al [5] | POR, 175nm | 76 | 130 | No |
| This work | POR, 175nm | 55 | 87 | Yes |
| New, 100nm | 70 | 110 | Yes |

The original iteration of the SLCFET amplifier demonstrated a FT / FMAX of 47/124 GHz. Through processing improvements, an amplifier was demonstrated with a FT/ FMAX of 76/136 GHz. While these processing improvements were being implemented on the amplifier, it was determined that the SLCFET switch required additional passivation to reach reliability targets. The ultimate goal of this amplifier device is to maintain full compatibility with the SLCFET switch process to enable integration of the technologies for TR MMIC applications, so this additional passivation was implemented into the third iteration of the device. The presence of the additional passivation increases the gate to source and gate to drain capacitances, CGS and CGD, which in turn lowered the FT and FMAX to 55 GHz and 87 GHz respectively. By scaling the gate length with the 100nm T-gate process, the transconductance increased which enabled the amplifier to improve to the previously stated Ft/Fmax of 70GHz/110GHz.

## Conclusions

The first 100nm SLCFET T-gate was demonstrated using a newly designed process, which drastically improves the metallization into the 3D castellation structure leading to an increase in gate control and the resultant transconductance. RF characterization of the devices showed an improvement in FT /FMAX from 55/87 GHz on the best devices fabricated with the baseline process to 70/110 GHz on the new 100nm T-gates. Comparing T-gates fabricated with the new process at different gate length confirmed that gate length scaling does improve FT irrespective of the process, which aligns with the theoretical expectations for gate scaling.

## Acknowledgements

The authors would like to thank the GaAs/GaN foundry and testing teams for their hard work to process and characterize the wafers use in this work.

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Acronyms

SLCFET: Superlattice Castellated Field Effect Transistor

EDS: Electron Dispersive Spectroscopy