**Wet-etching Process Problem Identification in Type-II InP DHBT for 5G Power Application**

Yu-Ting Peng, Xin Yu, Milton Feng

Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign,

Holonyak Micro and Nanotechnology Laboratory, 208 North Wright Street, Urbana, IL 61801

Email: [ypeng14@illinois.edu](mailto:ypeng14@illinois.edu)

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## **ABSTRACT**

Wet-etching issues in type-II DHBT process fabricated by standard triple-mesa wet-etching have been identified and reported in this paper. For comparison, devices fabricated by hybrid-etching with incorporation of inductively-coupled-plasma (ICP) are also present. With better uniformity and yield, hybrid-etching process can potentially lead to a more reliable and reproducible process for 5G power amplifier application.

## Introduction

Type-II InP based double heterojunction bipolar transistor (DHBT) has been widely deployed in mixed signal integrated circuit and radio frequency (RF) instruments by Agilent since 2005, when the first reliable demonstration of AlGaAsSb/InP DHBTs with and greater than 200 GHz [1,2]. Compared with type-I DHBTs, type-II DHBTs have more favorable base-collector (BC) junction to eliminate the current blocking effects and base-push-out in type-I DHBTs [3]. However, current blocking at base-emitter (BE) junction makes type-II DHBTs inherently have lower current gain, which can be further improved by incorporating a type-I base-emitter junction with a type-II base-collector junction (Type-I/II DHBTs) to facilitate the hot electron injection from emitter to base [3,4]. In 2011, the remarkable results of and greater than 400 GHz with = 4.2 V have been demonstrated on UIUC fabricated type-I/II DHBTs. The record performance of /= 480/620 GHz with = 6.3 V in type-II DHBTs was reported by H. Xu in 2014 [5].

For sub-micron HBT process, wet-etching and ICP reactive ion etching process are both widely implemented. Particularly speaking, ICP etching process provides better uniformity and controllability over wet-etching process in mesa formation. However, utilizing plasma such as CH4/H2 can cause severe hydrogen passivation effect on carbon-doped base layer, which has been a fatal issue in device performance [6]. Several studies have been switched to BCl3/Cl2 based dry etching in order to avoid this issue, however, elevated substrate temperature along with low ICP power were found out to be necessary to minimize the damage on device surface and sidewalls. The etching rate in BCl3/Cl2 based ICP etching is also slower due to the non-volatility of the indium-chloride byproduct [7]. In order to develop a uniform and yieldable DHBT process for 5G power application, a comprehensive study of different process techniques is essential.

While most of the previous study has been focused on the development of high-speed type-II InP DHBT for mixed signal circuits, less attention has been paid to the 5G millimeter-wave power amplifier application and its process issues identification. In this paper, we report process development and issue identification of type-II InP DHBT process development for power application, which potentially would be beneficial to the performance improvement of devices.

Epitaxial Structure

The epitaxial layer for this study was grown on semi-insulating InP substrate by molecular beam epitaxy (MBE). The layer structure of the device is shown in Table I. The structure consists of a 450 nm InP to achieve higher breakdown voltage, a 40 nm carbon-doped GaAsSb grading base to accelerate the electron transport via quasi-electric fields to reduce the base transit time and an AlInP/InP graded emitter to create electron launcher at Base-Emitter (BE) interface for hot electron injection.

Device Fabrication

Devices with various emitter lengths and widths were fabricated first with acid based etching solution with emitter metal contact defined by JEOL-6000FS/E electron beam lithography. The etching time is controlled to form 100 nm undercut to prevent the BE short from self-aligned base

Table I. Layer structures of Type-II GaAsSb/InP DHBT

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Layer** | **Description** | **Material** | **Composition** | **Thickness (nm)** | **Dopant** |
| 9 | Cap | InxGa1-xAs | x = 0.53 | 100 | Si |
| 8 | Grading Layer | InxAlyGa1-x-yAs | x = 0.52 y = 0.19 | 35 | Si |
| 7 | Emitter | InP | - | 5 | Si |
| 6 | Emitter Launcher | AlxIn1-xP | x = 0.1 → 0 | 15 | Si |
| 5 | Base | GaAs1-xSbx | x = 0.39 → 0.49 | 40 | C |
| 4 | Collector | InP | - | 450 | Si |
| 3 | Sub-collector | InxGa1-xAs | x = 0.52 | 10 | Si |
| 2 | Sub-collector | InP | - | 400 | Si |
| 1 | Etch Stop | InxAl1-xAs | x = 0.52 | 20 |  |
|  | Substrate | InP | - | - |  |

metal. A thin layer of SiNx is then deposited using PECVD and etched back using RIE to form SiNx hard mask for the following Base-Collector (BC) etch in two approaches: (i) 1:1 diluted hydrochloric acid (HCL) wet-etching (ii) hybrid-etching with CH4/H2 based ICP and hydrochloric acid treatment. Two devices with same emitter width will be compared side by side for further process improvement analysis. After collector metal contact deposition, isolation etch will be performed before BCB planarization to reduce extrinsic parasitic [8]. For experimental purposes, wet and hybrid isolation etching will both be conducted to achieve profile comparison and analysis. A scanning electron microscopy (SEM) image of a device after collector metal and post metal deposition is shown in Fig. 1.

Fig. 1. The top view of the fabricated HBT device after collector and post metal deposition.

Wet-etching process Issues and Results

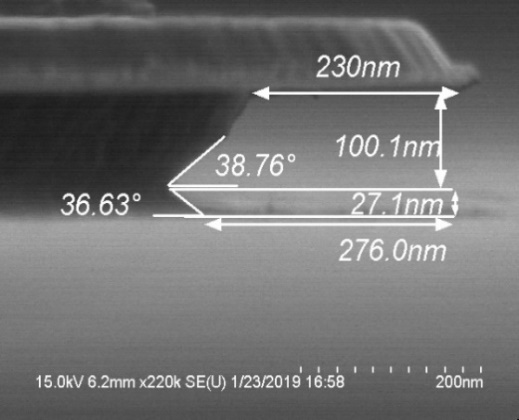
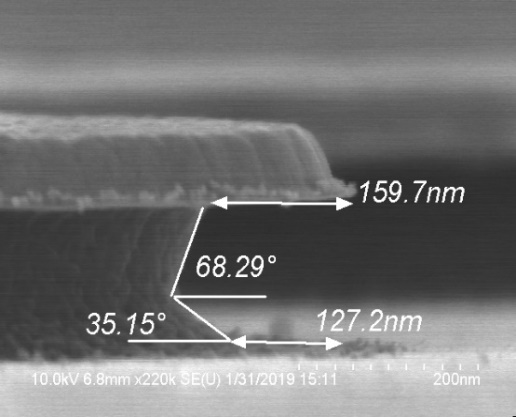
A) Base-Emitter (BE) Etching

Base-Emitter mesa formation was achieved by selectively etching away emitter cap and emitter layer with emitter metal acting as an etching mask. With the same etchant used, we

found out the lateral undercut can be significantly reduced to almost half (from 276 nm to 127 nm) by etching the sample

in dark for the first half of the etching duration. Less tilted etching profile (68.3 compared to 38.8) can also be observed on the sample etched in dark as shown in Fig. 2 (b). This strategy could potentially be helpful to minimize the BE resistance for self-aligned base metal contact. Moreover, the etching time can be precisely controlled to form narrower lateral undercut.

Fig. 2. Cross-sectional views of (a) sample A etched in uniform light and (b) sample B etched in dark.



**(a)**

**(b)**

B) Base-Collector (BC) Etching

(i) Wet-Etching

Followed by the emitter etch described in reference paper [5] and base metal deposition, the extrinsic parasitics are further minimized by depositing SiNx spacer on base metal to self-align Base-Collector (BC) etch. The 40 nm graded base layer can be selectively etched by either citric acid (C6H8O7) or any strong acid such as phosphoric based etchant [9], followed by diluted hydrochloric acid treatment to clear the 450 nm InP layer. However, the wet-etched profile eventually will reflect the crystal orientation of InP, as shown in Fig. 4 (a), which isotropically results into huge lateral undercut in the favorable crystal directions such as {111} plane. The lateral undercut was measured to be more than 400 nm each side, which results into higher chances of device collapse, especially for smaller devices with length comparable to the magnitude of the undercut. Such lateral undercut could be a yield-killer due to there would be no more BC mesa left after wet-etching was performed. Moreover, the etching rate near the edges of the pattern turned out to be significantly faster because multi-directional entries are available for etchants, leading to the fact that the etching rate is difficult to be controlled under such condition. Thinner collector layers can fundamentally result into less undercut profile at the expense of lower breakdown voltage, which is unfavorable for power application.

(ii) Hybrid-Etching

To maximize the remaining BC mesa after etching was performed, incorporating ICP dry etching has become a better approach. The etching process was first calibrated to optimize smooth and vertical sidewall profile with CH4/H2 plasma at 10 mTorr. Around 50 nm/min InP etching rate can be obtained at a power ratio of 1:2 (RIE to ICP). The etching profile detected by the laser endpoint detector is depicted in Fig. 3. The etching was stopped at the 3rd minimum consistently to land on the intended layer. Surface treatment dip was then performed after ICP dry etching was finished to clear the surface. Figure 4 shows the comparison between these two etching techniques. It is worth noted that ICP dry etching not only provides minimal undercut to the BC mesa but also achieves higher yield for devices with short length such as 2 um. By examining ten 2-um devices randomly, nine of the devices have intact mesas without experiencing huge lateral undercut, achieving a yield of 90% across the sample.



Fig. 3. Etching profile detected by the laser endpoint detector from CH4/H2 ICP etching process.

**(a)**

**(b)**





Fig. 4. BC mesa formed by (a) wet-etching process after SiNx spacer removal (b) hybrid-etching process before SiNx hard mask removal.

Isolation Etching

(i) Wet-Etching

The extrinsic basic contact is further minimized by performing isolated etch from the intrinsic device with photoresist etching mask, as shown in Fig. 5 (a). However, devices have found to suffer non-uniform etching during the intermediate status owing to the metal enhancement etching effect. The region with metal pad revealing will have a tendency of being etched faster than that without metal pad present. The etched surface will eventually become level at both sides after long duration of acid treatment, introducing huge lateral undercut on one side of the device as shown in Fig. 5 (b). The longer the etching, the greater the risk for metal post to collapse, which greatly affects the yield of the devices when it comes to device scaling.

(ii) Hybrid-Etching

Figure 6 shows the complete device after isolation etch with the aid of hybrid-etching. Lateral undercut can be introduced by further acid treatment from the straight sidewall profile achieved by CH4/H2 ICP dry etch. Without unevenly etched surface, the isolation profile provides better isolation from intrinsic devices as well as uniform results all over the sample.

**(b)**

**(a)**

A picture containing light, white

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A picture containing sitting, white, black, table

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Fig. 5. (a) Intermediate status during the isolation etch with photoresist coverage on the intrinsic region (b) Final status of isolation etch.

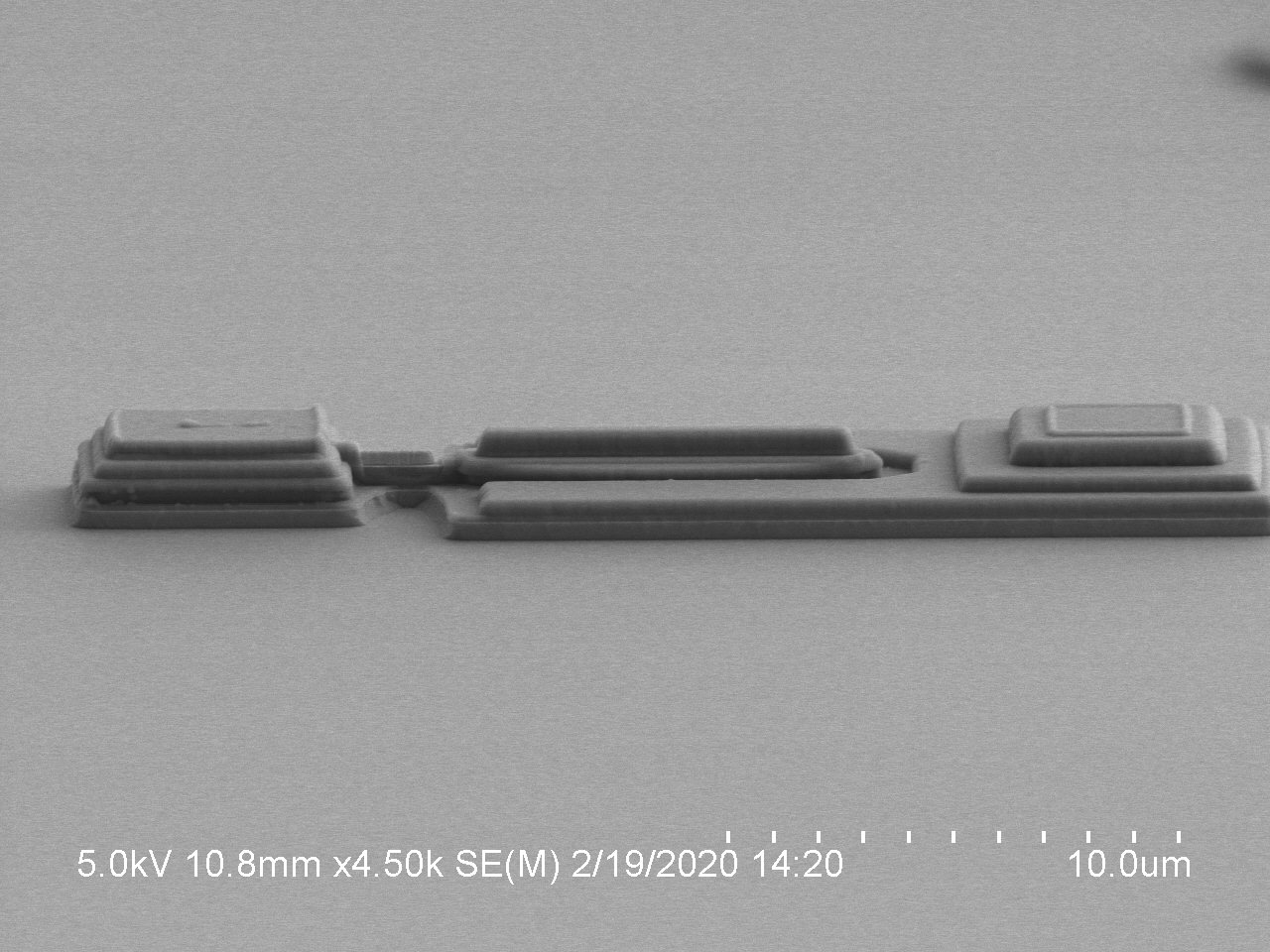


Fig. 6. Final status of isolation etches by hybrid-etching with CH4/H2 ICP dry etch technique.

Conclusion

Metal and light enhancement etching fundamentally have limited the wet-etching process from producing better uniformity and higher yield of devices. Hybrid-etching utilizing CH4/H2 ICP etching technique has been demonstrated to be preferable and reliable in BC and isolation etching without experiencing enormous lateral undercut. As the dimension of InP DHBT is scaled down, process development becomes critical and important to establish a reproducible process with high yield and uniformity.

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## Acronyms

DHBT: Double heterojunction bipolar transistor

: Breakdown voltage with base open

ICP: Inductively-coupled-plasma

RIE: Reactive-ion etching

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**(b)**

**(a)**