Recent development of vertical GaN planar-gate MOSFETs fabricated by Ion Implantation

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## **Abstract**

**We have demonstrated the vertical GaN planar-gate MOSFETs fabricated by an ion implantation process. The fabricated GaN vertical MOSFET shows a specific on-resistance of 2.78 mΩ cm2 and a breakdown voltage of 1200 V, by applying a Mg and N sequential implantation to improve the breakdown voltage of the pn-junction and** **the control of the MOS channel characteristics on the p-type ion implanted layer. Consequently,** **the vertical GaN planar-gate MOSFETs with high breakdown voltage and low on-resistance could be realized by ion implantation process. On the other hand, there are still many challenges for realizing practical GaN vertical MOSFETs, so continuous development is necessary.**

## Introduction

GaN has attracted attention as a semiconductor material for next-generation power switching devices. Vertical-type GaN devices with MOS gate driving are preferable for high-power switching applications. Due to recent advances in bulk GaN crystal growth [1], more studies are reporting vertical-type GaN devices with a breakdown voltage exceeding 1 kV on GaN substrates [2-4]. However, all these reports use an epitaxially grown p-type layer.

For practicality and reliability viewpoints, it is essential to form a p-type layer by ion-implantation (I/I). I/I requires a high-temperature activation heat treatment, however, heat treatment at 800 °C or higher decomposes GaN due to the very strong triple bond of N molecule that reduces the negative Gibbs free energy of the nitride component [5]. Consequently, p-type formation by I/I into GaN is extremely difficult.

The p-type characteristics of Mg I/I layer have been reported recently. For example, the PL spectrum shows that some of the implanted Mg atoms form acceptors because the observed acceptor-related UV luminescence is similar to that of epitaxially grown p-GaN layers [6]. The p-type hole conduction in the Mg-implanted GaN layer annealed at 1400 °C under a nitrogen pressure of 1 GPa was also demonstrated using the temperature dependence of the Hall effect [7].

To realize a vertical GaN planar-gate MOSFET fabricated by I/I, it is necessary to secure a high breakdown voltage of pn junction by improving the characteristics of the p-type I/I layer and control the MOS channel characteristics on the p-type I/I layer. In this talk, we will introduce recent development of the I/I process and demonstration of the vertical GaN planar-gate MOSFETs.

### Improvement of characteristics of p-type ion implantation layer

It has been reported that large complex defects formed by clustering of Ga vacancies and N vacancies introduced by Mg I/I remain after the activation heat treatment [8]. In addition, the emission peaks from deep levels due to N vacancy-related defects was confirmed from the PL spectrum [6]. These defects have been found to adversely affect the electrical properties of p-type I/I layers. Therefore, sequential N I/I into the Mg I/I layer has been investigated to reduce N vacancies [9].

To evaluate the breakdown voltage of the pn-junction, we fabricated a pn-diode by I/I [10]. A 10-μm-thick n-GaN layer was epitaxially grown by MOCVD on the n-type GaN (0001) substrate. The net donor concentration of the n-GaN epitaxial layer was around 1.5×1016 cm-3. Mg ions were selectively implanted on the n-GaN layer. The Mg ions were implanted with 10 to 240 keV and a total dose of 8.4×1013 cm-2 to obtain a 0.3-μm-thick box-profile of 1×1018 cm-3 with a p+ contact region of 2×1019 cm-3 near the surface. After Mg I/I, N I/I was carried out sequentially. N ions were implanted with 10 to 180 keV and a total dose of 9.9×1013 cm-2. In addition, samples without N sequential I/I were fabricated. After Mg and N I/I, the wafers were annealed at 1300 °C for 5 minutes in a N2 atmosphere at standard pressure with an AlN encapsulation cap to prevent GaN dissociation. After annealing, the AlN cap was chemically removed. AFM measurements in a 1-μm square area indicated that the typical RMS surface roughness of GaN after activation annealing was 0.25 nm. The anode electrode was composed of nickel and gold, while the cathode electrode was composed of titanium and aluminum.

In Fig.1, it is shown the reverse I-V characteristics of the pn-diodes fabricated by Mg I/I. Subsequent N I/I drastically suppresses the leakage current and increases the breakdown voltage. Using CV measurements, PL, and positron annihilation spectroscopy, we reported that N sequential I/I reduces hole traps due to N vacancies [11]. Therefore, the breakdown voltage improves due to the enhanced pn junction characteristics. Unfortunately, the forward characteristics of the fabricated pn-diodes and/or electrical properties of the Mg I/I layer itself have not yet to be evaluated since the p-type contact is not sufficiently improved and ohmic contact is not obtained. Consequently, evaluating the activation ratio of the Mg I/I layer is a future task.



Fig. 1. Reverse I-V characteristics of the fabricated GaN pn-diode [10]. Copyright (2019) The Japan Society of Applied Physics.

### Control of the MOS channel characteristics on p-type ion implanted layer



Fig. 2. The linear region *I*d-*V*g transfer characteristics of fabricated MOSFETs measured at *V*d = 0.5 V [13]. Copyright (2019) The Japan Society of Applied Physics.

For the applications of the GaN power devices, it is important to realize high channel mobility to differentiate from SiC devices. We reported that inversion-type MOSFET operation is possible on an epitaxially grown p-type GaN layer and the channel mobility of more than 100 cm2V-1 s-1 can be obtained [12]. For realizing a vertical-type devices, it is desirable to form MOS channel on a p-type I/I layer. Therefore, we investigated the control of channel characteristics on Mg I/I layer [13].

Mg ions were implanted on the n-GaN epitaxial layer grown by MOCVD on the n-GaN (0001) substrate. The donor concentration of n-GaN epitaxial layer is around 5×1015 cm-3. The implantation energy of Mg was set at 700 keV, and three samples with different implantation doses were fabricated. The Mg I/I dose was set to 4.2×1014, 1.4×1014 and 4.2×1013 cm-2, respectively. The source and drain regions were selectively formed by Si I/I. An activation annealing of Mg and Si was simultaneously performed at 1300 °C for 5 minutes in N2 atmosphere at standard pressure with an AlN encapsulation cap. Finally, the AlN cap was chemically removed. Then a plasma-CVD apparatus with TEOS gas deposited a 100-nm-thick SiO2 layer at 300 °C. Titanium and aluminum were used as the gate, source, and drain metal. Forming gas annealing was performed at 400 °C for 30 min. In order to clarify the MOS channel property, the long channel lateral MOSFETs with the channel length of 100 μm and the gate width of 100 μm were evaluated.

In Fig. 2, it is shown the *I*d-*V*g transfer characteristics measured at *V*d = 0.5 V. As the Mg dose increased, the threshold voltage (*V*th) increased and the drain current decreased, obviously. The *V*th is determined as a gate bias intercept of the linear extrapolation of *I*d. The *V*th were 9.2 V, 4.2 V, and 2.2 V on the Mg I/I layer with the Mg dose of 4.2×1014, 1.4×1014 and 4.2×1013 cm-2, respectively. It was shown that the *V*th can be controlled by Mg I/I dose.

In Fig. 3, it is shown the field effect mobility (**fe) curves calculated from the *I*d-*V*g characteristics. The **fe gradually increases by applying the gate bias and show a peak at certain gate voltage. By decreasing Mg dose, the maximum **fe increases, and the peak values are 53, 119 and 173 cm2V-1 s-1 on the Mg I/I layer with the Mg dose of 4.2×1014, 1.4×1014 and 4.2×1013 cm-2, respectively.

Therefore, the MOS channel characteristics can be controlled by Mg I/I dose and a high channel mobility of more than 100 cm2V-1 s-1 can be realized on p-type I/I layer.

## Vertical GaN planar-gate MOSFETs

We demonstrated the vertical GaN planar-gate MOSFETs with low on-resistance and high breakdown voltage by combining the improvement of the pn junction breakdown voltage by sequential N I/I and the control of the MOS channel characteristics on the p-type I/I layer [10].

In Fig. 4, it is shown a schematic images of the fabricated vertical GaN planar-gate MOSFETs by I/I process. A short cell pitch design of 5 μm was used to reduce the channel resistance. The designed size of the active region on the photomask was 91 μm x 40 μm. The designed channel length was 1 μm, the JFET length was 1 μm, and the source length was 2 μm. We adopted a single-layer electrode structure to avoid the complicated process of stacked electrodes. The source parasitic resistance of a single-layer electrode structure was large compared to the stacked electrode in vertical contact with the source implanted region because the source electrode of a single-layer electrode structure is in contact with the active region at a position besides the horizontal direction.



Fig. 3. The *V*g dependence of the field effect mobility obtained on different Mg ion implantation dose layers [13]. Copyright (2019) The Japan Society of Applied Physics.



Fig. 4. Schematic images of vertical GaN planar-gate MOSFETs with all ion implantation process. (a) plan view, (b) cross sectional image of active region.

Firstly, Mg ions were selectively implanted on the 10-μm-thick n-GaN layer grown by MOCVD on the n-type GaN (0001) substrates. The net donor concentration of the n-GaN epitaxial layer was around 1×1016 cm-3. Mg ions were implanted with 10 to 700 keV with a total dose of 6.5×1013 cm-2. The Mg concentration near the surface was adjusted to control *V*th to about 3 V. Additionally, increasing the Mg concentration in the deep region provided a sufficiently thick p-well region. Afterwards, N ions were implanted sequentially with 10 to 600 keV and a total dose of 6.7×1013 cm-2. Secondly, Si ions were selectively implanted into the source regions with 15 to 40 keV and a total dose of 1.9×1015 cm-2. Thirdly, O ions were selectively implanted into the JFET region with 10 to 700 keV and a total dose of 2.3×1013 cm-2 to reduce the JFET resistance.

After triple I/I, the wafers were annealed at 1300 °C for 5 minutes in a N2 atmosphere at standard pressure with AlN encapsulation cap. Finally, the AlN cap was chemically removed.

Then a plasma-CVD apparatus with TEOS gas deposited a 100-nm-thick SiO2 layer at 300 °C. Titanium and aluminum were used as the gate, source, and drain metal, while nickel was used as the body contact metal. Forming gas annealing was performed at 400 °C for 30 min.

In Fig. 5, it is shown the *I*d-*V*d output characteristics on fabricated GaN vertical MOSFET. The fabricated GaN vertical MOSFETs show normal MOS channel behaviors such as a suitable drain current control by the gate voltage, good ohmic contact, and a low gate leakage current (<1.0×10-3 A cm-2). In Fig. 6, it is shown the breakdown measurement of the fabricated GaN vertical MOSFET. The fabricated GaN vertical MOSFET catastrophically breaks down around 1200 V. The *V*th determined as a gate bias intercept of the linear extrapolation of *I*d was about 3 V. However, the threshold voltage of the subthreshold region was negative. Hence, the breakdown voltage was measured while applying -5 V to the gate electrode. The drain leakage current at 1000V is less than 1.0×10-3 A cm-2.

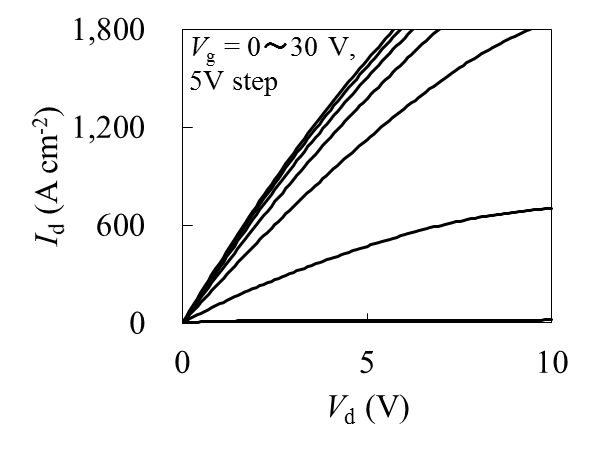


Fig. 5. *I*d-*V*d output characteristics of fabricated GaN MOSFET [10]. Copyright (2019) The Japan Society of Applied Physics.

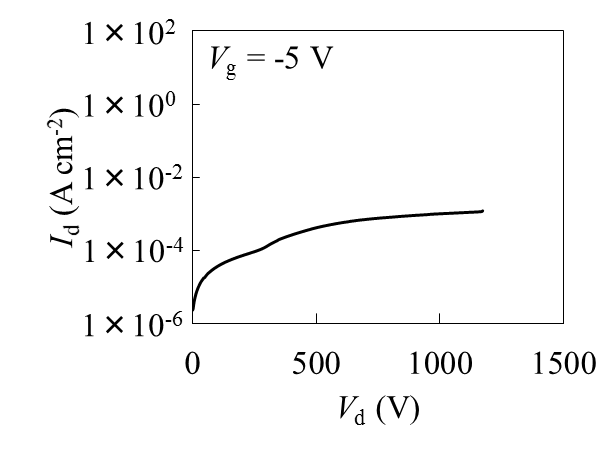


Fig. 6. *I*d-*V*d breakdown measurement of fabricated GaN MOSFET [10]. Copyright (2019) The Japan Society of Applied Physics.

The specific on-resistance determined from the slope of the *I*d-*V*d curve at *V*g = 30 V and *V*d = 1 V is 2.78 mΩ cm2. In consideration of the current spread in the drift layer, the area of ​​the active region used to calculate the specific on-resistance was set to 101 μm x 50 μm by adding the drift layer thickness (10 μm) to the designed size of the active region. As described above, we adopted a single-layer electrode structure in this demonstration, so the source parasitic resistance was large compared to the stacked electrode structure. The effective specific on-resistance of the active region was estimated to be about 1.4 mΩ cm2 by subtracted the source parasitic resistance. Therefore, the vertical GaN planar-gate MOSFETs with high breakdown voltage and low on-resistance could be realized by I/I process. For realizing practical GaN vertical MOSFETs, further process improvements are necessary, such as the investigation of the stacked electrode with a short cell pitch design and the p-type region with a high hole concentration for p-body contact.

## Conclusions

We have demonstrated the vertical GaN planar-gate MOSFETs with high breakdown voltage and low on-resistance fabricated by I/I process. We confirmed that good MOSFET characteristics were obtained by forming active regions such as p-well, source, and JFET region by I/I.

On the other hand, there are still many challenges for realizing practical GaN vertical MOSFETs such as further activation of I/I layer, improvement of hole conductivity, control of MOS channel characteristics, and reliability. Therefore, continuous development is necessary.

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Acronyms

GaN: Gallium Nitride

MOS: metal-oxide-semiconductor

FET: field effect transistor

PL: photoluminescence

UV: ultraviolet

MOCVD: metal organic chemical vapor deposition

RMS: root-mean-square

SiC: Silicon Carbide

TEOS: tetraethyl orthosilicate

JFET: junction FET