140 nm and 90 nm GaN MMIC Technology for Millimeter-wave Power Applications

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Fig. 1. DC transfer curves collected on 4x75 µm 140 nm devices fabricated on a single wafer with Vds = 10V. This figure includes 20 test sites collected across a 4-inch wafer.

**Abstract: This work describes an on-going effort to develop and mature a 140 nm GaN MMIC technology with a focus on efficient power amplification at frequencies ranging from DC to 50 GHz and a 90 nm technology targeted towards V- and W-band applications, and then release the technologies within a foundry process that is open to the DoD community.**

## Introduction

 GaN RF MMIC Technology has emerged as the leading solid-state technology for RF power technologies because it offers similar high-frequency performance as GaAs, but with >5X increased operating voltage, output power density, and linearity. Because of these performance advantages, GaN has begun to displace incumbent GaAs technologies for defense applications where high output power is critical to mission performance, including radar, electronic warfare, and seeker systems. Despite the tremendous progress made in GaN HEMT technology in the past decade, the majority of offerings from commercial foundries perform well at frequencies below 18 GHz, and there is limited access to more advanced technology nodes. A new generation of emerging threats demands that the DoD community have access to GaN technology that can provide efficient RF power at millimeter wave frequencies.

 BAE Systems is collaborating with AFRL/RY to develop 140 nm device technology that will offer best in class power performance at millimeter wave frequencies. The 140 nm process incorporates key features within AFRL’s devices that provide discriminating performance [1], combined with features of BAE Systems production MMIC process that provide industry-leading reliability and manufacturability [2]. At the conclusion of this program, we will mature the process to MRL 6, scale the process to 6-inch wafer diameter, and make the technology available to DoD suppliers through an open foundry service.

## 140 nm GaN Technology

 To support broadband electronic warfare (EW) and millimeter wave power applications, the 140 nm devices were designed without source-connected field plates to enhance the device gain and reduce parasitic drain to source capacitance. To improve the intrinsic performance of our device technology, we identified and incorporated key features of AFRL’s technology. These include the device geometry (with 140 nm gate length), epitaxial structure, and the surface passivation process. The key element to improving large-signal device performance was found to be the low-stress, high refractive index (n = 2.3) SiN surface passivation process that was adapted from AFRL/RY’s MMIC process.

 4x75 µm devices with 140 nm gate length were characterized for DC, small-signal, pulsed IV, and Ka-band load-pull performance. The DC transfer curves are shown in Figure 1. The devices achieve >1.3 A/mm maximum drain current (Imax) with gm greater than 370 mS/mm. Figure 2 shows the small signal gain at Vd = 10V, Id = 250 mA/mm. Performance was uniform with excellent PCM yields. Data shown in Figures 1 and 2 are collected from measurements of a single wafer (1 test site per reticle).



Fig. 2. Small signal measurements on 4x75 µm 140 nm CPW devices fabricated on a single wafer with Vds = 10V, Ids = 250 mA/mm. This figure includes 20 test sites collected across a 4-inch wafer. Median fT and fmax were 56 GHz and 120 GHz respectively.



Fig. 5. Cross-section of the device and epitaxial structure used in the 90 nm GaN technology.



Fig. 3. Load pull characteristics of a 140 nm device measured at 35 GHz with Vds = 28V, Ids = 100 mA/mm on a 4x65 µm CPW cell. The device had 4.1 W/mm output power with 41% PAE when matched for optimum PAE.

 Figure 3 shows the load pull characteristics at 35 GHz with the device matched for optimum efficiency. At quiescent bias of 28 V, the device exhibits output power of 4.1 W/mm with associated PAE of 41%. Measurements at Vd of 20 V showed output power of 3.1 W/mm with PAE of 45%. The test devices were CPW devices with no on-wafer pre-matching. Therefore, the measured performance was limited by the maximum reflection coefficient available on the tuners in our measurement setup (i.e. the optimum source and load impedances were outside of the tuning range). Active load pull measurements at frequency of 10 GHz with 2nd and 3rd harmonic turning produced 3 W/mm with 79% PAE at Vds of 20 V.



Fig. 4. Small-signal testing of our X-band evaluation circuit, fabricated using the 140 nm MMIC technology, showing high yield on 20 out of 20 test sites. The inset shows the layout of the test circuit.

 As part of the technology qualification, we are performing accelerated life testing using standard evaluation circuits. Our test vehicle, shown in Figure 4, is a single-stage X-band MMIC amplifier. Our testing of the first article wafer demonstrated good small-signal uniformity and yield, with 20 out of 20 test sites (one test site per reticle) passing the screening criteria. The reliability test is on-going and results will be reported at a later date.

 Future efforts will scale the technology from 4-inch to 6-inch wafer diameter, mature the process to TRL/MRL level of 6, develop PDKs in ADS and Microwave Office formats, and release the process to an open foundry service that is accessible to the DoD community at large.

## 90 nm GaN Technology

The 140 nm GaN process discussed in the previous section is expected to enable MMIC amplifiers at frequencies up to approximately 50 GHz. In the near future, we expect that new applications will increase the demand for MMICs that operate within the 50-75 GHz and 75-110 GHz frequency bands. Scaling transistor performance to higher frequencies involves (1) reduction of the gate length, (2) proportional reduction of the barrier layer (or effective oxide) thickness, and (3) lowering parasitic resistance.



Fig. 6. Measured small signal gain performance of advanced GaN 90 nm device on a 4x35 microstrip device with Vd = 10V and Id of 250 mA/mm. The fT/fmax were 120 GHz and 210 GHz respectively.



Fig. 8. Load pull characteristics measured at 35 GHz with Vds = 10V, Ids = 100 mA/mm on a 4x75 µm CPW device with 90 nm gate length. The device had 2.4 W/mm output power with 45% PAE, Gp of 9.5 dB, and 51% drain efficiency when matched for optimum PAE.



Fig. 7. Measured pulsed IV characteristics of a 2x50 µm 90 nm GaN device, measured with 200 ns pulse width and quiescent bias of Vg, Vd of 0V, 0V and -5V, 10V. Measured drain lag was less than 10%.

In this work, we iterated upon our past work on scaled devices that are targeted at higher frequency applications up to 110 GHz [3]. The epitaxial structure is based on vertically-scaled InAlGaN quaternary epitaxial layers, which are lattice-matched to GaN while offering very high sheet charge density with thin barrier layers due to the material’s high spontaneous polarization [4]. The material sheet resistance was very low at 250 ohm/sq, which offers both high maximum drain current as well as low access resistance.

Devices were fabricated with a Ge/Ti/Al/Ni/Au-based alloyed ohmic contact, which demonstrates a contact resistance of about 0.2 ohm-mm to this material system. Mesa isolation was performed using a Cl2-based ICP etch. T-gates with 90 nm gate length and low parasitic capacitance were fabricated using e-beam lithography, and devices were passivated with SiN. The wafers were processed through our backside process in order to fabricate devices in a microstrip configuration. Wafers were thinned to a thickness of 55 µm, and slot vias with dimensions of 15 µm x 25 µm were etched through the substrate. These BEOL processing steps are critical to realize high-performing devices with low source inductance and compact cell layout. The devices have 2.0 µm source-drain spacing with 0.5 µm gate-source spacing.

These devices demonstrated excellent DC and small signal performance, with Imax > 1.7 A/mm, and gm > 750 mS/mm. Gate-drain breakdown voltage (defined at 1 mA/mm of leakage current) was measured as about 27 V, which is sufficient for MMIC operation at 10 V. Device fT/fmax of 120/210 GHz were measured on 4x35 µm microstrip devices at bias of Vd = 10 V and Id = 250 mA/mm. The measurements were obtained with a probe-tip calibration and no de-embedding of pad parasitics. The high fmax of the device demonstrates the technology offers sufficient gain to obtain W-band power amplifiers using this process.

A key challenge in scaled device technologies is obtaining low current-collapse, which is a requirement for efficient large-signal device operation. Pulsed-IV measurements were conducted with quiescent bias of Vg = 0 V, Vd = 0 V, and compared with measurements taken at quiescent bias of Vg = -5 V, Vd = 10 V. The IV characteristics show very low current collapse, indicating that the surface condition and trap density within this material system is well controlled. Load pull measurements were conducted on 4x75 µm devices at 35 GHz with Vds = 10 V showed output power of 2.4 W/mm and PAE of 45%.

These represent preliminary results in this new technology, and we expect further improvement will be obtained through optimization of the process. In particular, future work will focus on improving the process to obtain higher breakdown voltage, as the present value is far below the theoretical value of GaN, and restricts the available output power density [5].

## Conclusions

 In conclusion, we have demonstrated preliminary results on our next generation GaN technologies at BAE Systems. The 140 nm GaN technology is a state of the art millimeter-wave power technology, which offers excellent power and efficiency for RF power amplifiers at frequencies up to 50 GHz. The 90 nm process is designed to extend the frequency range to 110 GHz in order to access the V and W bands. While attractive for higher frequency power amplifiers, this technology will also be attractive for high dynamic range millimeter-wave low noise amplifiers, and T/R MMICs that require both excellent PAE and low noise figure capabilities.

 Efforts to mature the technology to MRL 6, design demonstration MMICs, and scale our manufacturing process to 6-inch wafer diameter are ongoing, and will be reported in future work.

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Acronyms

MMIC: Monolithic Microwave Integrated Circuit

HEMT: High Electron Mobility Transistor

DoD: Department of Defense

AFRL: Air Force Research Laboratory

EW: Electronic Warfare

PAE: Power Added Efficiency

PDK: Process Design Kit

TRL: Technology Readiness Level

MRL: Manufacturing Readiness Level

CPW: Co-planar Waveguide

ICP: Inductively Coupled Plasma

BEOL: Back End Of Line