**Plasma Enhanced Atomic Layer Deposited Silicon Nitride on GaN MISCAPs with High Charge and Mobility**

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***Abstract***

*In this work fabrication of MISCAP structures was achieved on n-type gallium nitride using atomic layer deposited silicon nitride as the dielectric layer and sputtered ruthenium contacts. Preliminary values extracted from C-f data suggests very high capacitance densities up to 3.18 μF∙cm-2 and very high accumulation-mode field effect mobility, as high as 325 cm2V-1s-1 at a bias voltage of 2.5 V.*

**Introduction**



**Figure 1** - Fundamental challenges in manufacturing viable MISFET devices include creating sub 2nm dielectrics over a variety of surfaces.

Within power electronics and communications technology, gallium nitride has attracted attention for its strong theoretical switching properties summarized in its Baliga Figure of Merit, which is superior to other compound semiconductors such as gallium arsenide and silicon carbide. While considerable work has been done on GaN based HEMTs1, issues with interface states stemming from the absence of a good native insulator for GaN have limited channel mobilities and stymied the development of GaN MISFETs2. In order to achieve the superior off state performance3 and high gate voltage benefits1 of MISFET architecture, continued research is required.

A fabrication technique of interest in current microfabrication is atomic layer deposition. ALD has attracted considerable attention recently for the ability to form thin films with high conformality and uniformity, by-products of the self-limiting nature of the deposition reactions4. Uniformity is of great interest in metal-insulator-semiconductor technologies as these technologies benefit strongly from thin, high quality dielectric layers that can provide high capacitance and subsequently higher current densities when the device is turned on. Conformality is a deposition trait that lends itself to enabling more exotic device architectures, such as the vertical GaN fin transistors being developed by many groups5, which would be considerably more difficult to fabricate without the conformality of ALD.

Further to this even a simple MISFET structure (Figure 1) requires pinhole free dielectrics to be formed either on top of metal source drains or on heavily doped GaN. For this reason the focus of this study is shifted to low temperature growth ALD. By moving to lower temperatures the conformality of the film across a variety of surface conditions is enhanced. While considerably lower growth rates are present in this low temperature deposition, the low temperature coupled with tailored pulse time approach guarantees true ALD that provides consistent growth over a wide range of surface conditions.

**Fabrication Procedure**

MISCAPs were fabricated on n+ and n- GaN wafers (with respective doping densities of *ND* ≈ 1018 and *ND* ≈ 1016 cm-3) from Kyma, which were cleaned with piranha solution prior to fabrication. The SiN film was grown by PEALD at 100°C using tris(dimethylamino)silane (3DMAS) and forming gas (N2:H2) plasma in an ALD-150LX reactor from Kurt. J. Lesker. A proprietary pre-treatment was applied prior to ALD deposition. Through in-situ ellipsometry measurements, 0.013 nm/cycle deposition rates were observed. Film thicknesses were monitored *in-situ* using spectroscopic ellipsometry in an M2000DI spectroscopic ellipsometer from J. A. Woolam - wherein the SiN film data was fitted according to the Tauc-Lorentz model, indicating film thicknesses of 1.90 nm, 2.75 nm and 5.00 nm on the n- wafers, and 2 nm on the n+ wafer. Sputter deposition was used to fabricate the 80 nm thick ruthenium contacts. Ru is chosen because it has excellent diffusion barrier characteristics and has exhibited a high degree of inertness under many conditions.

While this is not within the normal true ALD rate of growth (closer to 0.1 nm/cycle should be expected for true ALD), what is guaranteed in this process is a full saturation of deposition and a minimization of pin holing in the film. Typical ALD films are not typically epitaxial or polycrystalline, but rather have an amorphous microstructure. The amorphous microstructure has a two-fold advantage in this application, the films are physically more dense, and the films have fewer conduction channels available for electron transport across the dielectric barrier. This leads to a true tunneling-limited current which is desirable for maximizing MISFET performance.



**Figure 2 -** The oxide stack on the GaN **(3)** is considered for analysis. The electrons form a channel at the boundary of the dielectric, semiconductor interface. It has an effective centroid thickness of de and contributes to the effective capacitance of the gate stack. The dielectric **(2)** and the native oxide **(1)** on top of the deposited dielectric contributes to the overall capacitance density and effective dielectric thickness.

Despite the high density of the SiN films, dangling bonds remain on the surface and a resulting native oxide film occurs on the surface of the SiN film (Figure 2). At these thicknesses this slight native oxide contributes to a significant alteration in the total capacitance observed, reducing it in a manner described below.

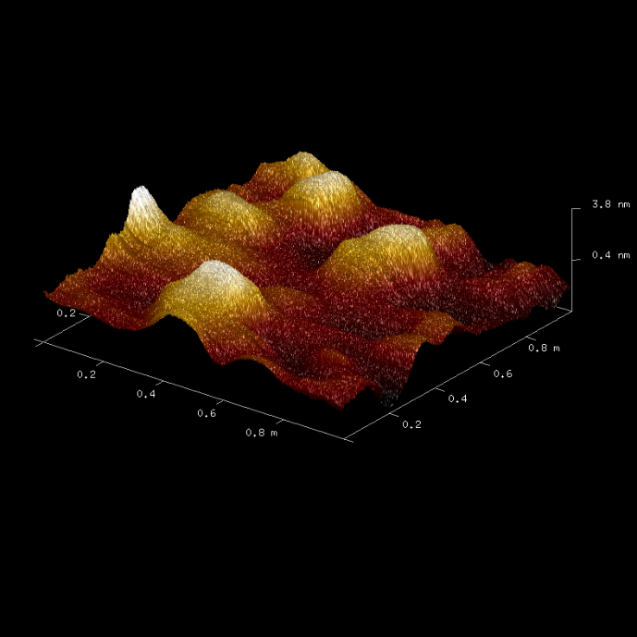


Future iterations of this process could replace the native silicon dioxide with a high-k gate dielectric. This would not significantly impact the net capacitance density, would reduce the leakage current, and would maintain the preferred surface mobility of the GaN/SiN interface.

**Results and Analysis**

In order to assess the uniformity of the ALD SiN, AFM was used to measure the roughness of the SiN surface and contrast it with the sputtered Ru contacts. As can be seen in Figure 3a, the SiN surface is considerably less bumpy than the Ru surface in Figure 3b. Quantitative analysis confirmed this, with the ALD SiN and sputtered Ru surfaces having root-mean-square roughness of 0.496 nm and 0.879 nm respectively.

A close up of food

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b.)

a.)

**Figure 3 –** AFM images of **a.)** ALD SiN and **b.)** sputtered Ru surfaces.

Capacitance-frequency characteristics of the MISCAP were used to extract the capacitance and subsequently the field-effect mobility using a distributed model9. Curve fittings were conducted about the roll-off frequencies at biases above the flat-band voltage. Fitting of the roll-off frequencies detected between 50 kHz and 1 MHz is shown (Figure 4).

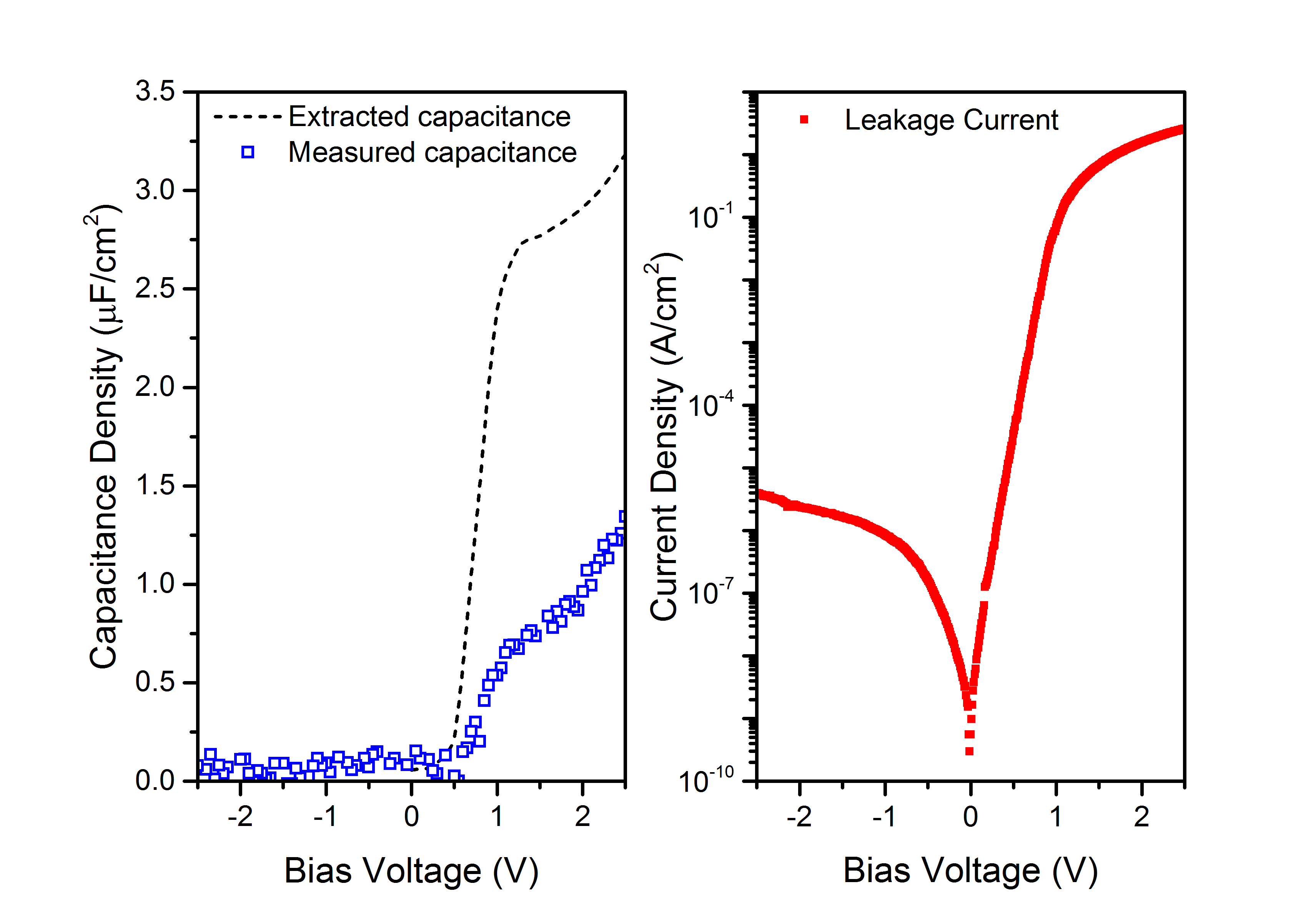
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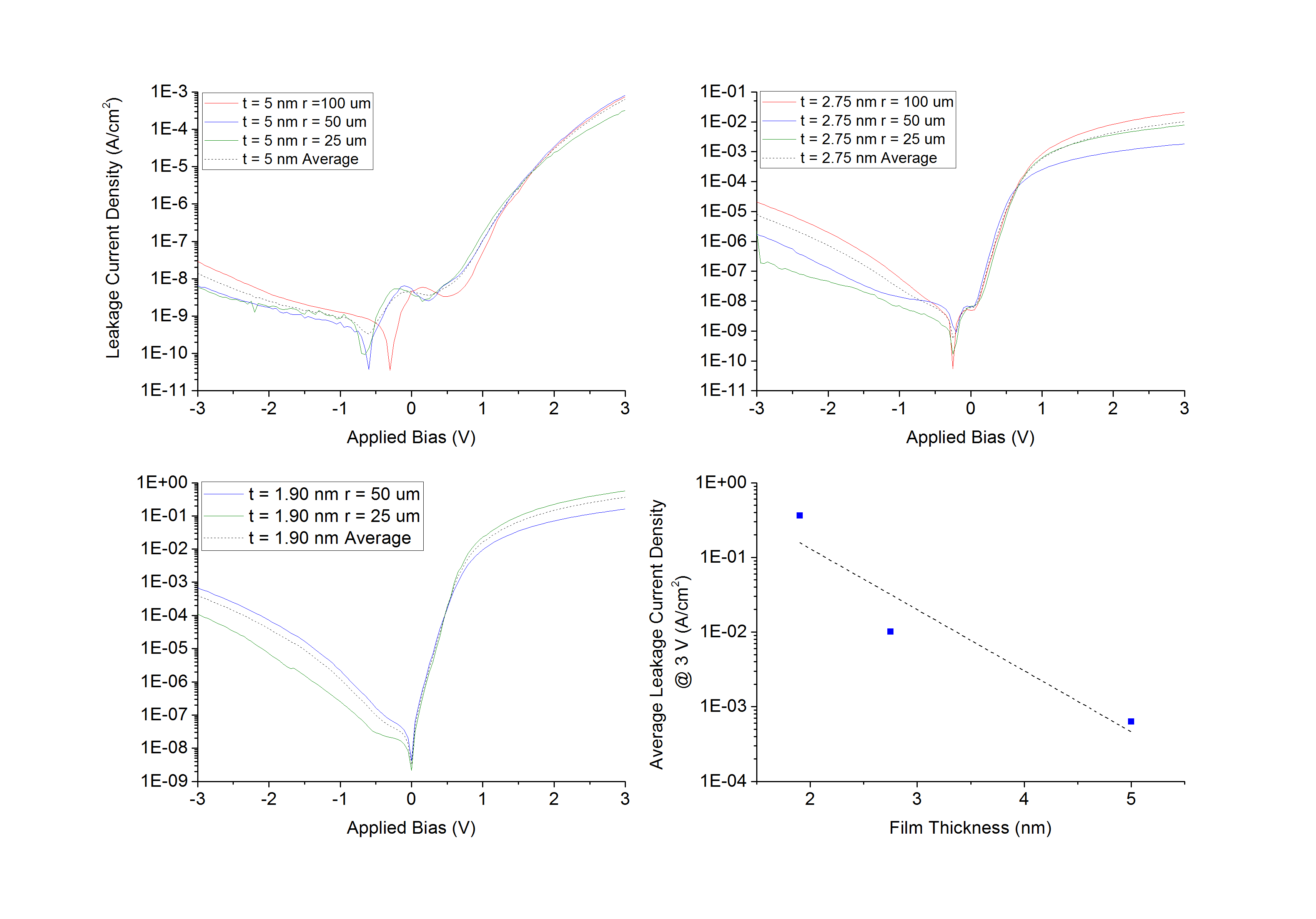
**Figure 4** – Fitted C-f curves at various voltages above flat-band.

From the analysis, extracted capacitance Cex reached a peak of 3.18 μF∙cm-2 at 2.5 V as shown in Figure 5 (2.75 μF∙cm-2 at 1 V is a more conservative estimate), consistent with the in-situ ellipsometry thickness data. The extracted field-effect mobility µFE was found to be 324 cm2∙V-1∙s-1 at a bias voltage of 2.5 V (Table I below). At an estimated field of 8 MV/cm, this mobility was consistent with prior published data10.

In order to further characterize the quality of the SiN films, the leakage current was measured in capacitors of varying area with films of varying thicknesses. The leakage currents were normalized to device area, with the resulting current densities shown in Figure 6 below. As expected, the leakage current density is largely independent of device area and decreases with increasing film thickness. The current density data was also used as a benchmark for the n+ MISCAPs, and both the 1.90 nm n- MISCAP and 2 nm n+ MISCAP showed similar peak leakage current densities under forward bias.

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**Figure 5** – Measured vs. extracted C-V curves and J-V curve.



**Figure 6** – Leakage current densities for n- MOSCAPs with ALD SiN films of thickness **a.)** 5 nm, **b.)** 2.75 nm, and **c.)** 1.90 nm, **d.)** shows the maximum leakage current density vs. film thickness.

**Table I** – Comparison of extracted mobility and capacitance of various MIS devices on GaN.

|  |
| --- |
| **Dielectric (Device Type): Mobility µFE (cm2V-1s-1): Cap. Density (μF∙cm-2): Bias (V):** |
| SiN (MISCAP) \*This work 325 +/- 3.2 +/- 2.5 |
| SiN (MISHEMT)10 203 0.3 17 |
| ZrO2 (MISCAP)11 120 3.8 2.0 |
| HfO2 (MISCAP)11 120 3.0 2.0 |

**Conclusion**

Silicon nitride thin film dielectric deposited by ALD was used to create MISCAP structures on a GaN substrate. Fitting early data to a model has suggested capacitance up to 3.18 μF∙cm-2 and mobility up to 325 cm2V-1s-1. Through this we have highlighted SiN as a potential area of development to improve the dielectric-semiconductor interface in GaN MISFETs for high frequency applications.

**References**

1. Sugiura S, Hayashi Y, Kishimoto S, et al. Fabrication of normally-off mode GaN and AlGaN/GaN MOSFETs with HfO2 gate insulator. *Solid State Electron*. 2010;54(1):79-83. doi:https://doi.org/10.1016/j.sse.2009.10.007

2. Pérez-Tomás A, Placidi M, Perpiñà X, et al. GaN metal-oxide-semiconductor field-effect transistor inversion channel mobility modeling. *J Appl Phys*. 2009;105(11):114510. doi:10.1063/1.3140614

3. Bothe KM, Barlage DW. Underlying design advantages for GaN MOSFETs compared with GaN HFETs for power applications. *J Comput Electron*. 2014;13(1):217-223. doi:10.1007/s10825-013-0502-7

4. Cremers V, Puurunen RL, Dendooven J. Conformality in atomic layer deposition: Current status overview of analysis and modelling. *Appl Phys Rev*. 2019;6(2):21302. doi:10.1063/1.5060967

5. Sun M, Zhang Y, Gao X, Palacios T. High-Performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates. *IEEE Electron Device Lett*. 2017;38(4):509-512. doi:10.1109/LED.2017.2670925

6. Roccaforte F, Greco G, Fiorenza P, Iucolano F. An overview of normally-off GaN-based high electron mobility transistors. *Materials (Basel)*. 2019;12(10):1-18. doi:10.3390/ma12101599

7. Chien Y-HC, Hu C-C, Yang C-M. A Design for Selective Wet Etching of Si3N4/SiO2 in Phosphoric Acid Using a Single Wafer Processor. *J Electrochem Soc* . 2018;165(4):H3187-H3191. doi:10.1149/2.0281804jes

8. Schroder DK. *Semiconductor Material and Device Characterization Third Edition*. 3rd ed. John Wiley & Sons, Inc.; 1990.

9. Bothe KM, Hauff PA von, Afshar A, Foroughi-Abari A, Cadien KC, Barlage DW. Capacitance Modeling and Characterization of Planar MOSCAP Devices for Wideband-Gap Semiconductors With High-κ Dielectrics. *IEEE Trans Electron Devices*. 2012;59(10):2662-2666. doi:10.1109/TED.2012.2209653

10. Zhang Z, Qin S, Fu K, et al. Fabrication of normally-off AlGaN/GaN metal–insulator–semiconductor high-electron-mobility transistors by photo-electrochemical gate recess etching in ionic liquid. *Appl Phys Express*. 2016;9(8):84102. doi:10.7567/apex.9.084102

11. Bothe KM, Hauff PA von, Afshar A, Foroughi-Abari A, Cadien KC, Barlage DW. Electrical Comparison of HfO2 and ZrO2 Gate Dielectrics on GaN. *IEEE Trans Electron Devices*. 2013;60(12):4119-4124. doi:10.1109/TED.2013.2283802

**Acronyms**

ALD – Atomic Layer Deposition

PEALD – Plasma Enhanced Atomic Layer Deposition

GaN – Gallium Nitride

SiN – Silicon Nitride

HEMT – High Electron Mobility Transistor

MISHEMT – Metal Insulator Semiconductor High Electron Mobility Transistor

MISFET – Metal Insulator Semiconductor Field Effect Transistor

MISCAP – Metal Insulator Semiconductor Capacitor

AFM – Atomic Force Microscopy