Defect Inspection for Compound Semiconductor Wafers

# Varun Gupta, Peimei Da, Akash Nanda, Edwin Chew, Mukundkrishna Raghunathan

KLA Corporation, One Technology Drive, Milpitas, California 95035, USA

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## **Abstract**

**With expanding applications and growing performance requirements in Power, RF and Optoelectronics markets, leading device manufacturers are looking for new ways to characterize yield-limiting defects that will help them achieve faster development and ramp times, higher product yields and lower device costs. Full-surface, high sensitivity defect inspection and accurate process control feedback has enabled the industry to improve substrate quality as well as to optimize the yields on epitaxy growth processes.**

**As device manufacturers continue to push the boundaries of process designs, the requirements for defect inspection and overall yield management become increasingly more stringent and critical. The Candela unified surface and photoluminescence (PL) defect inspection platform enables high sensitivity inspection and defect classification at production throughputs of a wide range of critical defects (e.g. micro scratches, stacking faults, basal plane dislocations) and effectively separates front-surface defects and buried defects on transparent SiC substrates and epitaxial material. In addition, automated defect classification capabilities reduce the time required to identify, source and correct various yield-limiting defects such as carrots, triangles, sub-micron pits and others.**

**The process of growing III-V epitaxy has unique challenges. The large mismatch in the lattice constant and the thermal expansion coefficient between epitaxy layer and substrate causes high lattice stress which leads to cracking on and through the epitaxy layer, making parts of the wafer unsuitable for device production. This cracking can be minimized by using a suitable buffer layer and optimizing the epitaxy reactor conditions. Improper epitaxy reactor conditions may also cause other device reliability killer defects such as micropits, craters, epi droplets and/or bumps.**

**This study discusses how multiple complementary techniques such as scatterometry, reflectometry, ellipsometry and photoluminescence could be used together for simultaneous detection and classification of multiple critical defects on compound semiconductor wafers. We demonstrate how feedback from defect inspection equipment can be used to screen incoming substrate wafers and to monitor and optimize the performance of CVD reactors during the epitaxy process.**

## Introduction

The growth of silicon carbide (SiC) and gallium nitride (GaN) technologies has been the key focus for power electronics, RF and optoelectronics manufacturing. The promising performance of SiC and GaN are driving significant development resources in 2020 by world-leading device manufacturers to try to break down barriers for universal wireless charging to advanced power converters.

While wide-bandgap technologies offer significant performance capabilities, device makers must overcome numerous technical challenges and reliability issues to gain greater market adoption. In order to characterize and manage yield-limiting defects that impact yield, full-wafer defect inspection is indispensable for quick process debugging and timely, accurate process control feedback. The *Candela* integrated surface and photoluminescence inspection platform enables high sensitivity inspection and classification to a wide range of critical substrate and epitaxy defects suitable for production applications. Implementation of automated wafer inspection with statistical process control methodology can significantly minimize yield loss due to epi defects, reduce metal-organic chemical vapor deposition (MOCVD) reactor process excursions and increase MOCVD reactor uptime.

## Overview of the Candela defect inspection platform

The Candela full-wafer defect inspection platform integrates both macro and micro detection for surface and crystal defects of compound semiconductor materials. As illustrated in Figure 1, the Candela platform employs proprietary optical designs to simultaneously measure scattering intensity from a normal laser and oblique laser, as well as wafer surface reflectivity, topographic variations, phase shift and photoluminescence. Multi-channel detection enables accurate and automatic classification of a broad range of defects of interest across multiple compound semiconductor device types. This inspection platform achieves full-surface coverage in minutes and produces high-resolution images and wafer maps with customized, classified defects. The results from the Candela defect inspection platform allow process engineers to make quick, informed decisions regarding the health of the process. Different defect types and image examples of SiC and GaN materials will be discussed in the following sections.

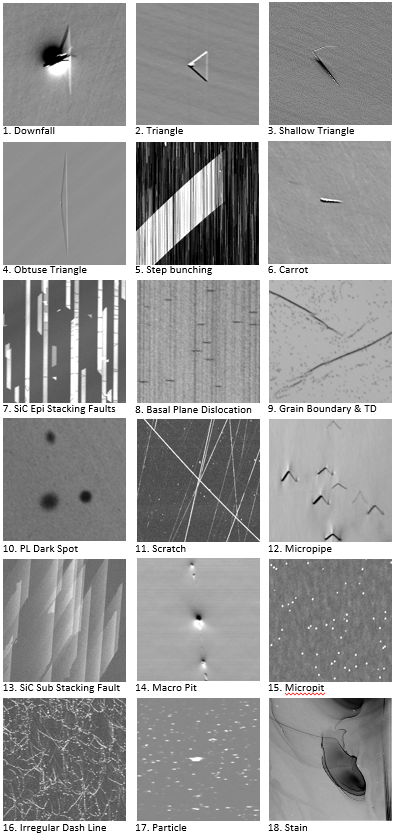


Figure 2. Image examples of SiC substrate with various epitaxy defects. Number 1-10 images are defect examples observed on SiC epitaxy wafers. Number 11-18 images are defect examples observed on SiC substrate wafers. Process defects (scratch, pit, particle, stain) widely exist on almost all material types of wafers.

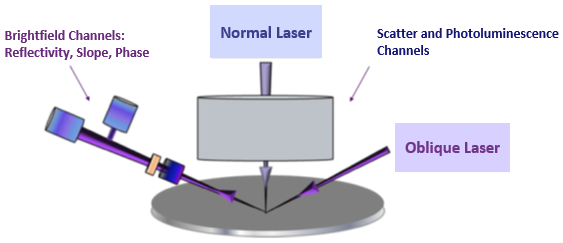


Figure 1. Optics overview of the integrated surface and photoluminescence inspection system.

## Defect inspection for SiC

SiC crystal growth is a high temperature, single crystal process that must be carefully controlled to produce the proper crystal polytype with minimum impurity levels. However, besides inevitable crystal defects in the step-controlled epitaxy process, there is much evidence that substrate defects can migrate into the post-epi layer, including process defects and crystal defects. In particular, the occurrence of micropipes can fatally damage device performances. Thus, monitoring the wafer defectivity level in a non-destructive way before and after the epitaxy process are critically important to optimize the yield and reliability of manufactured devices.

In addition to detection and classification of various killer defects using its multi-channel architecture, Candela inspection system provides the option to save raw images collected from multiple detectors for further in-depth review of defect characteristics. The tool can also effectively capture and extract unique defect type signatures which are detected on one or more of the detection channels present on the tool. For example, the phase channel is used specifically for sensitive stain (Figure 2-18) detection.

The image gallery in Figure 2 shows some of the common yield-impacting defect images of SiC substrate and epitaxy layer collected with the Candela inspection platform. For macro surface defects, such as downfall, triangle, carrot and macro-pit, topographic signatures and defect attributes are normally used for classification. Micro defect classification such as particles and micro-pits is based on comparison of scattering intensity between normal- and oblique- incidence. The Candela inspection platform has photoluminescence detectors covering near ultra violet and visible bands, which are optimized for detection of SiC crystal defects like BPD, stacking faults, grain boundary and other unusual PL activity induced by crystal defects.

The primary inspection channel for scratch detection on the Candela platform is the normal incidence scatter signal. Since the penetration depth of the normal laser into SiC material is ~ 50µm, good frontside versus backside signal separation is achieved. In contrast, another commonly used technique based confocal technology cannot screen out signals from the wafer backside, including backside scratches or vacuum pad marks. Also, as confocal technology has a relatively lower sensitivity than scatterometry, faint CMP scratches that are barely visible on confocal OM images can be easily captured using the scattering signal.

At major SiC device manufacturers, non-optimized SiC CMP processes are a major contributor to yield loss. It is therefore critical to identify all killer scratches since SiC substrate quality impacts final production yield. As shown in Figure 3, there is a direct transfer of SiC substrate scratches and CMP polishing residues to the SiC epitaxy defects detected post epi growth. From the inset traceback images of scatter and PL channels, severe step bunching, stacking faults and triangular defects are caused by scratches from substrates. The Candela software records the coordinates of all automatically classified defects, and the traceback function of the Candela defect map enables convenient defect image review and pre/post epi image comparison.

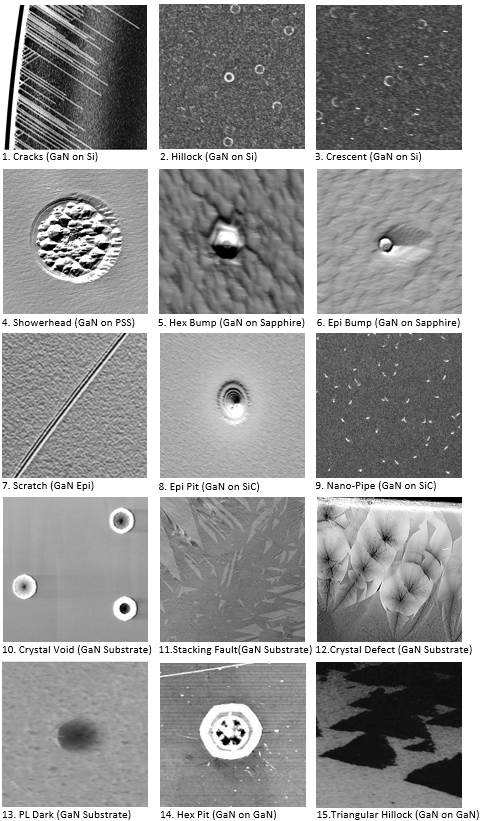


Figure 4. Image examples of GaN epitaxy and bulk GaN defects.

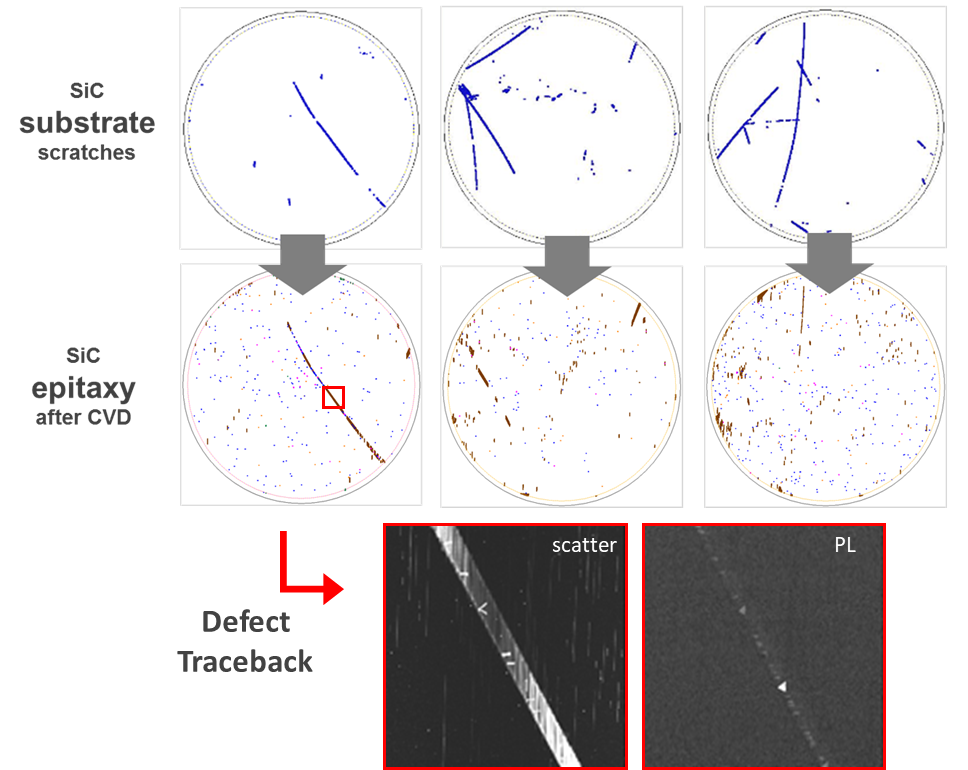


Figure 3. Demonstration of how CMP scratches on the SiC substrate can be the root cause of SiC epi stacking faults and macro step (step bunching aggregates).

Similar substrate-to-epi correlations have also been observed for SiC crystal defects using Candela technology: (1) defects on SiC substrate can induce epi stacking faults[1]; (2) severe substrate grain boundaries can propagate into the post epitaxy layer[2]; (3) substrate PL bright spots are verified to be nucleation centers of surface “V” shape killers [3].

Micropipe defects are well known to cause fatal leakage current on SiC devices, and very high correlation has been observed between micropipes on SiC substrates and device yield [4]. Today, manual defect counting, map drawing and density calculation are widely used for micropipe monitoring, with approximately 20 minutes per one 4-inch wafer required for an experienced operator to go through the process. In addition to being time-consuming, other challenges lie in manpower cost, operator subjectivity, potential omissions, and no image traceback/review. Automated full wafer micropipe mapping plus the image review feature can be realized with the Candela platform, with a high throughput of ~2 minutes per 4-inch wafer. In the Candela inspection platform, different channels are used as the primary channel for pit and micropipe separation to accurately distinguish them, avoiding overkill of wafers. Micropipes have a unique “seagull” signature in specular channels while macro-pits show a negative-to-positive signal change in surface topography (refer to the macro-pit and micropipe images in Figure 2). For pits smaller than 20µm, the scattering intensity ratio between normal and oblique lasers is used for classification.

## Defect inspection for GaN

Growing III-V epitaxy has its own challenges. GaN systems are intrinsically highly defective layers, MOCVD processes produce a variety of defects when a GaN epi layer is grown on different substrate materials (silicon, sapphire, PSS, SiC and GaN), in addition to the fabrication challenges of bulk GaN wafers. The Candela inspection platform is capable of detecting yield-impacting defects including cracks, hexagonal bumps, hexagonal pits, showerhead droplets, crescents, scratches, crystal defects and other topographic and novel defects. The image gallery in Figure 4 shows examples of different GaN defects. The photoluminescence imaging on GaN epitaxy provides accurate yield impact information for defects on multi-quantum well (MQW) structure as photoluminescence can reflect the actual impacted region which is often much larger than the scatter response from the wafer surface.

Cracks are one of the most important killer defects in GaN-based devices. The large mismatch in the lattice constant and the thermal expansion coefficient between the GaN epi layer and a foreign substrate creates a high level of stress which results in cracking on and through the epitaxy layer. Some cracks can extend far into the wafer center, with cracked parts of the wafer no longer suitable for device fabrication. The Candela inspection platform is highly sensitive for crack detection, using the physics and algorithms of the scatter channels. Detection results provide direct feedback to allow process engineers to tune buffer layers or to optimize reactor conditions. Further, pseudo die grid overlay capability can determine the percentage of the wafer impacted by defects. Automated defect binning/length statistics output are also available for high volume manufacturing process control and process development. The tool user can set the wafer PASS/FAIL criterial based on crack die impact and length statistics in the factory automation setup.

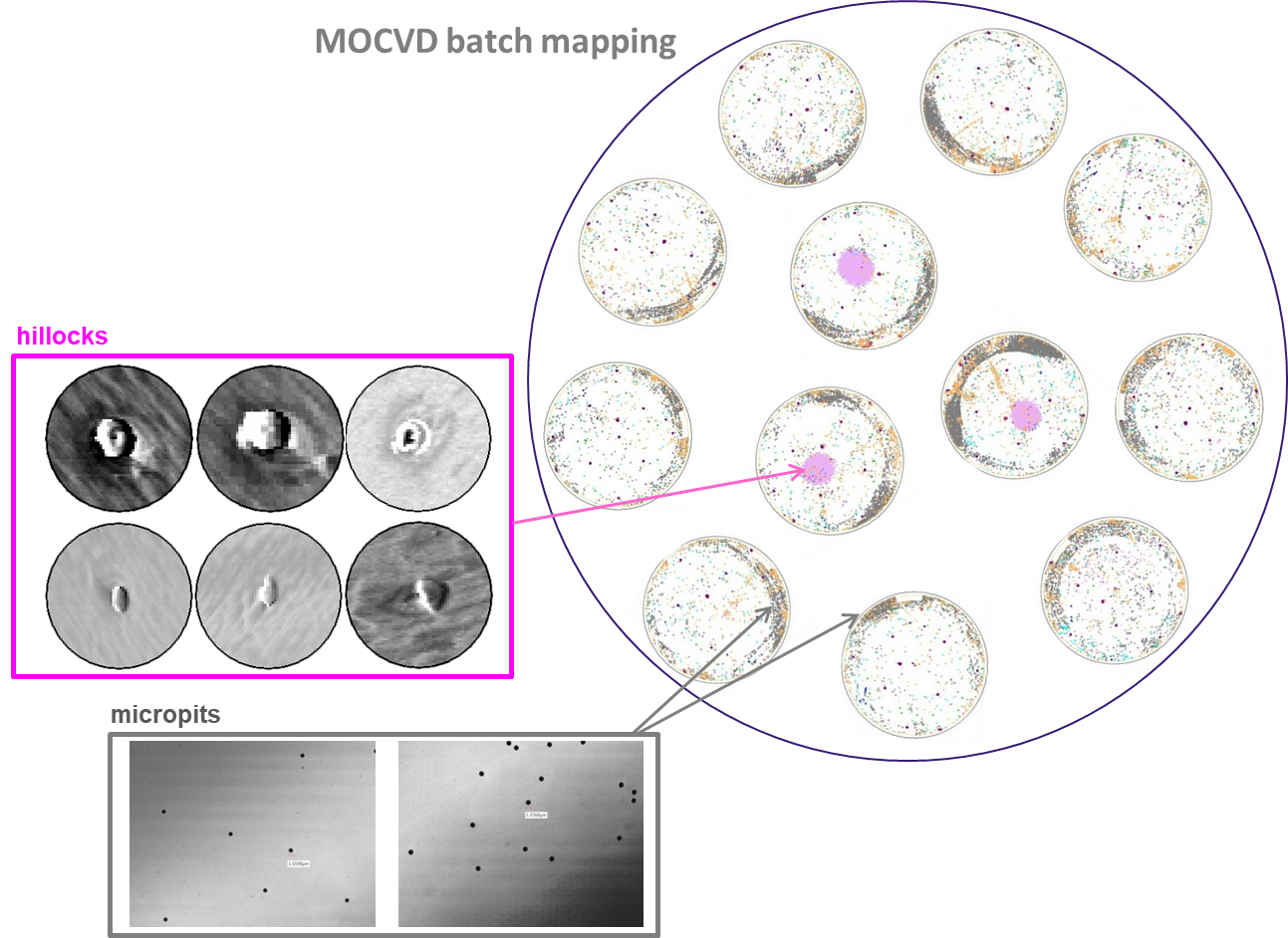


Figure 5. The Candela system can help capture MOCVD reactor dynamics and flag improper or variable reactor conditions. From inspection wafer maps, clear defect trends are observed across the MOCVD chamber, and potential temperature gradients across pockets induce different distribution of hillocks and micropits.

Finally, the Candela inspection platform can also help to flag improper MOCVD reactor conditions using MOCVD batch defect mapping. As shown in Figure 5, 12 wafers from the same MOCVD batch are scanned and analyzed using the inspection platform. Excursions of hillocks are flagged in the centering pockets, indicating potential temperature gradients across these pockets, as hillocks usually aggregate under relatively higher temperature while micropits are induced at relatively lower temperature. Particle droplets inside pockets might potentially result from a non-uniform heating surface. From the chamber mapping results of all pockets, a clear trend of higher micropit density toward the MOCVD chamber center is also observed, signifying uneven heating across the entire chamber.

## Conclusions

This paper discussed how multiple complementary technologies including scatterometry, reflectometry, ellipsometry and photoluminescence can be integrated together for fast and accurate automated defect inspection and classification of compound semiconductor materials. The Candela inspection platform’s high sensitivity, versatility and throughput provide a comprehensive solution for multiple inspection points during production, such as incoming wafer screening, process development and monitoring. Implementation of automated wafer inspection with statistical process control methodology will significantly reduce yield loss due to timely feedback of substrate/epi defects, increase better utilization of MOCVD reactor uptime, and finally achieve faster ramp and lower cost.

## Acknowledgements

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Acronyms

BPD: Basal plane dislocation

CMP: Chemical-mechanical polishing

GAN: Gallium Nitride

HEX: Hexagonal

MOCVD: Metal-organic chemical vapor deposition

MQW: Multiple quantum well

PL: Photoluminescence

PSS: Patterned sapphire substrate

SF: Stacking fault

SIC: Silicon Carbide

TD: Threading dislocation