Formation of Diamond Superjunctions to Enable GaN-Based Super-Lattice Power Amplifiers with Diamond Enhanced Superjunctions (SPADES)

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## **Abstract**

 **The super-lattice power amplifier with diamond enhanced superjunctions (SPADES) is a device that incorporates nanocrystalline diamond superjunctions into the super-lattice castellated field effect transistor (SLCFET), to improve breakdown voltage. A diamond superjunction is formed with p-type nanocrystalline diamond to balance mutual depletion between the two-dimensional electron gas superlattices and the doped diamond in order to reduce the peak electric field in the drain access region. Formation of the diamond superjunction presents several challenges, such as managing diamond conformality, strain, and control over p-type doping. Optimization of diamond growth led to conformal films, with low stress, and linear dependence hole concentration from p-type doping, suitable for the SPADES device.**

## Introduction

 Stacking multiple AlGaN/GaN layers induces multiple two-dimensional electron gas (2DEG) channels, forming a superlattice, increasing the areal charge density. Compared to planar GaN high electron mobility transistors (HEMTs), with a single 2DEG channel, multiple 2DEGs reduce the on-resistance, improving the achievable power density and gain [1-4]. However, to electrostatically control the stack of 2DEG channels, a novel 3D castellated gate structure must be employed. The resulting device is known as a Super-Latticed Castellated Field Effect Transistor (SLCFET) [1-4].

 The extremely high charge density that results from the stacked 2DEGs creates electric field crowding at the drain side of the gate leading to premature breakdown. For the devices reported here, a nanocrystalline diamond (NCD) superjunction is formed within the drain access region to manage the electric field profile, and thereby to improve the breakdown voltage. The resulting device is termed a super-lattice power amplifier with diamond enhanced superjunction (SPADES), shown in Figure 1. Formation of the NCD superjunction poses several challenges which will be discussed in this work, including conformal NCD growth within small aspect ratio features, strain management, and achieving controllable p-type doping of the NCD films.



Figure 1. Schematic of SLCFET with a T-gate

## Experiment

 NCD was deposited by microwave plasma chemical vapor deposition at 750C. The diamond growths were primarily performed in a 1.5 kW reactor designed for uniform growth across 2 inch diameter wafers, however the chuck was modified to accept 4 inch wafers, compromising film thickness uniformity. To achieve uniform thickness of NCD growths across 4 inch wafers, the growth process was transferred to a 6.5 kW reactor designed for uniform NCD thickness across 4 inch wafers.

 P-type dopant incorporation into the NCD films was achieved by introducing diborane (B2H6) during diamond growth. Test structures were fabricated to characterize the NCD properties, such as Van der Pauw (VdP) structures. O2 inductively coupled plasma reactive ion etching was performed to create mesa isolation. Ohmic contacts were formed by evaporation and lift-off of Ti/Al/Ni/Au, followed by a N2 rapid thermal anneal at 600C for 5 minutes.

## Results and Discussion

 Ultra-sonic dispensing of nanodiamond seeds was used to create NCD films that conformally fill high aspect ratio features, such as required in the SPADES device. To optimize the NCD conformality when deposited over surfaces exhibiting high aspect ratios (such as encountered in the SPADES devices), trenches were patterned into a Si substrate to act as a test structure mold for NCD growth. NCD seeds were then dispensed across the patterned Si substrate. Then, nucleation of the diamond film begins in the NCD growth reactor with a coalescence step to ensure the seeds grow together. Then, the NCD film was grown from the coalesced seeds in a columnar fashion. As the NCD film thickness increases, the size of the NCD grains also increases. The patterned Si substrate was then fully etched away in HNA (HF:Nitric:Acetic), leaving behind a membrane of diamond with the mold of the patterned Si wafer. The rigidity of the NCD film maintained the membrane even at a ~0.5 μm film thickness. Then, the nucleation interface of the diamond was imaged from the nucleation side to observe the quality of filling (Figure 2).



Figure 2. NCD deposited into Si trenches and then the Si is removed and imaged from the nucleation side.

 This optimized process of seed dispersion, diamond nucleation/coalescence, and growth was then implemented on a SPADES device, as shown in Figure 3. The p-type diamond superjunction (SJ) is created on the drain access region in order to deplete some of the SLCFET channel charge. Hydrogen silsesquioxane (HSQ) is used as a temporary mask to block off certain regions of the device from receiving the NCD film. Then, an O2 ICP RIE is used to etch the diamond film to form the SPADES device shown in Figure 3.



Figure 3. Images showing filling of NCD in the gate-drain region of the SPADES device.

 Precise control of the p-type doping level in the NCD superjunction in the SLCFET is required, to balance the charge in the NCD, and thus the total charge in the channels, in order to reduce the electric field and not sacrifice on-resistance. In order to accurately control the p-type doping, NCD wafers were grown while varying the B2H6 flow from 2 to 3 sccm. NCD films were grown ~0.5 μm thick on semi-insulating Si wafers with 200 nm of thermal SiO2 to isolate the NCD film from the Si wafer, to ensure carrier transport only occurs in the NCD films. Van der Pauw structures were fabricated on these test structures, and the free hole concentration was determined using AC Hall effect measurements on a Lakeshore cryogenic probe station. To accurately determine the NCD film thickness (since thickness non-uniformities existed in films grown in the 1.5 kW reactor), the diamond thickness was measured on the mesa of each VdP structure by profilometry. As shown in Figure 4, the hole concentration increases exponentially with B2H6 flow. Over two orders of magnitude in hole concentration variation was achieved with low variability in the doping level. The in-plane mobility of the NCD films is low, on the order of 1 cm2/Vs, which is expected due to the granular columnar nature of the NCD film.

Figure 4. AC Hall measurement of hole density versus B2H6 flow rate

 The diamond growth process was then transferred to a 6.5 kW reactor suitable for uniform growth across 4 inch diameter wafers. Optimization was required to ensure low stress in the diamond films. Any significant stress in the diamond would create issues integrating the diamond into the SLCFET process for the SPADES device. To characterize the stress in the NCD films, the methane/hydrogen ratio was varied while growing on 4 inch Si wafers. The Si wafer bow was mapped with the k-Space Associates, Inc. kSA multi-beam optical sensor (MOS) before and after diamond growth. Figure 5 shows the resulting stress map in GPa.



Figure 5. Stress map of NCD on Si determined by wafer curvature measurements.

## Summary

 P-type NCD films were grown by microwave plasma chemical vapor deposition and integrated onto SLCFET devices to create a SPADES device. Optimization was performed to ensure conformal filling of high aspect ratio small features, control over doping, and low stress across 4 inch wafers.

## References

1. R. S. Howell *et al.*, “The Super-Lattice Castellated Field Effect Transistor (SLCFET): A novel high performance Transistor topology ideal for RF switching,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015 February, p. 11.5.1-11.5.4, 2015.
2. R. S. Howell *et al.*, “Advances in the Super-Lattice Castellated Field Effect Transistor (SLCFET) for wideband low loss RF switching applications,” in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, vol. 2016–August, pp. 1–3.
3. T. J. Anderson *et al.*, “Nanocrystalline Diamond Integration with III-Nitride HEMTs,” *ECS J. Solid State Sci. Technol.*, vol. 6, no. 2, pp. Q3036–Q3039, Oct. 2017.
4. J. Chang *et al.*, “The super-lattice castellated field-effect transistor: A high-power, high-performance RF amplifier,” *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1048–1051, 2019.