**High-Gate-Voltage-Swing Region of Normally-Off *p*-GaN MIS-HEMT With ALD-Grown Al2O3/AlN Gate Insulator Layer**

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## **Abstract**

**Metal–insulator–semiconductor *p*-type GaN high-electron-mobility transistor with an Al2O3/AlN deposited by atomic layer deposition was investigated. The selected insulator, AlN has been proven to have a good interface with GaN. A traditional p-GaN device without an Al2O3/AlN layer was processed for comparison. Due to the Al2O3/AlN layer, the gate leakage was lower, and the threshold voltage was higher, at 4.7 V. Additionally, excellent turn-on voltage was obtained. Furthermore, low current degradation and smaller VTH shift at high temperatures was also observed. Hence, growing a good-quality Al2O3/AlN layer can achieve an enhancement-mode operation with superior stability and high gate swing region.**

## Introduction

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are crucial for high-frequency and high-power applications because of their material attributes, including excellent thermal properties, high breakdown fields, and high mobility levels. Typical implementation of simple circuits requires normally-off devices with high performance. Several methods, such as fluorine ion treatment [2], gate recess [3], and employing a *p*-type GaN cap layer [4], [5], have been considered for use in normally-off devices; *p*-type GaN layers can achieve positive threshold voltagewithout affecting channel mobility and are widely considered the most effective of these approaches. However, both uniformly etching away *p*-GaN from the ungated access region and overcoming plasma-induced damage [6] during *p*-GaN removal are challenging. Cl2-based ion etching is typically used to remove the *p*-GaN layer. If such etching is imprecise, it may result in a rough surface with plasma bumps, in-surface defects, or other damages; these may cause gate lag [7]. To control etching depth, an AlN etching stop layer [8] between the *p*-GaN and barrier layers can achieve highly selective etching for superior etching uniformity, lower gate leakage, and lower dynamic on-resistance. Typically, the low hole concentration of *p*-GaN limits the threshold voltage; when this occurs, the resulting product in unsatisfactory practical applications. Moreover, the *p*–*n* junction gate turns on under forward bias,

leading to notably high gate leakage current. In this study, to minimize defects that may arise after *p*-GaN etching and increase the gate swing region, we deposited Al2O3 and AlN layers [9] through atomic layer deposition (ALD)on the device surface; these layers improved device performance and

turn-on voltage, reduced gate leakage current, and improved device stability at high temperatures.

## Experimental Procedures

The HEMT structures used for our devices were grown on 6-inch Si (111) substrates through metal–organic chemical vapor deposition (MOCVD). A 300-nm-thick undoped GaN channel was deposited on top of a 4-μm-thick undoped GaN buffer transition layer. Subsequently, a 12-nm-thick Al0.17Ga0.83N layer, 1-nm-thick AlN layer, and 70-nm-thick *p*-type GaN top layer were deposited. TheAl2O3/AlN interlayer was deposited by ALD. A schematic representation of the device is presented in Fig. 1(a).

(b)

(a)

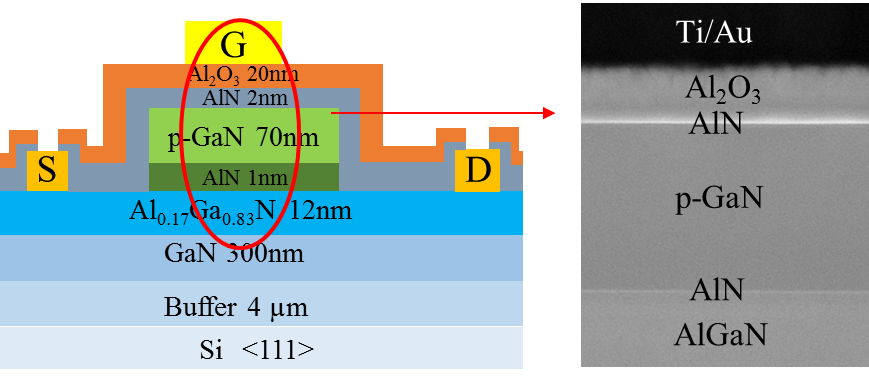


Fig. 1. (a)Schematic of the device structure. (b) TEM photograph of the device. x

The device was thermally annealed in an MOCVD chamber at 720 °C for 10 min in a N2 atmosphere. The active Mg concentration was 1 × 1018 cm−3, according to Hall measurement. The device was fabricated using mesa isolation with inductively coupled plasma (ICP) for the first step. Second, a *p*-GaN layer was etched by ICP etching with Cl2/BCl3/SF6 as the etching gas. When the mixed gas reached the AlN layer, the SF6 plasma [10] reacted with the Al atoms and formed a thin AlF3 etching stop layer. Subsequently, the sample was soaked in diluted HF/NH4F solution to remove the AlF3. Then, a Ti/Al/Ni/Au (25/120/25/150 nm) ohmic metal stack was deposited to serve as the source and drain through electron beam evaporation (E-gun); the metal stack was annealed at 875 °C for 30 s in a N2 atmosphere with an RTA system.



Fig. 2. Energy band diagram for Metal-gate and MIS-gate HEMT

The oxide/insulator layer Al2O3/AlN (20/2nm) was deposited by ALD, as show in Fig. 1(b), and the band diagram is also show in Fig. 2, after which the ohmic via was etched by buffered oxide etching. Then, Ti/Au (25/120 nm) layers were deposited by E-gun to serve as gate electrodes. A second device with metal gates (but without Al2O3/AlN layers) was fabricated for comparison.

## RESULTS AND DISCUSSION

For examination of the effect of the Al2O3/AlN/*p*-GaN interface on device performance and the relationship of the AlN layer formed by ALD with an AlN etching stop layer at the sidewall and ungated region, device *I*–*V* characteristics were measured. Because an Al2O3/AlN layer can fill the nitrogen vacancies on the surfaces of *p*-GaN and AlN, depositing an Al2O3/AlN layer has the same effect as passivation. The *I–V* curve revealed that the gate leakage current was suppressed. Furthermore, because the polarization effect was enhanced by the Al2O3/AlN layer, the metal–insulator–semiconductor MIS-gate HEMT presented a higher drain current density and superior on/off ratio, that MIS-gate has three orders more than the metal-gate HEMT, as illustrated in Fig. 3 (a). *I*DS–*V*DS characteristics are graphed in Fig. 3 (b). The saturated drain currents of the MIS-gate and metal-gate devices were 303 and 249 mA/mm at *V*DS = 10 V. In Fig. 3 (c), the MIS-gate HEMT data are graphed, demonstrating that the Al2O3/AlN layer had high gate voltage swing region [11].

To determine device reliability, Schottky breakdown voltage and OFF-state breakdown voltage were measured; when measuring the OFF-state breakdown voltage, the device gate must be biased to 0 volts to ensure that the device is in the off state. The results are graphed in Fig. 4. Because the Al2O3/AlN layer had the similar effect as passivation and minimized any damage that might be caused by etching, the Al2O3/AlN gate device presented higher Schottky breakdown voltage and off-state breakdown voltage. The typical device had a Schottky breakdown voltage of 310 V and OFF-state breakdown voltage or 298 V, whereas the Al2O3/AlN-gate device had 454 V and 358 V, respectively.

(a)

(b)



(c)



Fig. 3. (a) *I*DS–*V*GS, (b) *I*DS–*V*DS, (c) *I*GS–*V*GS characteristics of the *p*-GaN HEMTs with a metal (red) or MIS gate (blue).



Fig. 4. Schottky breakdown voltage and OFF-state breakdown voltage of metal- and MIS-gate devices.

In order to observe device stability behavior, *I*–*V* characteristics with temperature increase and pulse measurement was measured. As illustrated in Fig. 5 and Fig. 6. With every 25° increase in temperature, the current of the proposed MIS-gate HEMT degraded by approximately 11%, preferable to the 17% degradation of the typical metal-gate HEMT, furthermore, when the temperature increased, the IDS–VGS curve of MIS gate had a positive shift of approximately 0.42 V at a drain current of 1 mA/mm, which was smaller than the 0.67 V positive shift for metal gate.



Fig. 5. *I*DS–*V*GS characteristics at different temperatures (logarithmic scale).



Fig. 6. With quiescent gate bias stress voltage of *Ron* ratio.

The dielectric layer Al2O3/AlN exhibits similar capability in suppressing the current collapse in p-GaN/AlGaN/GaN HEMTs, Fig. 6 graphs the dynamic to static on-resistance ratio (*R*Dynamic, on:*R*Static,on) at different quiescent gate voltages. There are three bias conditions need to set up which are pulse voltage (VGS, VDS) and quiescent voltage (VGSQ, VDSQ), during the measurement, when the quiescent voltage was applied, the carrier will be trapped by the defect. When the pulse voltage switching to the quiescent voltage rapidly, after calculation, the dynamic to static *R*on ratio of the MIS- and metal-gate HEMTs was switched with a 2 μs pulse width and 200 μs period, the quiescent gate bias was swept from 0 to −15 V with a 5 V increment. Clearly, the MIS-gate HEMT exhibited superior dynamic *R*on to that of the metal-gate HEMT, improving it from 2.13 to 1.24. Therefore, the MIS-gate HEMT had a lower surface trap density surface, which inhibited current collapse. The *R*on ratio under different temperatures was also measured. At high temperatures, the ratio of the MIS-gate HEMT exhibited less variance than did that of the other device. The Al2O3/AlN layer not only minimized surface defects but also proved that this MIS-gate HEMT had greater device stability at high temperatures.



Fig. 7. *C-V* measurement with different frequency.

High-frequency Capacitance-voltage (*C-V*) curves were measured to investigate the effective density of the interface traps *Dit* [12]. In this work, the frequency of the *C-V* measurement is 10kHz to 1MHz in Fig. 7, Fig. 7 shows the hysteresis and multi-frequency *C-V* curves of the MIS- and metal-gate HEMTs. The interface trap density (*Dit*) values were 8.1×1012 cm−2 eV−1 and 1.7x1011 cm−2 eV−1, respectively. Although the AlN layer was an excellent interface with the GaN, to suppress the current collapse, the interface charge of the Al2O3 layer generates more trap density, which leads to higher *Dit*. However, even with the shortcoming of higher trap density, the dielectric layer Al2O3/AlN outperforms other dielectrics, such as SiN*x* and HfO2 [13].

## Conclusions

In summary, a normally-off *p*-GaN HEMT with an Al2O3/AlN layer has been investigated. The device exhibits excellent *I*–*V* characteristics. The turn-on voltage was 16 V, with a threshold voltage of 4.7 V and high saturation drain current (approximately 303 mA/mm), and the gate leakage current and instability were suppressed. The device Schottky and OFF-state breakdown voltages in the MIS gate improved because of the Al2O3/AlN layer deposited by ALD formed an excellent interface between the *p*-GaN and AlN. The lower trap density and trapping/de-trapping effects were analyzed by pulse measurement. Overall, the Al2O3/AlN dielectric gate layer can really greatly improve the performance, reliability and stability of the device. Therefore, the as-developed design exhibits high potential for repeatable and manufacturable normally-off *p*-GaN gate HEMTs for use in practical applications.

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