**Effect of Process Variation on Pinch-Off   
Voltage of Depletion-Mode pHEMT**

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**ABSTRACT**

**Pinch-off voltage is a key device characteristic of depletion-mode pseudomorphic high electron mobility transistors (pHEMT).** **Pinch-off voltage (Vp) shifts caused by manufacturing process variation were studied in this paper. Experimental results showed higher pinch-off voltage if the AlGaAs Schottky layer is oxidized or contaminated by metal. A significant increase in pinch-off voltage was observed when the Schottky layer was exposed to air for up to 2 hours after oxygen plasma treatment. Investigation also revealed an increase in pinch-off voltage in relation to staging time and environment before gate contact metal deposition. In both cases, the effective thickness of the AlGaAs Schottky layer was reduced, and pinch-off voltage was increased. Models of metal cross-contamination and a “last wafer” effect in wet clean processing were also evaluated to address pinch-off voltage variation.**

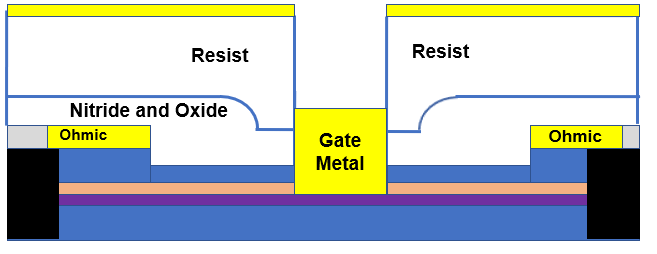
INTRODUCTION

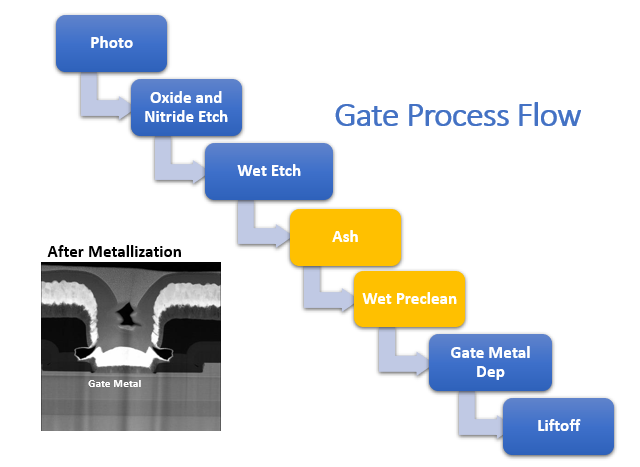
Pseudomorphic High Electron Mobility Transistors (pHEMT) are a well-established technology forintegrated wireless components1-4. Qorvo has many generations of pHEMT products utilizing double recess enhancement and depletion-mode GaAs/AlGaAs/InGaAs transistors1. The nominal pinch-off voltage (Vp) is targeted at -800 mV for depletion-mode pHEMT1. Shifts in pinch-off voltage could affect device performance and may lead to reliability concerns, therefore Vp variation is the main yield killer for pHEMT manufacturing. This is especially true for positive Vp variation, because this can cause low switch speed for pHEMT devices.

Many different manufacturing process factors can affect pinch-off voltage uniformity. Several failure mechanisms are discussed in this study including long exposure times of the AlGaAs Schottky surface to air, and cross-contamination during wet cleans processing caused by combining processes or sub-optimal wafer loading. Avoiding these can significantly reduce pinch-off voltage variation, both within wafer and wafer-to-wafer.

DEVICE FABRICATION FLOW

In this work, gate features were defined by a bi-layer photo process to create lift off undercut, as shown in Figure 1.





**Figure 1. Device structure and gate process flow**

After photo develop, a dry etch process was used for oxide and nitride removal, followed by wet etch for epi recess. Oxygen plasma and wet cleans were used to remove etch residue and surface oxide. Ti/Pt/Au stacks were used as gate contact metal to the AlGaAs Schottky layer and were deposited using a DC sputter system. Then the gate metal liftoff was completed in a solvent sink followed by quick dump rinse in water.

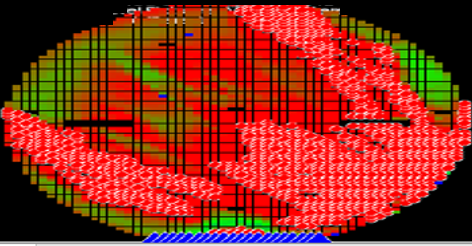
To improve wafer and die yield of pHEMT technology, experiments were conducted at the oxygen plasma and wet preclean steps prior to gate contact metal deposition to understand the root causes of increased pinch-off voltage (Vp).

RESULTS AND DISCUSSION

**I. High Pinch-off Voltage: AlGaAs Schottky Layer Oxidization**

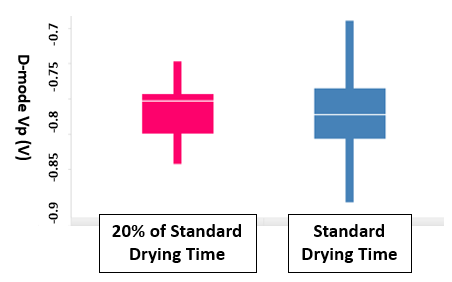
During the initial release of a D-mode pHEMT product, diesort test yield was found to be low due to high Vp. As shown in Figure 2, a diesort wafer map showed a typical “wet” staining pattern on wafers with high Vp.

Since polymeric dry etch residue could be formed at the gate contact area after oxide/nitride removal, effective plasma oxygen and wet cleans are critical to make good gate metal contact. Therefore, oxygen plasma etch and wet cleans were investigated as potential root causes of this high Vp issue.



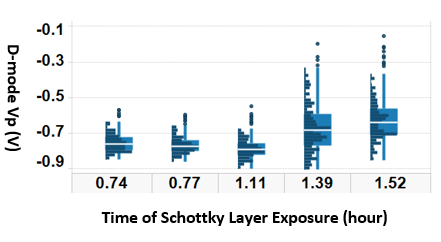
**Figure 2. Diesort wafer map of low switching current related to high VpD. “Red” regions are failing die.**

Based on the wet staining pattern, one proposed model was water attacking and etching the epi (Schottky AlGaAs) layer during the wafer drying step which followed the wet preclean. Drying time experiments were conducted, and the results are shown in Figure 3. Standard and reduced drying time splits were compared and the results showed that the wafers which were dried for shorter duration (20% of Standard) did not demonstrate a significant Vp shift. Incomplete drying was not the root-cause of this high Vp issue.



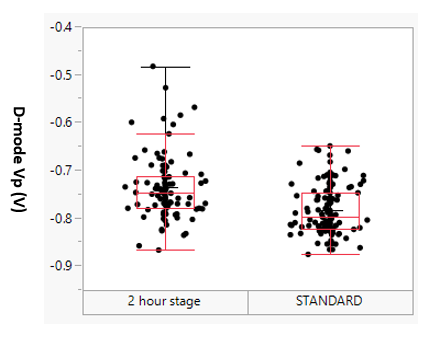
**Figure 3. Pinch-off voltage vs. the drying time.**

Another hypothesis was that the root cause of this Vp variation was oxidation of the Schottky layer. Extended data analysis indicated that the wafers with high pinch-off voltage had longer wait times (waiting time before or after processing) at the oxygen plasma etch step. The single-wafer oxygen plasma etch tools have no vacuum load lock, and all wafers are exposed to air during wait times both before and after processing. As shown in Figure 4, if the wafers have less than 1.1 hours of wait time, Vp variation is small and within control. With longer wait times, significant Vp shift is observed. The processing time for the oxygen plasma etch was the same for all wafers. It was found that the wait time difference was due to the differences in wafer unloading time after the plasma etch process. During this post-process waiting time for unloading the lot, the Schottky layer was exposed to air.



**Figure 4. Pinch-off voltage vs. the time Schottky layer exposed to air at the oxygen plasma etch step.**

Further time control experiments confirmed this failure mode. The results in Figure 5 show that the wafers exposed to atmosphere for 2 hours after oxygen plasma etch and prior to wet clean had Vp shifted by roughly +50 mV compared to the case where the wafers were returned to a runbox immediately after unloading from the oxygen plasma etch equipment.



**Figure 5. Controlled staging time experiment indicated 2 hours in air shifted Vp mean by +50mV.**

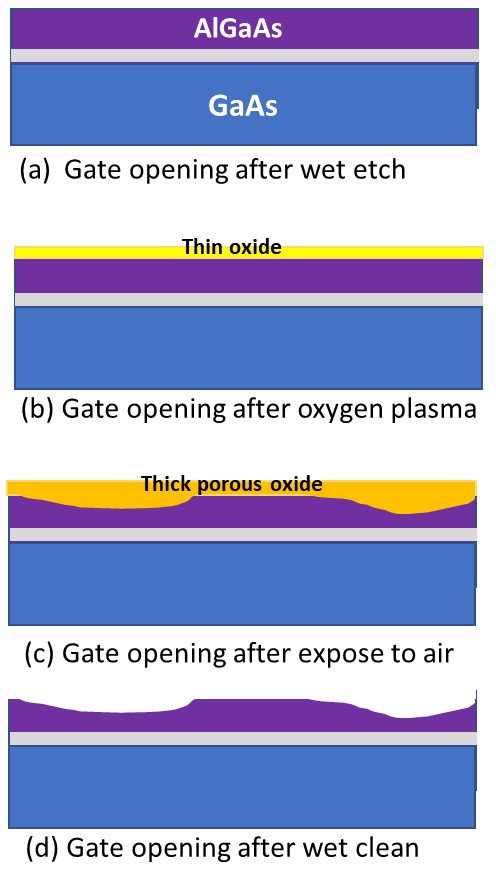
To understand this Vp increase, STEM images of affected transistor gates were taken. As shown in Figure 6 (b), a curved/wavy gate Ti / AlGaAs interface is observed for the wafers exposed to air for >2 hours at oxygen plasma etch. The control wafer exposed to air for 70min had straight Gate Ti / AlGaAs interface, shown in Figure 6(a).



1. **70min in air; (b) > 120min in air**

**Figure 6. (a) 70min in air, straight Gate Ti / AlGaAs interface, Vp Avg = -0.88V, STDEV=0.05V (b) >120min in air, curved/wavy Ti / AlGaAs interface. Vp Avg = -0.62V, STDEV =0.13V**

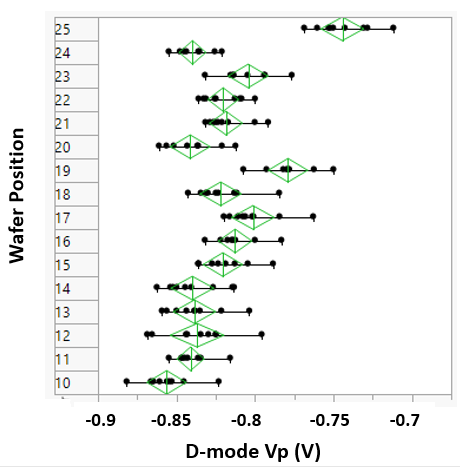
A thin uniform oxide film should form after oxygen plasma etch. When exposed to air, the oxide layer gradually grows non-uniformly by reacting with oxygen and moisture. After the wet clean, this non-uniform oxide layer is removed and produces a non-uniform AlGaAs layer as illustrated in Figure 7. This reduces the effective thickness of AlGaAs Schottky layer, causing Vp to shift higher. The “wet staining” failure pattern observed on the wafer map is the direct result of the non-uniform oxidized Schottky layer removal by wet clean.

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**Figure 7. Model of Schottky layer oxidization and porous oxide removal after wet clean leaving a wavy/curved AlGaAs layer. (a) Gate opening after wet etch exposes the Schottky AlGaAs layer; (b) A thin uniform oxide forms after oxygen plasma clean; (c) A thick porous oxide film forms after AlGaAs is exposed to air for longer times; (d) After wet clean, the porous oxide is removed, producing a non-uniform AlGaAs layer.**

**II. High Pinch-off Voltage: Wet Sink Last Wafer Effect**

Lot-to-lot Vp variation was reduced after restricting the Schottky layer air exposure time. This improvement then allowed a single wafer effect within the lot to be observed. A single wafer with high Vp was found to be the last wafer in the wet preclean tank. Wafer ordering experiments indicated Vp was higher for the wafer in the top slot in the cassette (slot 25) than the rest of the lot (Figure 8), which was then confirmed on multiple lots.

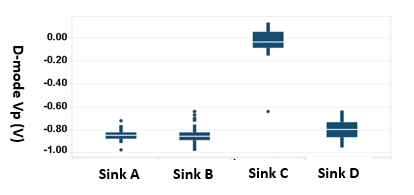


**Figure 8. Wet clean last wafer effect.**

We believe this single-wafer Vp shift is due to the absence of a wafer above slot 25 in the wet sink. This difference in the wet cleans exposure environment of the wafer in the 25th slot changes both the amount and uniformity of AlGaAs removed for this one wafer. Based on these results, sink cassettes were modified to 26 slots, with a dummy wafer in slot 26. This change prevented the non-uniform etching and single-wafer Vp shift.

**III. High Pinch-off Voltage: Sink Chemistry and Metal Contamination Effect**

Multiple wet clean sinks have been tested for the gate process, and we have found significant Vp shift for the wafers processed in a certain wet clean sink. As shown in Figure 9, Vp increased from nominal, negative values to nearly 0 for the wafers processed through sink C. That particular sink was also used for metal cleaning processes, and it is believed that cross-contamination caused Vp to increase in this case. When the AlGaAs Schottky layer is contaminated by metal, the pinch-off voltage characteristic changed from depletion mode, approaching values typical of enhancement mode.



**Figure 9. Effect of wet preclean chemistry and metal contamination.**

CONCLUSION

In this paper, we discussed the effect of processing variation on the pinch-off voltage of depletion-mode pHEMT devices. D-mode Vp lot-to-lot and wafer-to-wafer variation can both be greatly reduced? by controlling wafer cycle time at oxygen plasma etch, preventing metal contamination in cleans sinks and adding a 26th “dummy” wafer to sink cassettes.

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ACRONYMS

pHEMT: pseudomorphic High-Electron Mobility Transistor

VpD: Pinch-off Voltage for Depletion-mode FET

STEM: Scanning TEM