Wafer-Level Packaging for Electronic RF Systems Using GaN Technologies

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## **Abstract**

**The main objective of the Covered Gallium Nitride (CoGaN) project is the demonstration of the electrical performance of a GaN HPA in a frequency range between 25 GHz and 40 GHz with a maximal output power of 5 W in a chip scale packaging technology for 5G applications. In addition, requirements are existing for reliability testing at THB condition of 85°C/85% rel. humidity. In this work a test vehicle circuit with a pre matched 1 mm transistor is used for showing the process feasibility.**

## Introduction

In this paper two basic concepts are described for wafer level packaging (WLP). Concept A (Fig. 1) applies a BCB and a glass passivation. The MMIC is fully encapsulated by the BCB and the top glass layer.

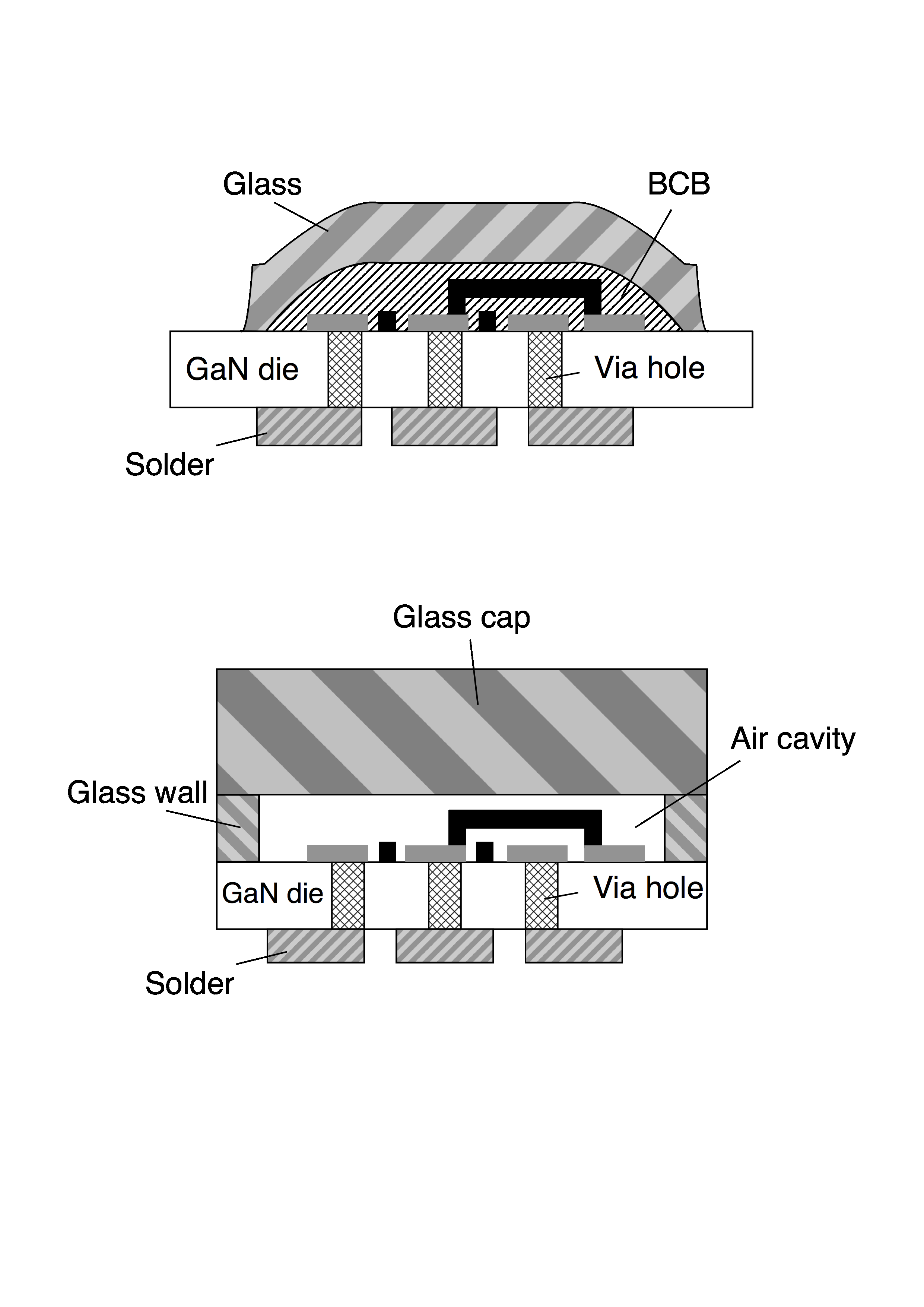


Fig. 1: Concept A – BCB & glass passivation

In case of concept B (Fig. 2) an air cavity package is realized using glass deposition of walls with subsequent wafer bonding techniques for a hermetic closure of the package. The electrical connection of the system is accomplished with a hot via approach that is connecting signal and ground contacts from the backside of the wafer by through wafer via holes to the front side of the chip. Either solder layer deposited on metal contacts on to backside or solder balling provides the interface to the system module.

The final hermitically sealed and small sized WLP MMIC product in both concepts shall enable the assembly on a PCB board without any additional packaging. This will provide a significant cost benefit.

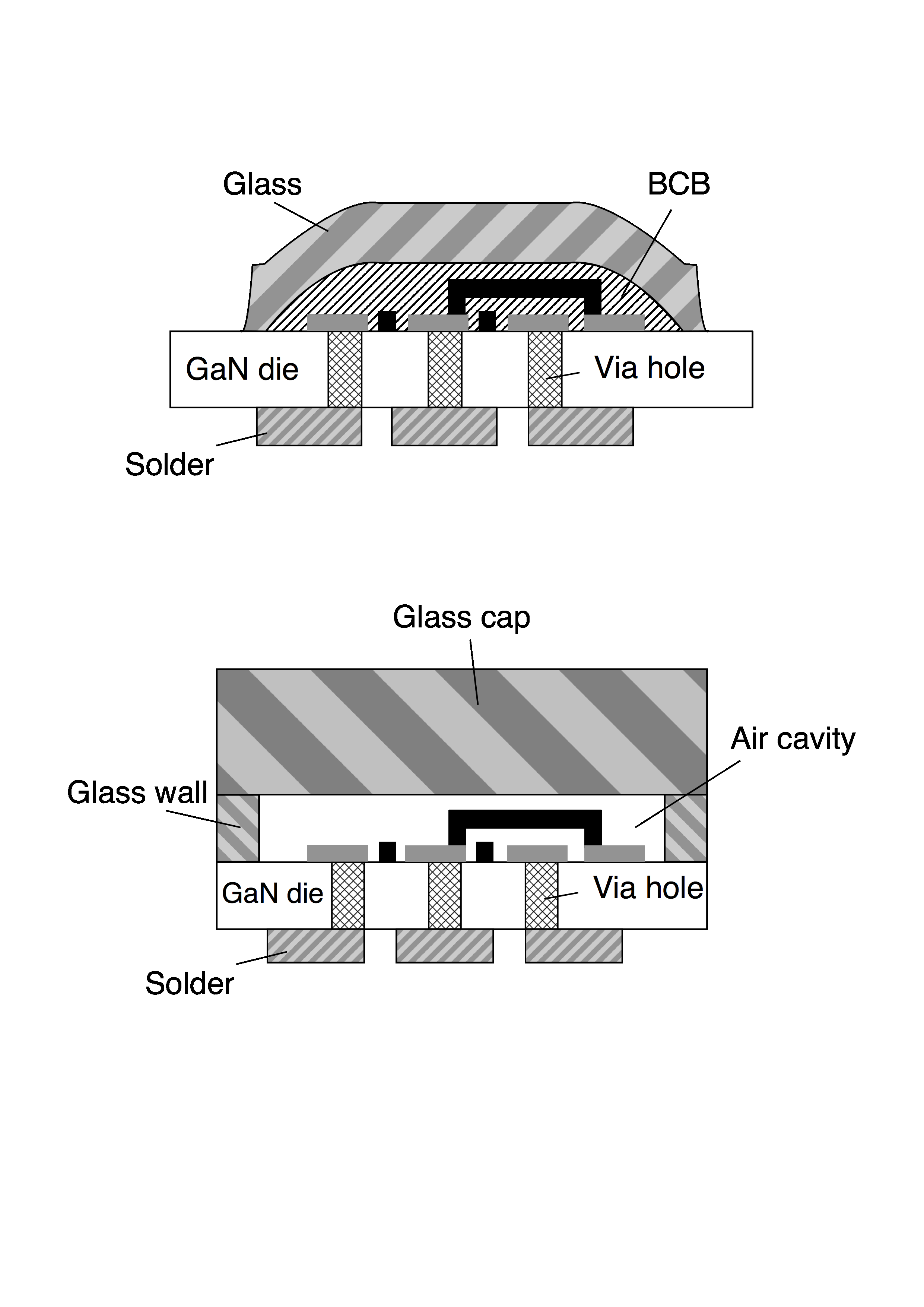


Fig. 2: Concept B – Hermetic air cavity package

Both wafer level packaging approaches are applied on the GH15 technology of UMS. This technology is a 150 nm gate GaN HEMT technology providing a power density of 4.0 W/mm and application up to 35 GHz. Aside from the humidity testing, it is mandatory to investigate the impact of the WLP on the electrical performance of the technology. The following paragraphs describe the process flows and results for both WLP concepts.

## Process Description

The innovation of this work is the application of the glass evaporation process by PVD technique. MSG Lithoglas offers a unique glass thin film deposition technology with uses in different fields of applications like MEMS or the packaging of medical devices and opto-elec­tronic semiconductors.

In the following sections the two different process flows are described for the WLP concepts.

*Concept A*

In concept A the material BCB – (Benzocyclobutene) is used for the first passivation layer of the front side finished 4-inch wafer of GH15 technology (Fig. 3). The BCB is coated using a resist coater with a subsequent soft bake. The polymerization degree up to 75-100% is achieved in a curing process. In reference [1] a more detailed description about the BCB structure can be found. In the next step, the BCB has to be cleared inside the saw line. A lithography soft mask is applied for a subsequent dry chemical etch process applying SF6/O2 etch gas chemistry. Due to the deposition properties of the evaporated glass it is mandatory to process a very shallow and positive BCB slope for the final glass coverage of the complete device. The positive slope can be achieved by applying a resist reflow bake after the resist development. The anisotropic dry chemical etch transfers the reflowed resist slope into the BCB. The etch process has to avoid trenching effects and surface roughness. Each parasitic topology can lead to incomplete closure of the glass layer during deposition.

Before glass deposition another lithography level is required for the lift-off process that is applied afterwards. The glass layer that has a nominal thickness of around 20 µm requires a resist thickness of around 25 µm with adequate undercut. The lift-off is applied with state-of-the-art solvents.

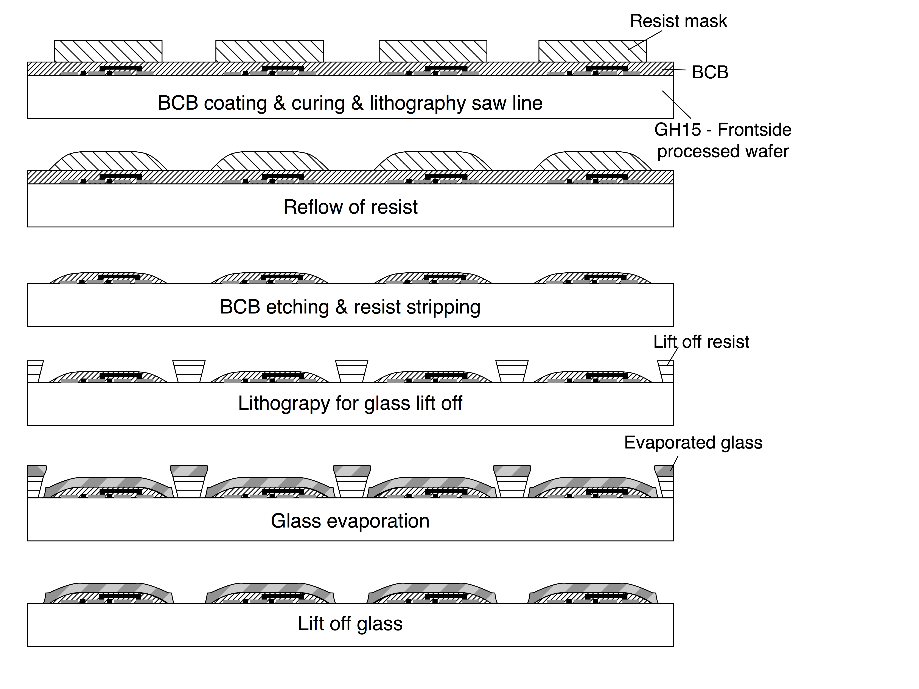


Fig. 3: Process flow WLP concept A

The devices are passivated and hermetically sealed after completion of the glass layer.

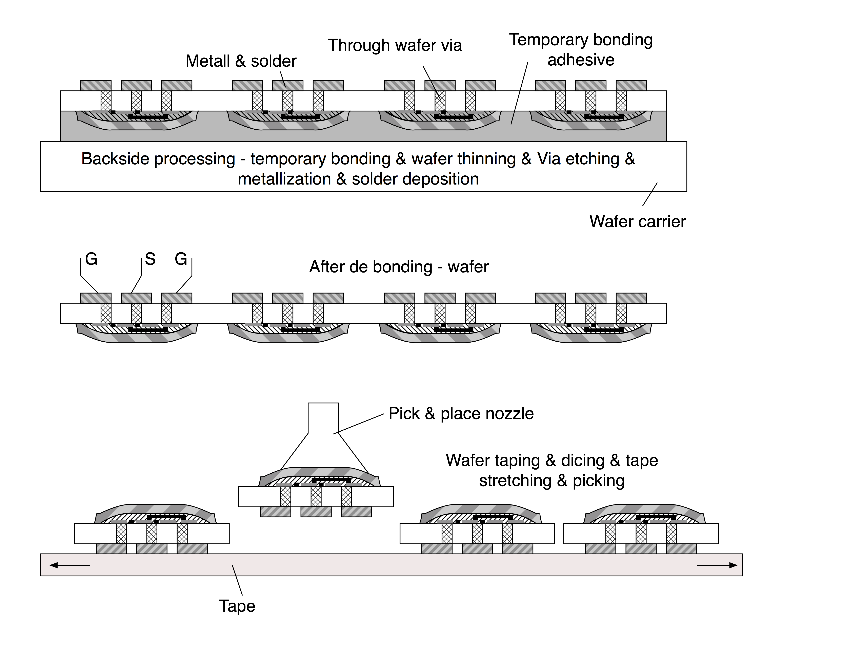


Fig. 4: Back Side process flow WLP concept A

For the back side processing (Fig. 4) that includes the wafer thinning and the via hole etching, the wafer is flipped over and temporary bonded on a wafer carrier using a temporary bonding adhesive. After the deposition of AuSn solder on top of the Au metallization the functional electrical test of the devices take place on a wafer prober from the backside upside down. RF characterization allows the extraction of S-parameters and output power. After die separation the fully packaged MMIC can be picked from the dicing tape.

## *Concept B*

In case of concept B a preparation of the glass cap wafer is necessary for the realization of the WLP packaged MMIC. At the first step the glass walls are built by lift-off on a separate glass wafer with adapted CTE to the SiC device wafer. In Fig. 5 the WLP process steps seem to be more simplified compared to the previous approach.

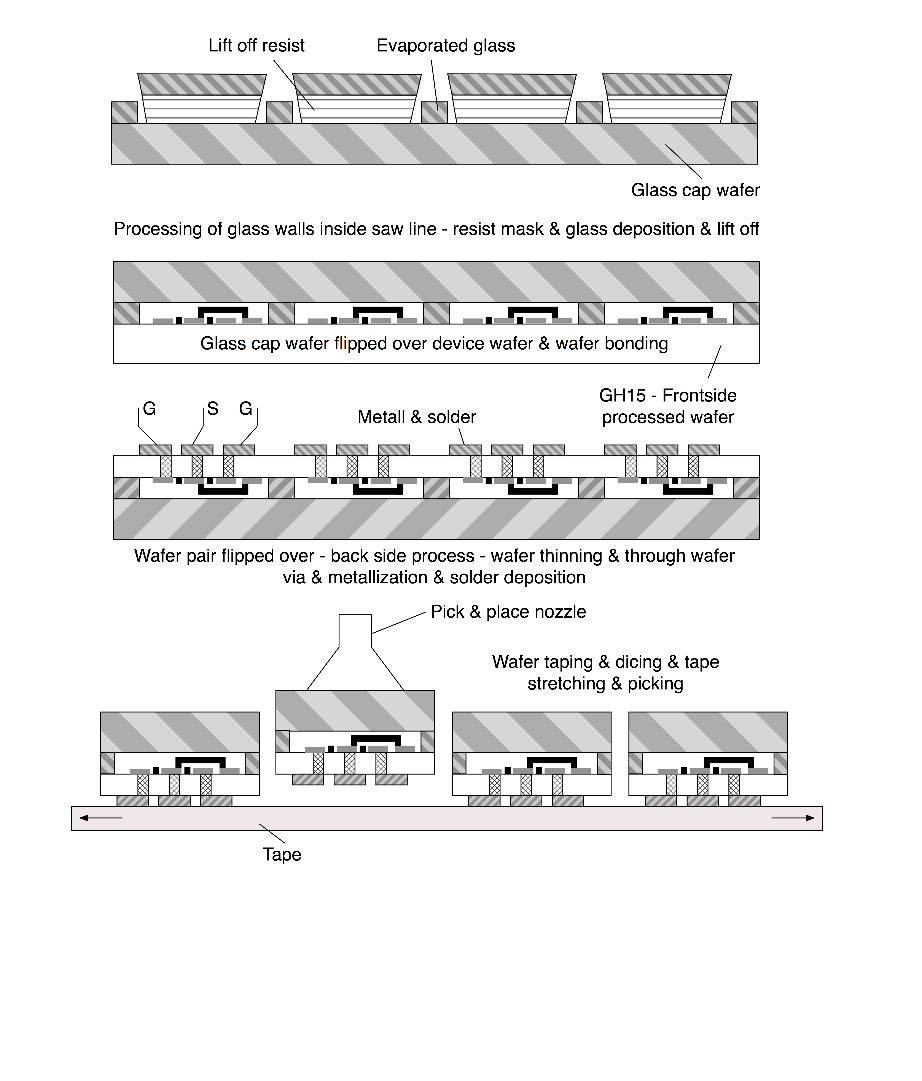


Fig. 5: Process flow WLP concept B

The usage of the glass cap wafer as carrier wafer for the backside process enables another opportunity for cost savings, as the steps of temporary bonding and final de bonding are no longer required. The glass cap wafer is flipped over and is permanently bonded on top of the device wafer. The top of the glass wall and the saw line build the bonding interface. The permanent bond has to withstand the shear forces of the wafer thinning process as well as the temperature budget of all backside process steps. Similar to concept A the same backside processes are applied for the electrical interconnection of the MMIC by through wafer via holes as well as the electrical functional test of the circuits. After the dicing a hermitically closed WLP packaged MMIC in air cavity can be picked. For concept B it is expected to have minor impact on electrical RF performance due to the air cavity approach compared to the BCB encapsulation at concept A.

## Process Results WLP

In both cases process development of single steps has been carried out prior to the start of the demonstrator runs. Based on existing processes optimization of some processes are needed to ensure the mechanical integrity of BCB and glass and an adequate permanent bonding force of glass to the device wafers saw line in case of concept B.

## *Concept* *A*

The challenge for the BCB & glass passivation is the complete coverage of the BCB slope as well as the mechanical integrity of both materials. The BCB shrinkage during curing applies a strong tensile stress to the wafer. The glass shows a strong compressive stress. A simplified on-wafer thermomechanical cycling TMCL test setup should reveal the process variant with fully closed glass layer on top of BCB and no crack of the glass on top and edge of the chip. The DOE comprises the variation of the BCB slope angles of 20°, 30° and 50°. For each BCB slope a 3 µm and 10 µm thick glass deposition is applied. Fig. 6 shows SEM images of the chip edges in tilted and cross section view after the on wafer TMCL test.

|  |  |  |  |
| --- | --- | --- | --- |
|  | 20° | 30° | 50° |
| 10 µm thick glass |  |  |  |
|  | trenching  glass  BCB |  |
| 3 µm thick glass |  |  |  |
|  |  |  |

Fig. 6: Glass & BCB optical quality after TMCL (10x 25°C 🡪150°C @ 2 min) at 20°, 30° and 50° BCB slope at 3 and 10 µm glass thickness

BCB slopes less than 30° show very good conformity and a closed layer of glass. However, cracks occurred on BCB slopes greater than 20° at the die edges and corners. Glass thickness of 10 µm shows lower occurrence of cracks than 3 µm. As outcome the BCB slope angle was defined less than 20° at a glass thickness greater than 15 µm for the next process runs.

The first feasibility process run of the BCB glass approach is applied on UMS GH15 technology. The mask consists of two RF test circuits called DEC1 (1.9 x 2.2 mm) and DEC2 (1.9 x 4.8 mm) with a pre matched 1mm transistor device and a DC test vehicle for humidity tests with a size of 4.8 x 4.8 mm.

The BCB slope of less than 20°C is achieved by the temperature adjustment at the etch mask reflow step. Two glass evaporation process variants are applied for the runs comprising different level of compressive stress. After the finishing of the front side process no optical yield loss due to glass cracks could be identified for the processed wafers. The optical view as well as the SEM inspection show a high quality of the BCB and glass processing steps as shown in Fig. 7.

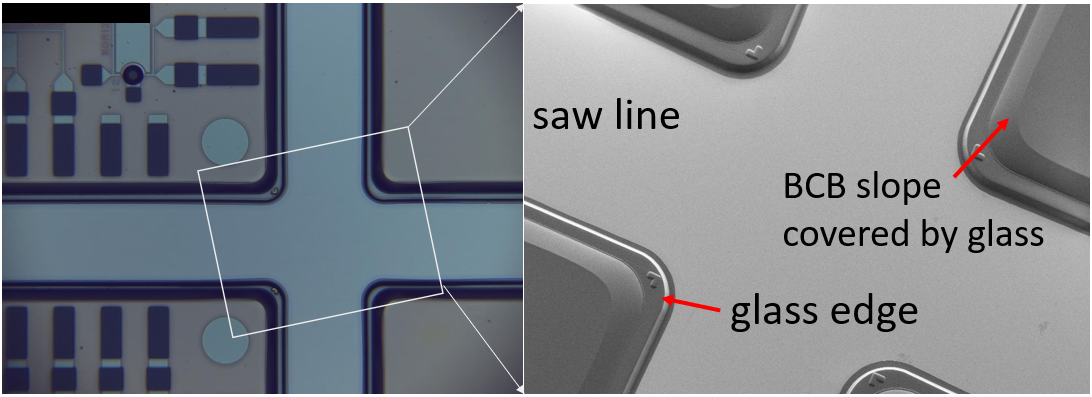


Fig. 7: Inspection of saw line clearance after glass lift-off

The selective solder deposition is not applied for the first runs. It was decided to apply a solder ball assembly for the WLP dies later onto the AlN substrate boards. Optical yield determination with regards to glass cracks after completion of back side process shows for the high compressive stressed wafer 91% yield for DEC1 and 78% yield for the test vehicle chip. As large the die as higher the impact is on the optical yield. The wafer with lower compressive stressed glass showed 100% optical yield regarding cracks. Due to the very low process statistics glass cracks could be a weakness that has to be further investigated for WLP concept A.

In Fig. 8 the DEC1 device is shown with the view on front and back side. This circuit is used for the evaluation of the electrical functional yield of the WLP process flows. As the probing is applied from the back side of the wafer the prober marks could be seen on top of the backside metal layer.

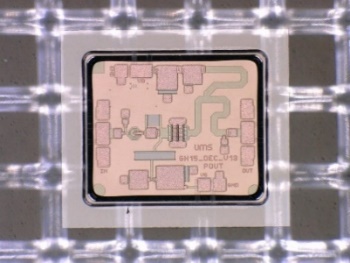
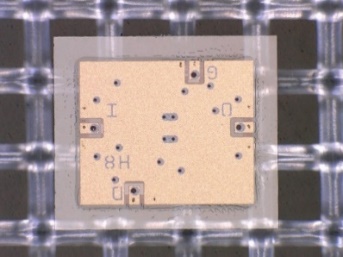
 

Fig. 8: top view of DEC1 (left) and on backside (right)

Fig. 9 shows the output power Pout and gain parameter during power sweep at 9 GHz. The on wafer electrical test after the backside process showed 100% function of the 21 DEC1 devices tested. The error bars show the standard deviation of pout and gain of all devices under test. One outlier could be explained by a weak ground connection at the input.

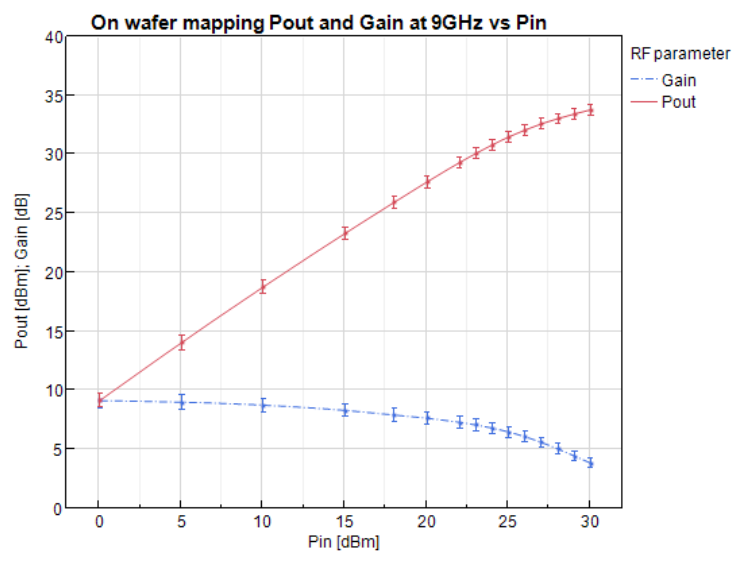


Fig. 9: Pout and gain vs power sweep at on wafer probing from back side with standard deviation error bar

After dicing and picking a polished cross section is performed to show the full WLP circuit.



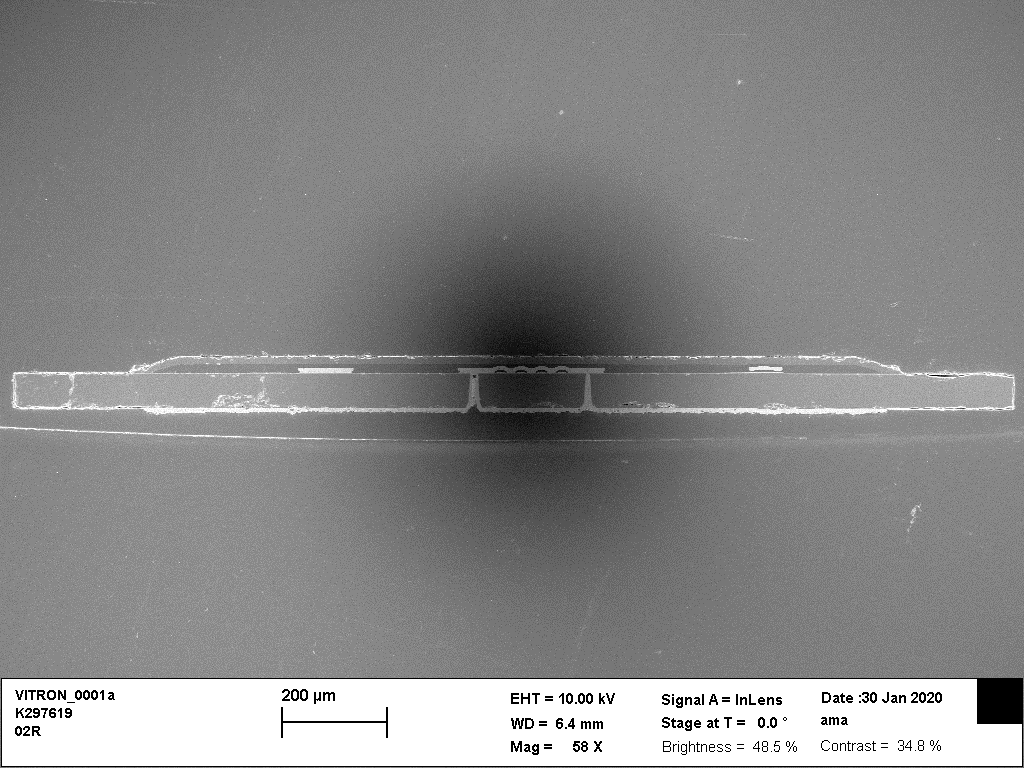


Fig. 10: Cross section of DEC2 device –input G-S-G pads with via interconnect (top view) and transistor topology with air bridges (bottom view)

The physical failure analysis shows preparation artefacts with material that is broken out during the polishing. However, the cross sections show the Ground-Signal-Ground interconnection from the back side in Fig. 10 and the cross section through the transistor topology 8x125µm device of the DEC2 circuit.

## *Concept B*

In case of concept B, the main focus was put on the permanent bonding of glass to the device wafer. After comparison of various bonding and welding techniques the final decision was to apply anodic bonding. Anodic bonding requires conducting substrates that enable the exchange of ions at the bond interface. GaN on SiC EPI material reveals too high isolation properties for this process step. In order to come over this constraint additional process steps have to be developed for enabling a final anodic bond. First the bonds were performed on full sheet wafers in order to see the process feasibility. After then the first device wafers were successful bonded as shown in Fig. 11.

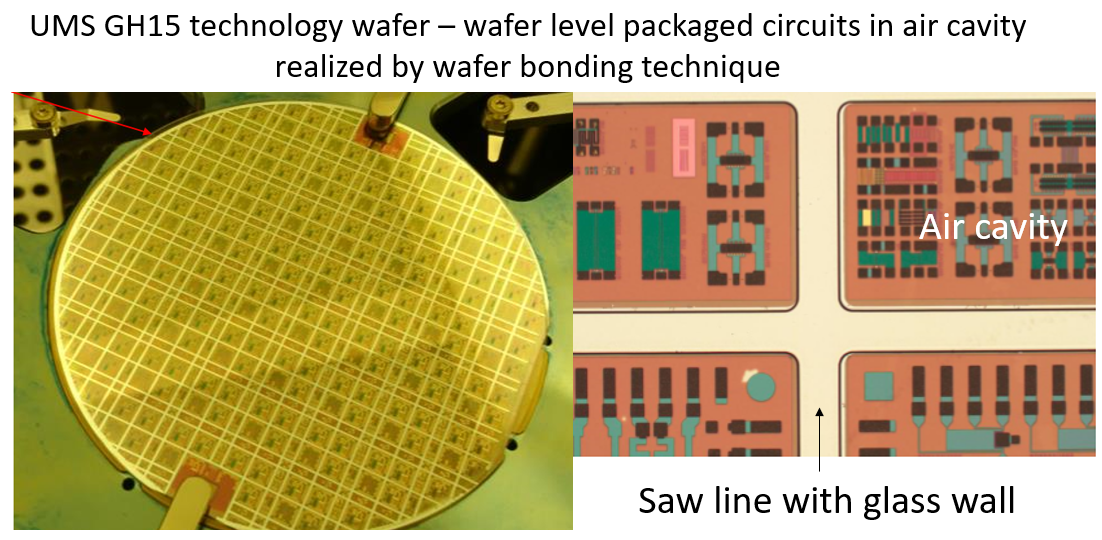


Fig. 11: Glass wafer with glass walls permanent bonded to a stacked wafer pair

After the definition of the permanent bonding technique some steps of the backside processes were applied on full sheet bonded wafers. The critical process steps are wafer thinning, via hole etching and wafer dicing which the permanent bonding interface has to withstand. In case of these process steps the full sheet bonded wafer showed no process issues.

## Conclusion and Outlook

The process results of the concept A showed a good level of confidence. Process feasibility has been shown from wafer processing until the final assembly of the test vehicles and the DEC1 test circuit. The next step is the process demonstration of a 2 stage 30GHz power amplifier.

## Acknowledgements

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## References

[1] H. Stieglauer, et al., *Via etching in BCB for HBT technology*, 2008 GaAs MANTECH Technical Digest, pp. 97-101, April 2008.

## Acronyms

WLP: Wafer Level Packaging

CoGaN: Covered Galium Nitride

THB: Temperature Humidity Bias

TMCL: Thermo Mechanical Cycling