Investigation of RF Performance of InGaP/GaAs HBT Power Stage with Flip-Chip Bumping Technology

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Abstract

In this paper, we present 3.5 GHz HBT power cell device by using WIN's 5th generation HBT process and flip-chip bump technology. Small-signal and large-signal characterizations are investigated and analyzed through the measured results within different thickness of evaluation boards (EVB). Through a proper EVB design, the flip-chip bumped power cell exhibits a remarkable improvement on MAG/MSG, and it presents low surface temperature behavior. The maximum output power of 32 dBm can be achieved at supply voltages of 3.4 V and 4.3 V, and the maximum PAE performances are close to 68 % under 1-tone large-signal test.

In order to further realize the linearity performance relative to the grounding inductance caused from the via hole design of EVB, ACPR measurement was employed based on LTE modulation signal and loadpull system. With thermal IR measurement and calculation of thermal resistance, the performance optimization between small-signal and large-signal characterizations can be approached for ultra-high-band (UHB) HBT PA design.

INTRODUCTION

The demands of high power and better PAE performance are becoming necessary to face 5G sub-6GHz applications. Higher operating frequency and thermal dissipation due to highly integrated assembly become a challenge to achieve compact size package for front-end chip or multi-band/multi-mode PA module. To improve the issues, flip-chip technology has being widely used in front-end module and millimeter-wave chip design [1, 2]. Flip-chip technology provides the benefit of low parasitic inductance/capacitance on interconnection to reduce the high-frequency transmission loss compared to wire bonding [3]. However, low loss characteristic is relying on a proper PCB design and bump attachment [4]. Grounding path and trace arrangement for signal transmission seriously affect signal discontinuity and its quality.

In addition, thermal effect of semiconductor power device always dominates PAE performance. Flip-chip package can significantly improve thermal dissipation by using the substrate with high thermal conductivity [3, 5]. Since thermal behavior also determines device reliability and linearity performance especially for handset RF PA module, investigation of thermal distribution between wire bonding and flip-chip technologies and development of thermal model are necessary in HBT PA design, providing a detail thermal behavior [6, 7].

In this paper, a HBT power cell based on flip-chip bump technology was mounted on a well-designed EVB for 3.5 GHz PA applications. To optimize device performance involving thermal effect and grounding inductance of EVB, characterization of 2880 μm^2 HBT power cell has been investigated by DC, small-signal, and large-signal measurements. The device presents output power of 32 dBm and high PAE over 65 % with improved small-signal gain. LTE linearity performance is also investigated to figure out a correlation depending on the grounding inductance of EVB.

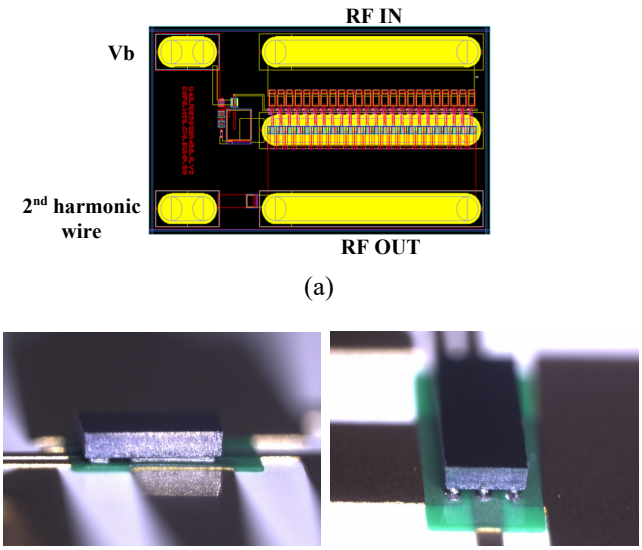


Figure 1. 2880 μm^2 HBT power cell was mounted on an evaluation board with bump solder mask; (a) layout of power cell (1.3×0.72 mm^2) and (b) side view of flip-chip die mount.

FLIP CHIP BUMPING

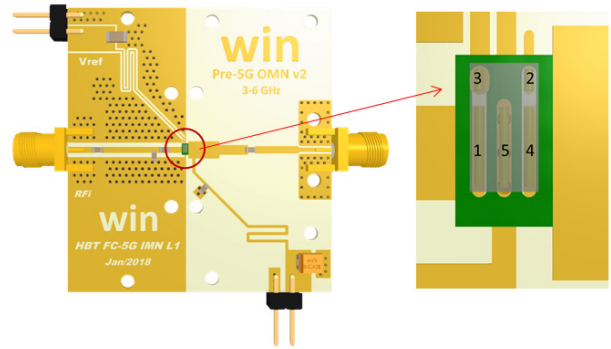
This work was done with WIN's 5th generation InGaP/GaAs HBT process. The 5th generation HBT process, so called HBT5, includes two interconnection metal layers ($M_1$and M_2) and a PBO layer as the dielectric layer between M_1 and M_2. Using a patterned PBO island instead of using global polyimide as an interlayer dielectric can provide better mechanical and moisture protection. The thicknesses of the Au metal interconnect layers are 1 µm evaporated and 4 µm plated for M_1 and M_2, respectively. MIM capacitors with unit capacitance of 570 pF/mm^2, stacked MIM capacitors with unit capacitance of 980 pF/mm^2, and thin film resistors with sheet resistance of 50 Ω/sq can be used for MMIC designs. The copper pillar bump process was subsequently manufactured to provide 40 µm of plated copper and 30 µm of plated Sn cap metal for flip-chip mounting utilizing a solder reflow process.

DC AND SMALL-SIGNAL CHARACTERIZATION

In order to demonstrate WIN's flip-chip technology applied on 3.5 GHz HBT PA design, we are now investigating DC and RF small-/large-signal performances by a power cell with emitter area of 2880 µm^2. The layout of the power cell was modified carefully from typical design for achieving 4G/5G high-band (HB) and ultra-high-band (UHB) applications. Fig.2 exhibits the power cell layout and its side view of flip-chip die mount, where device periphery of unit cell is 120 µm^2. The EVB is customized design with bump solder mask. The EVB not only prevents Sn spillage for die mounting, it also provides optimized input/output impedance matching networks and DC feeding paths for measuring RF performance as shown in Fig. 3.

In practice, flip-chip bump technology can improve thermal dissipation and result in a better thermal runaway effect. To understand thermal characteristic of HBT power cell, we make a performance comparison through wire bonding and flip-chip mounting. Fig.4 shows *I-V* curves of 2880 µm^2 power cells. It is apparent that current collapse can be improved for flip-chip mounted power cell when increasing V_{CE} and I_{CE}.

EVB design is not only affecting thermal dissipation for RF power device, it contributes parasitic inductance to determine grounding path due to high-frequency characteristic of via hole. Height of bump, thickness and numbers of grounding via hole of EVB are also the factors and must be optimized to reduce parasitic effect for UHB PA design. Fig. 5 shows MAG/MSG characterization at 3.4V with I_{CQ} of 1.67 kA for HBT power cells mounted on different PCB thickness, 6 mil and 32 mil. Theoretically, grounding inductance extremely dominates MAG/MSG characterization especially for high-frequency operation. In this experiment, the power cell mounted on 6-mil EVB exhibits a significant improvement on MAG/MSG, where the turning frequency is extended from around 2.7 GHz to



NO.	Name	Description
1	RFIN	RF input port
2	HC	2nd harmonic cancel tuning
3	VREF	DC bias input port
4	RFOUT	RF output and DC bias output port
5	GND	Ground port

Figure 2. Evaluation test board design for testing 2880 µm^2 HBT power cell. Inset table shows the definition of DC and RF ports.

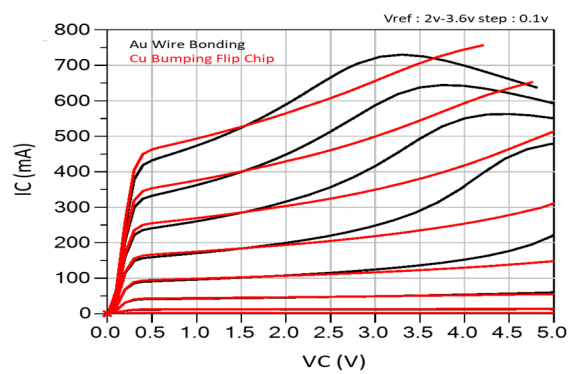


Figure 3. V_{CE}-I_{CE} curves comparison of using wire bonding and flip-chip bump.

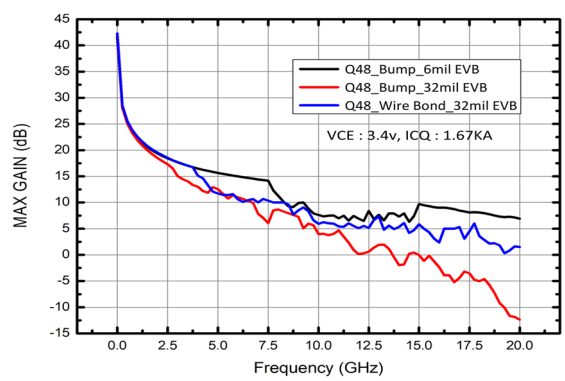


Figure 4. Small signal MAG/MSG comparison for flip-chip bump and wire bonding devices within EVB thickness of 6 mil and 32 mil.

7.5 GHz. It means that 6-mil PCB is appropriate for UHB PA design due to the concern of small-signal available gain. Through EM simulation and small-signal analysis, the grounding inductance of the EVB can be reduced from 190 pH to 26 pH at 5.0 GHz as shown in Fig. 5.

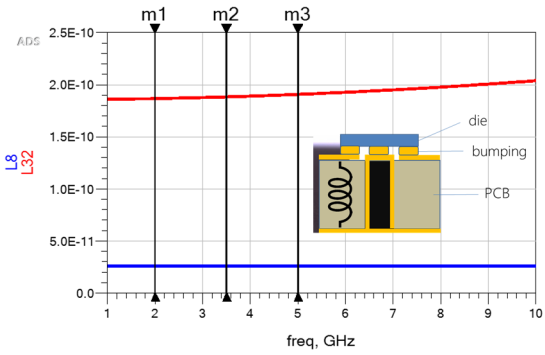
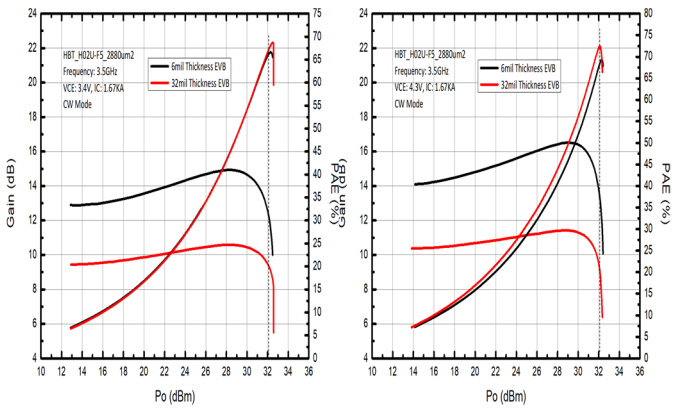
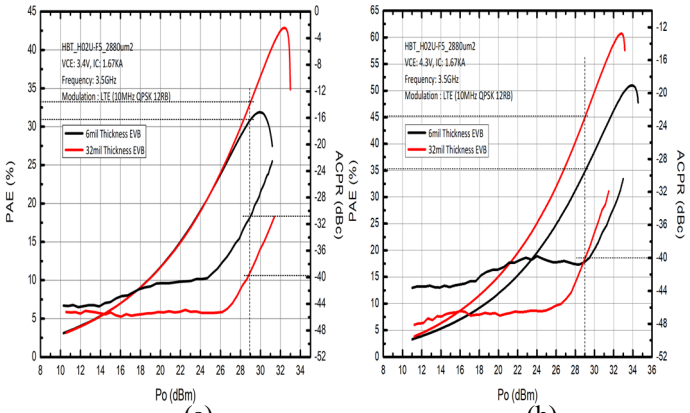


Figure 5. Simulated equivalent grounding inductances for 6-mil and 32-mil EVB thickness.



(a) (b)

Figure 6. 3.5 GHz power performance result of flip-chip bumped power cells at (a) V_{CE}= 3.4 V and (b) V_{CE}= 4.3 V.



(a) (b)

Figure 7. 3.5 GHz linearity performance at P_{out}=29 dBm (LTE uplink 10 MHz QPSK 12RB): (a) V_{CE}= 3.4 V and (b) V_{CE}= 4.3 V.

RESULT AND DISCUSSION

Through the DC and RF measured analysis, the HBT power cell with using flip-chip bump and 6-mil EVB exhibits characteristic benefit. To achieve the best output power and ACPR characteristics for either APT or ET applications, the power cell was measured by loadpull system. Furthermore, thermal characteristic is also a key factor to approach a package/module-level evaluation. For a better PAE and linearity performance, thermal resistance must be extracted by thermal measurement.

1) Power Performance and Linearity Evaluation

To investigate power gain performance and achieve high linearity requirement, tuning maximum output power was adopted for loadpull measurement. Fig. 6 demonstrates 3.5-GHz power performance corresponding to 6-mil and 32-mil EVB at 3.4 V and 4.3 V, respectively. It is obvious that the device mounted on 6-mil EVB at the same output power of 32 dBm presents a gain of 13.5 dB performance with PAE of 72 % under V_{CE}=4.3 V. Compared to the device on 32-mil EVB, it has almost 3.8 dB improvement in small-signal gain.

According to the technique of linearity improvement, emitter feedback can optimize linearity characteristic by embedding an emitter inductor (L_E) [8]. Since there are different grounding inductances between 6-mil and 32-mil EVBs, it would affect linearity performance specifically. To demonstrate Fig. 7 shows ACPR measured results for 3.4 V and 4.3 V. The device mounted on 32-mil EVB shows a better ACPR performance with PAE of 33.5 % at either low P_{out} or high P_{out} under V_{CE}= 3.4 V operation. However, it only presents large-signal gain of 8.2 dB. As the predication in [8], high equivalent L_E results in linearity improvement even if it has lower small-signal gain. As to the device on 6-mil EVB, it is can't pass -40 dBc criteria at P_{out}=29 dBm. Increasing V_{CE} from 3.4 V to 4.3 V can further improve ACPR from -30.3 dBc to -40.6 dBc. Among the measured results, the inductance on grounding path must be allocated carefully to be a tradeoff for small-signal gain and ACPR performances. The power performance at P_{out}=32 dBm is shown in Table I, and LTE ACPR results at 10 MHz offset for linearity evaluation at P_{out} =29 dBm is listed in Table II.

2) Thermal IR Measurement and Thermal Resistance

Due to having high current raising behavior on the wire bonding device, thermal IR measurement was used to further inspect surface temperature under designated dc power dissipation. Fig. 7 shows temperature distributions of the power cells, where the highest temperature presents at center of power device. The maximum hot spots of flip-chip mounted and wire bonding cells are 140 ºC and 180 ºC, respectively, exhibiting temperature difference of 40 ºC under a power dissipation of 2.0 W. The result presents an evidence of heat dissipation improvement by using flip-chip bump technology as prior published references.

In order to figure out R_{th} value including thermal effect from EVB, surface temperatures depending on different P_{diss}

TABLE I MEASURED LARGE-SIGNAL PERFORMANCES

P_{out} @32 dBm	3.4 V		4.3 V	
thickness	6 mil	32 mil	6 mil	32 mil
Gain (dB)	12.5	9.5	13.5	9.5
PAE (%)	66	66.7	68	72
I_{CC} (mA)	612	662	518	448

TABLE II LTE ACPR PERFORMANCES

P_{out} @29 dBm	3.4 V		4.3 V	
thickness	6 mil	32 mil	6 mil	32 mil
Gain (dB)	9.2	8.2	12.5	10.6
PAE (%)	31	33.5	35	45
I_{CC} (mA)	676	600	494	375
ACPR (dBc)	-30.3	-40.3	-40.6	-40

were measured between flip-chip and wire bonding devices as shown in Fig. 8. The result shows R_{th} difference of 21.6-°C/W

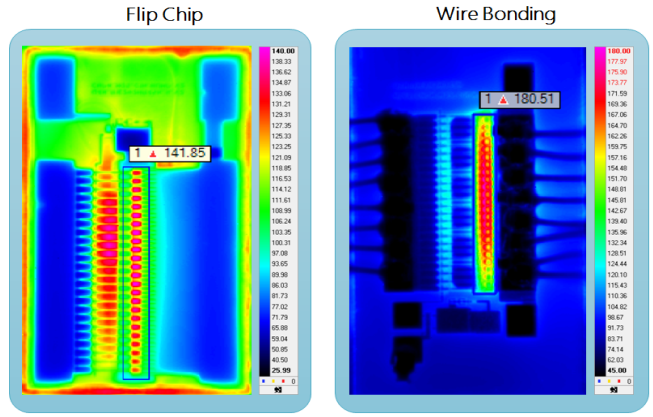


Figure 7. Thermal IR measurement for HBT power cells: (a) wire bonding and (b) flip-chip bump die mounts (V_{CE}= 3.4 V and P_{diss} = 2.0 W).

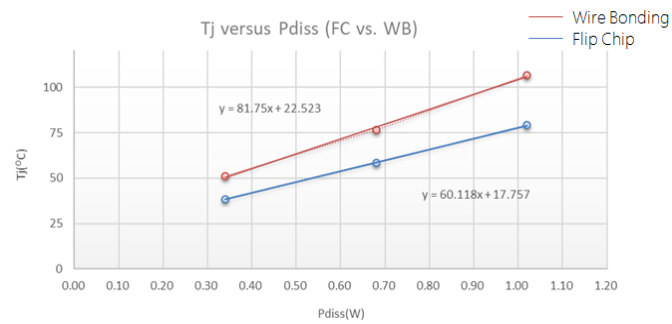


Figure 8. Calculation of thermal resistance at V_{CE}= 3.4V.

CONCLUSIONS

In this work, we demonstrate WIN's development of HBT5 process and flip-chip technology both can provide a favorable thermal characteristic and push the operating frequency up to UHB applications. Through the analysis of EVB design, grounding inductance can be optimized to determine large-signal performance. The significant device characterization will reduce complexity of die assembly due to the concern of thermal effect, and enhance design margin to develop sub-6 GHz power amplifiers.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
5G: 5th Generation Mobile Networks
Sub-6GHz: 5G Spectrum below 6GHz
PAE: Power Added Efficiency
ACPR: Adjacent Channel Power Ratio
APT: Average Power Tracking
ET: Envelop Tracking