Crystal Growth and Wafer Processing of 6" GaAs Substrates for Lasers

Tomonori Morishita

Sumiden Semiconductor Materials Co., Ltd., 1-1-1, Koya-kita, Itami, Hyogo, 664-0016 Japan
Phone: +81-72-771-3024, Fax: +81-72-771-0460, e-mail: morishita-tomonori@sei.co.jp

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Abstract

The market for lasers, especially vertical-cavity surface-emitting lasers (VCSELs), is growing rapidly. These applications utilize a large number of cavities, notably the use of VCSELs in array form. This leads to larger die sizes, which drive the economics of using larger diameter GaAs substrates.

In this paper we report the development of Si-doped 6-inch GaAs substrates for laser diodes (LDs) and the improvement of manufacturing productivity. GaAs crystals with low etch pit density (EPD) are obtained using the Vertical Boat (VB) crystal growth method. We have designed a 6-inch VB crystal growth furnace, and optimized growth conditions to reduce crystal defects and increase crystal length. We have also increased the productivity of the wafering process while maintaining the quality needed to for high device yield.

INTRODUCTION

VCSELs are expected to be key devices for several applications, including optical fiber communication, short distance area sensing, proximity sensing, infrared illumination, gesture recognition, and LiDAR. The VCSEL market is expanding rapidly. Some applications need two dimensional devices, such as VCSEL arrays. This drives larger chip sizes which in turn drives the need for larger diameter GaAs substrates. In 2016, VCSEL production was done mostly on 3-inch wafers. But the market has evolved rapidly.

This paper shows the development and the expansion of production technology for Si-doped 6-inch GaAs substrates for VCSELs. 6-inch wafers are produced with quality characteristics equal to or better than 3 inch wafers for key wafer characteristics such as EPD.

Figure 1 shows a graphical representation of the GaAs crystal wafer products of Sumitomo Electric Industries (SEI). Sumitomo Electric has a long history of manufacturing Si-doped 3-inch semi-conducting (S.C.) GaAs substrates with low EPD for LDs and carbon-doped 6-inch semi-insulating (S.I.) GaAs substrates for wireless communication devices.[1,2] Recent crystal growth technology development enabled us produce high quality 6-inch S.C. crystal suitable for laser applications. We followed this crystal development by also developing high volume production technology for 6-inch semi-conducting GaAs substrates, largely by applying techniques used for 6-inch semi-insulating wafers.

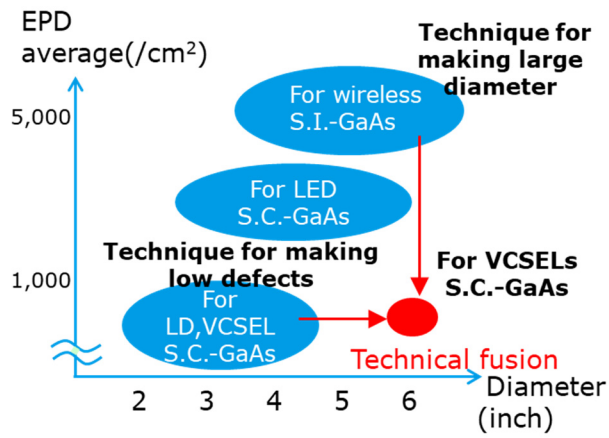

Figure 1. GaAs products of Sumitomo Electric, EPD vs diameter

THE CRYSTAL GROWTH PROCESS

In the early years of GaAs manufacturing, Sumitomo Electric mass-produced wafers for lasers using the Horizontal Boat (HB) crystal growth method, which was good for growing low EPD crystal. For wireless communication devices, we used the Liquid encapsulated Czochralski (LEC) crystal growth method to obtain large diameter crystals (Figure 2).

The HB method was not suited to making large diameter crystal, and the LEC method was not suited to making low EPD crystal. In the early 2000's, we developed production technology for the VB crystal growth method (Table 1).

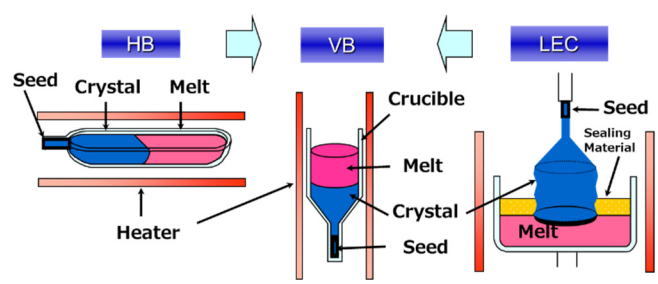

Figure 2. Evolution of GaAs crystal growth method

TABLE 1. COMPARISON OF CRYSTAL GROWTH METHODS

	HB	VB	LEC
Diameter	～2.5inch	2～8inch	3～6inch
EPD	Low	Very low	High

Using the VB method, we were able to mass-produce both low EPD crystal for 3-inch semi-conducting GaAs and long crystals for 6-inch semi-insulating GaAs. As we moved to develop long boule for laser diodes, we were able to draw on our existing technology for the production of 3-inch crystal for laser diodes and 6-inch crystal for wireless applications. We optimized the furnace design for large boules and low EPD growths. In the growth of a large diameter GaAs crystal, it is very difficult to control the thermal flow in both the lateral and vertical directions. Thermal flow control is crucial to keep an optimal, stable shape of the growth interface through the entire growth sequence. We further improved the growth technique and controlled thermal flow by using multiple zone heaters.

Crystal growth is carried out by filling the crucible with gallium, arsenic and silicon dopant. These materials are melted in a furnace, and the melt is then solidified starting from a seed crystal. The temperature in the furnace is controlled to maintain an optimum shape of the solid/liquid interface so that the in-plane variation of carrier concentration and EPD is reduced. The crystal is solidified while carefully controlling the furnace temperature at the optimum conditions. It is necessary to keep optimum temperature conditions from the early period of crystal growth to the latter period (Figure 3). To keep the optimal temperature conditions, the key parameter is the critical hot zone. We further improved control of the temperature profile by optimizing the number and the width of the main heaters. One of the advantages of the VB method is the ability to control the critical hot zone simply in one place, to stably produce a long crystal with precise temperature measurement at each furnace position while the crystal is moving.

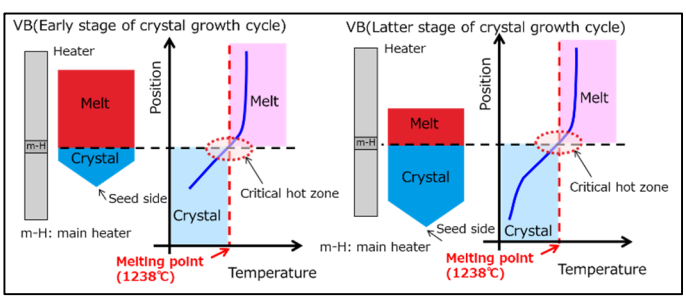

Figure 3. The relation between crystal temperature profile and crystal growth position

Figures 4 and 5 shows examples of EPD maps and carrier concentration distribution across the wafer of 3 inch and 6-inch GaAs substrates for laser diodes. The in-plane distribution of EPD and carrier concentration of a 6-inch substrate is equivalent to that of 3-inch substrate. We further believe that by optimizing the thermal environment, we can further lower the EPD 6-inch GaAs substrates.

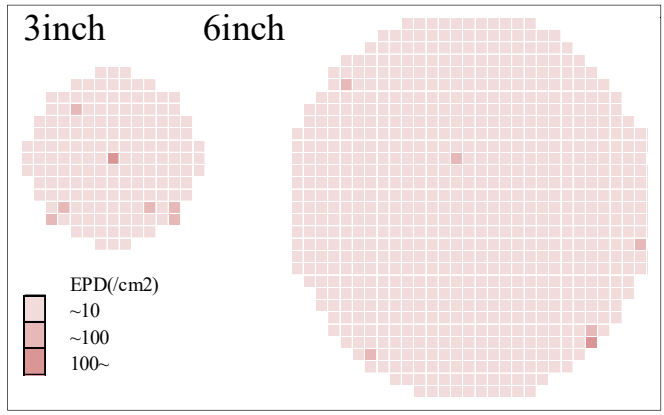

Figure 4. EPD maps for 3-inch and 6-inch S.C. GaAs substrates

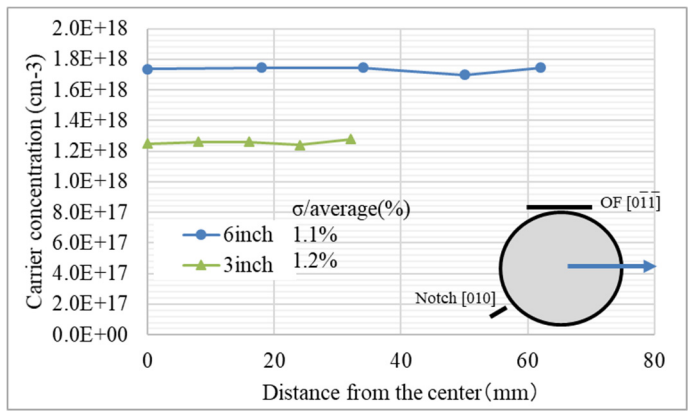

Figure 5. Carrier concentration distribution across 3-inch and 6-inch GaAs wafers

To keep EPD low, it is necessary to optimize and control the temperature precisely not only when the crystal is solidified but also when the crystal is cooling. The crystal growth sequence for 6-inch semi-conducting GaAs crystal takes more time than that for 6-inch of the semi-insutlating. This increases the production cost. So, we focused on the improvement of lot size and succeeded in developing a long VB-grown GaAs single crystal ingot for laser diodes. A longer crystal ingot yields more wafers from one ingot, reducing cost per wafer. We are also gradually reducing the furnace cost through the simplification of the structure. In addition, productivity per furnace is gradually increasing through incrementally larger lot sizes and yield improvement.

THE WAFERING PROCESS

Sumitomo Electric has accumulated a lot of experience for the wafering process of 6-inch from years of high volume

production of semi-insulating wafers. We were able to transfer much of the 6-inch process technology to the manufacturing of semi-conducting wafers. The wafer process is performed using a multi wire saw slicing (MWS) and double side polishing (DSP) and cleaning that is continuously improved for semi-insulating 6-inch GaAs wafers. The high precision surface orientation is maintained by managing the precision of the slicer. To reduce material loss, a smaller wire diameter is preferred, but there is a trade-off relationship to flatness, total thickness variation (TTV) and warp. Both low material loss and good flatness were achieved for 6-inch wafers by controlling the wire tension, wire speed and slurry supply with conditions similar to 3-inch production. Productivity was optimized by slicing a complete boule at one time, even for a very long boule. This helps to keep wafer properties uniform.(orientation, thickness, warp, etc.)

Figures 6 and 7 show the surface orientation and thickness capability of 3-inch and 6-inch GaAs substrates. 6-inch wafer properties are the same as the properties of 3-inch wafers due to the careful management of slicing facilities, precision of the slicing equipment and slicing conditions.

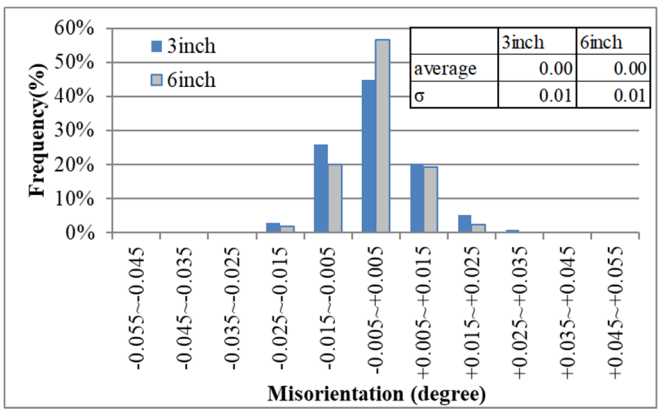

Figure 6. Surface orientation capability for GaAs substrates

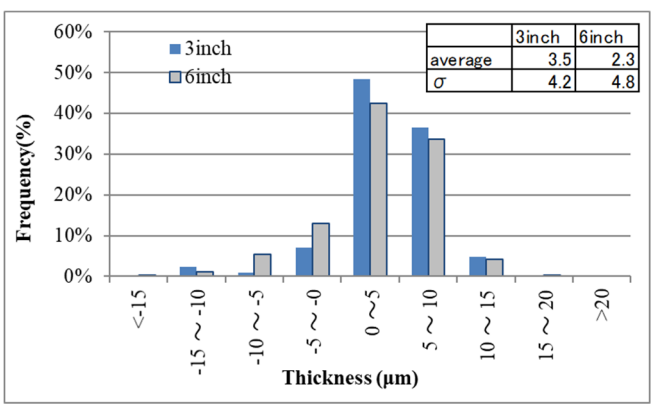

Figure 7. Wafer thickness capability for GaAs substrates (Thickness variation from the design thickness)

Figure 8 shows the flatness capability for 3-inch and 6-inch GaAs substrates. Our standard process for 3-inch is single side polishing (SSP). To maintain the same process capability for flatness in 6-inch, our standard process is double side polishing (DSP). The flatness capability of 6-inch substrate is slightly better than that of 3-inch even though the diameter is larger.

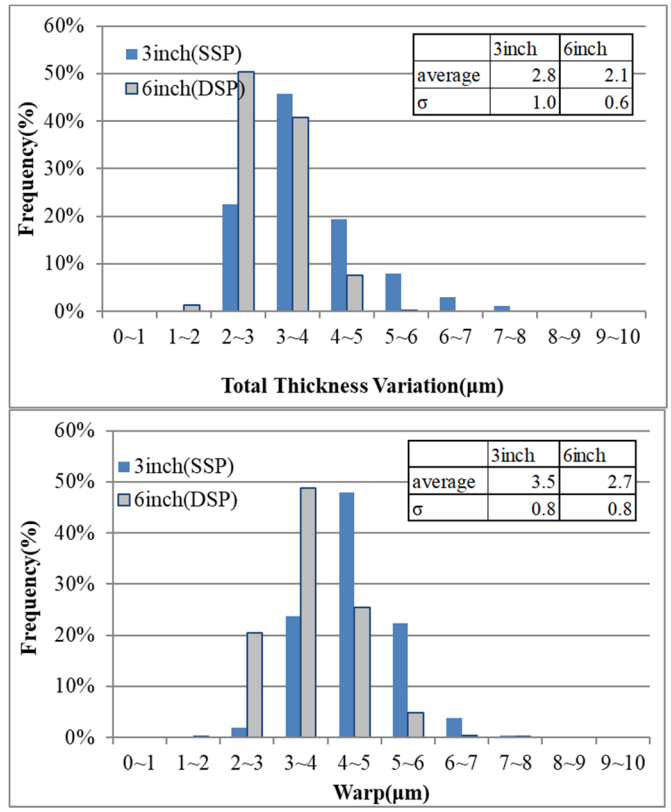

Figure 8. Flatness capability for GaAs substrates

Figure 9 shows the light point defect (LPD) capability for 3-inch and 6-inch GaAs substrates, as measured by a Surfscan tool. Our latest 6-inch's surface process control was applied, and some conditions were optimized for the semi-conducting wafer. Our LPD capability on 6-inch wafers is the same or superior to that of 3-inch wafers on a count per unit area basis.

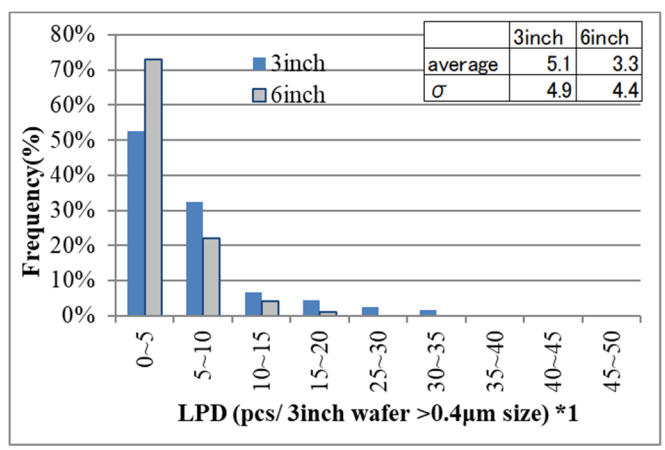

Figure 9. LPD capability for GaAs substrates

(*1) Relative number from 3 inch

The characteristics and productivity of 3-inch and 6-inch GaAs substrates for laser diodes are shown in Table 2.

TABLE 2. CHARACTERISTICS OF GaAs SUBSTRATES

Wafer size	3” for LDs	6” for LDs
Etch pit density(/cm2)	≦500	≦500
Surface Orientation variation(degree)	0.01	0.01
TTV (um)	≦7 (SSP)	≦5 (DSP)
Number of wafers per boule	1	1.2(*2)

(*2) Relative number from 3 inch

CONCLUSIONS

Sumitomo Electric has developed Si-doped 6-inch GaAs substrates for laser diodes, which have crystal and wafer properties similar to our 3-inch substrates. We have also developed efficient production technology. The market requires large volume production of 6-inch GaAs substrates for laser diodes with high quality and reasonable prices. To respond to this market requirement, we have focused on the cost-effective manufacturing by reducing both direct production cost and indirect investment cost. The optimization of both crystal growth and wafering process will make it possible to respond to this market requirement effectively.

REFERENCES

[1] Y.Hagi, et.al., GaAs MANTECH, 2001
Manufacturing 6" GaAs substrates by the VB method
[2] T.Kawase, et.al., GaAs MANTECH, 1999
Properties of 6 inch Semi-insulating GaAs Substrates Manufactured by Vertical Boat Method

ACRONYMS

LD: LASER DIODE
VCSEL; VERTICAL CAVITY SURFACE EMITTING LASER
S.C.: SEMI-CONDUCTING
S.I.: SEMI-INSULATING
HB: HORIZONTAL BOAT
LEC: LIQUID ENCAPSULATED CZOCHRALSKI
VB: VERTICAL BOAT
EPD: ETCH PIT DENSITY
MWS: MULTI WIRE SAW SLICING
DSP: DOUBLE SIDE POLISHING
SSP: SINGLE SIDE POLISHING
TTV: TOTAL THICKNESS VARIATION
LPD: LIGHT POINT DEFECT