Misinterpretation of Drain Transient Spectroscopy in GaN HEMTs: Explanation using a floating buffer model

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Abstract

Drain Transient Spectroscopy is a commonly used technique to characterize trapping in reliability studies in semiconductor devices, and it has been used extensively for GaN HEMTs. Here we show that the standard DLTS interpretation can suggest the presence of both electron and hole traps. However, we demonstrate that the trap attribution can be incorrect, and the hole trap is in fact an artefact. These results show that great care is required in the interpretation of drain current transients in GaN HEMTs, and that trapping cannot always be usefully defined in terms of trap densities and capture cross-sections without reference to carrier transport mechanisms associated with these traps.

INTRODUCTION

GaN HEMTs with high mobility now have a long history, with advancements in device design and processing making them a front runner in both RF and power switching applications[1-3]. Recently a GaN based experimental X-band transmitter was sent into space and is working seamlessly today after two years in orbit, showing no drift in performance[4]. These advancements have been possible due to extensive research which has taken place in the last few years to improve the device performance. Surface issues have been resolved with better passivation techniques and improvement in gate designs have been explored to enhance the performance. Different doping schemes such as Iron (Fe) and Carbon (C) have been used in order to make the buffer more insulating and avoid problems such as punch through in short channel[5]. Fe as dopant is widely used for RF devices, whereas carbon is used for power switching due to its ability to deliver higher breakdown voltage. Currently buffer optimisation has been the focus of research for GaN devices[1].

In this work we evaluate two nominally identical Fe doped GaN-on-SiC wafers with the only difference being the background carbon doping. Wafer A has higher background carbon density than wafer B but in both cases the carbon density is far lower than the bulk Fe doping. Wafer A showed a strong kink effect, whereas wafer B had minimal kink. Drain current transient spectroscopy showed an "electron-trap" response at ~0.59eV in both wafers corresponding presumably to the Fe traps. However, wafer A also showed an "electron" and a "hole" response at ~0.9eV with similar apparent capture cross-section of 4.6×10^{-16} and 1.7×10^{-16}cm^2. Simulation of the transient measurement using the Fe and C densities measured by SIMS can fully reproduce these 3 traps in wafer A, however, the simulation has been done using only two active electron trap levels. Hence it appears that DLTS analysis has inferred the presence of a fictitious hole trap state. We show that acceptor traps located on the drain side of the gate behave like "electron traps" whereas those on the source side behave like "hole traps". This arises due to the necessity to take into account the full transport path to the traps and the existence of more than one active depletion region in the device. We demonstrate that changes in source resistance (Rs) and drain resistance (Rd) are consistent with this interpretation. This work demonstrates that simple DLTS analysis should not be used without taking into account the semi-insulating nature of the buffer. A detailed study explaining kink using a floating buffer model and a linked RF study has been reported in [6, 7]. Here we provide additional details of the trapping dynamics.

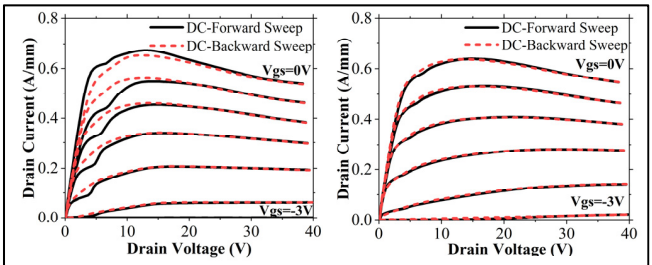

Figure 1. (a) DC output characteristics of wafer A with Vgs varying from -3V to 0V with steps of 0.5V in both forward sweep (0V to 40 V) and backward sweep direction (40V to 0V). Kink can be observed around 3-5V. (b) shows DC output characteristics of wafer B with Vgs varying from −3V to 0V with steps of 0.5V in both forward sweep (0V to 40 V) and backward sweep direction (40V to 0V). No kink is observed in this case.

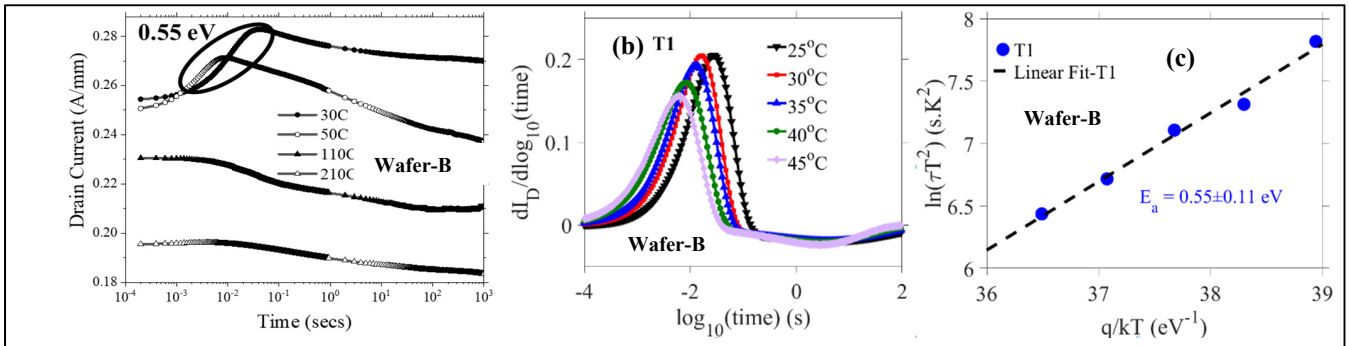

Figure 2. Wafer B: (a) Measured drain current transients following a step from V_{ds}=20V to 4V showing 1 distinct trap superimposed on slow drifts while (b) shows differentials extracted from measured transients at low temperature range 25 to 50°C (c) Arrhenius plots showing extracted activation energy.

SAMPLE AND MEASUREMENTS

Two identical GaN-on-SiC wafers were processed with identical layer structure incorporating nominally identical Fe doping to suppress punch-through, but with different growth conditions. SIMS measurement showed a typical exponential drop in Fe concentration from a bulk density of $3x10^{18}cm^{-3}$ to a density of ~$10^{16}cm^{-3}$ at the surface. There was a 0.2µm thick channel region with ~$5x10^{16}cm^{-3}$ carbon and a bulk GaN region with carbon levels of $3x10^{17}$ (wafer A) and $2x10^{16}cm^{-3}$ (wafer B). The two epitaxies were then fabricated using the BeMiTec process at the FBH in Berlin. Devices used in this study had a width of 2x125 µm, the source-drain spacing of 4µm, a T-gate with foot length of 0.25µm, and a source-gate spacing of 1µm. Ti/Al/Ni/Au and Ni/Au metal were used for Ohmic and Schottky contact respectively and with identical silicon nitride passivation.

Wafer-A like many GaN-on-SiC RF devices showed a significant kink effect which meant that it had a hysteresis at low applied V_{DS} during the DC measurements while Wafer B has much smaller kink as shown in Fig.1. The kink has been seen around ~3–5 V above the knee in all cases and was found to increase in magnitude with increasing the maximum drain bias. Above the kink, all signs of hysteresis are suppressed. The behaviour of kink had similar traits as observed before, such as drain bias dependence and absence during reverse drain sweep[8, 9]. Surprisingly this variation of kink has almost no impact on large signal RF performance measured at 1GHz and both wafers delivered 4W/mm output power at V_{DS}=28V[6, 7].

Drain current transient spectroscopy (DCT) has been performed corresponding to the situation under which kink occurs, stepping V_{DS} from 20V (a bias much higher than onset of kink) to 4V (bias below the onset of kink). Recovery transients were then monitored for 1000 seconds to gain insight into the de-trapping process. Wafer B showed a response at ~10ms (T1) with an activation energy of 0.55eV similar to that frequently observed for Fe doped devices as shown in Fig.2 (a)(b)(c)[10, 11]. For Wafer-A multiple different processes were observed as shown in Fig. 3 (a).

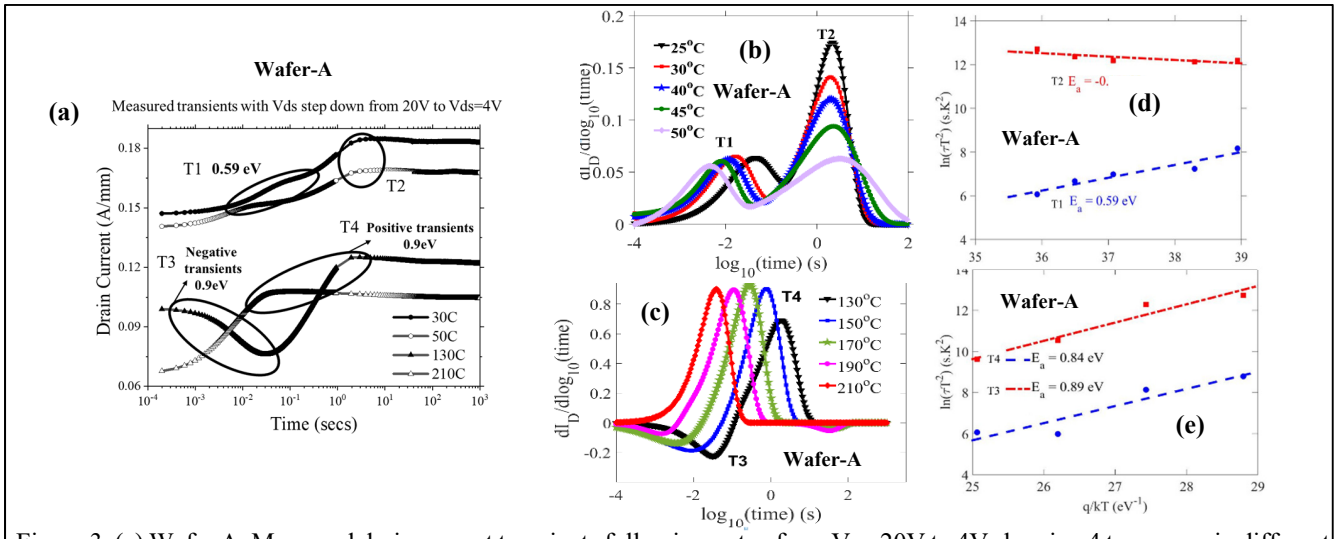

Figure 3. (a) Wafer A: Measured drain current transients following a step from V_{ds}=20V to 4V showing 4 traps seen in different temperature ranges. Differentials extracted from measured transients in the temperature range (b) 25 to 50°C, (c) 130 to 210°C. Arrhenius plots for low (d) and high (e) temperature ranges for all the traps observed in wafer A.

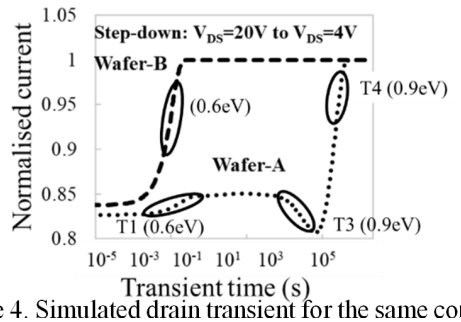

Figure 4. Simulated drain transient for the same conditions as Fig 2a for both wafers. Wafer A showing response from Fe (T1), the apparent 0.9eV hole (T3) and electron (T4) traps while wafer B shows only Fe trap.

Conventional DLTS interpretations showed an "electron-trap-like" response at 0.59eV (T1) corresponding to the Fe traps together with a longer time constant process which was fairly temperature independent (T2)[12]. However, at elevated temperature (beyond 100°C) the wafer shows, a negative (T3) and a positive (T4) response both with activation energy around 0.9eV, which would normally be interpreted as being an active electron and hole trap as shown in Fig.3 (c). Conventional DLTS interpretations would suggest presence of electron trap with positive going response with activation energy of E_A=0.89eV, σ_n=4.6x10^{-16}cm^2 (T4), and a negative-going response generated by a hole trap with E_A=0.84eV, σ_n= 1.7x10^{-16}cm^2 (T3) as shown in Fig.3 (d)(e).

Silvaco Atlas simulations have been performed to understand the origin of these transient responses[6]. Fig. 4, shows that simulation of the transient measurement using the Fe and C densities measured by SIMS can fully reproduce 3 traps out of four observed traps. However, the simulation has been done using only two active acceptor trap levels. Hence it appears that DLTS analysis has inferred the presence of a fictitious hole trap state. T2 has no strong T dependence and is not reproduced in the simulation. It is most likely associated with band-to-band trap-assisted tunnelling through the channel region below the 2DEG, which was not included in the simulation.

Discussion

These results can be explained using the leaky dielectric model for transport in the buffer originally established for GaN power devices[6, 13]. In wafer A, SIMS measurements have shown that in addition to the Fe there is a moderate but quite typical density of carbon of 3x10^{17}cm^{-3}, and this has the effect of neutralizing the Fe acceptors and pinning the Fermi level ~0.9eV above the valence band. So, the GaN bulk is converted to P-type resulting in a floating highly-resistive buffer which is now a semi-insulating region separated from the 2DEG by a P-N junction.

Under drain bias, impact ionization or leakage paths between the drain and the GaN buffer allow a small hole current to flow into the buffer eventually terminating at the source, forward biasing the source, and reverse biasing the drain 2DEG to p-type buffer diode. Hence the buffer can be represented as back to back diodes.

Fig. 5 (a) shows the net ionized charge distribution in the unbiased state and during Vds=20V for wafer A. Under no stress, there is a uniform depletion region of constant width which extends from source to drain. When biased, the holes flow through the semi-insulating buffer producing a resistive potential divider between drain and source. This back biases the 2DEG between drain and gate and produces a negatively charged depletion region of ionized carbon acceptors. The same current forward biases the 2DEG to buffer between gate and source reducing the depletion charge. Based on this the transient recovery can be explained, the two related components arise from: the ~0.9eV "electron trap", T4, resulting from the relaxation of the drain P-N junction, whereas the fictitious 0.9eV "hole trap", T3, is the result of the same acceptors but associated with the re-forming of the source depletion region. This produces the negative and positive components observed in the transients.

For Wafer B case the GaN bulk will be n-type due to the carbon density being less than the bulk background donor density allowing the Fermi level to be pinned to the Fe trap level 0.5-0.7eV below the conduction band. This means

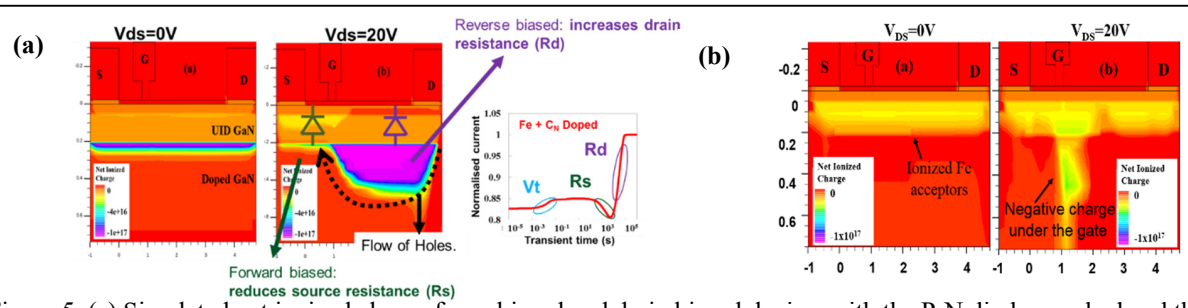

Figure 5. (a) Simulated net ionized charge for unbiased and drain biased device, with the P-N diodes marked and the indicated hole flow in the P-type buffer, along with corresponding transients for wafer-A.(b) Simulated net ionized charge for unbiased and drain biased device for wafer-B showing a relatively small geometrically defined negatively charged region of ionized Fe acceptors located under the gate edge.

TABLE I: IMPACT OF CHANGE IN R_S AND R_D FOR BOTH WAFERS UPON VDS STRESS OF 4V AND 20V ARE SHOWN HERE.

Measured by applying V_{DS}=4V or 20V, then step to 0V and measure R_S, R_D

		Rs (Ω.mm)	Rd (Ω.mm)
Wafer-B	No stress	0.33	2.0
	4V stress	0.33	2.3
	20V stress	0.34	3.4
Wafer-A	No Stress	0.40	2.5
	4V stress	0.36	2.7
	20V stress	0.28	3.2

there is no P-N diode and so the charge cannot accumulate to the same degree. As seen in simulated net ionized charge density under bias there is no significant voltage drop between the 2DEG and the buffer in the gate-drain gap and only a relatively small geometrically defined negatively charged region of ionized Fe acceptors located under the gate edge Fig. 5 (b), leading to a small V_T shift[14].

To confirm this interpretation, the changes in charge state of the P-N junctions under the source and drain access regions have been directly measured using a pulsed measurement of R_S and R_D following drain bias stress as seen in Table I for both wafers. Wafer-A showed a reduction in R_S and an increase in R_D upon stress while wafer- B only showed an increase in R_D and no change in R_S. These measurements give further evidence that the modelling correctly captures the dynamics.

CONCLUSIONS

This work demonstrates that simple DLTS analysis should not be used without considering the semi-insulating nature of the buffer. There is a huge density of traps in GaN HEMTs almost all of which are neutral or inactive. Transport to and from those traps through the resulting semi-insulating buffer should be included in any complete analysis of the device reliability. We note that transport dominated dynamics have also been seen in heavily carbon doped GaN[15].

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