Electrical and Thermal Characterisation of β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs

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Abstract

We report for the first time on the electron trapping and thermal properties of modulation-doped β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs. Capacitance-voltage and current transient measurements are used to characterise traps, while Raman nano-thermography is used to extract a thermal resistance of the devices. The fabrication of β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs offers a promising route to overcoming Gallium Oxide's low bulk electron mobility and via reduced carrier scattering in the conduction channel. In this work, we observe a large threshold voltage (V_{th}) shift during forward-bias capacitance-voltage measurements indicating significant negative charge trapping under the gate. Transient drain-stress measurements have been performed to identify the location of traps which are found to be in the gate and gate-drain access regions. Raman nano-thermography yields a channel R_{th} of 66±2°Cmm/W for a modulation-doped TLM structure. Identifying and reducing the effect of electron trapping in such devices, alongside effective thermal management is essential for reliable device operation and commercialisation.

INTRODUCTION

With a bandgap of 4.9eV, a Baliga's figure of merit (BFOM) more than three times that of GaN and a predicted breakdown field of 9MV/cm, β-Ga_2O_3 is a promising material for use in power electronics [1, 2]. A Johnson's figure of merit comparable to that of GaN also makes β-Ga_2O_3 a candidate for low-frequency, high power RF amplifiers [3]. The possibility of growing β-Ga_2O_3 using established melt methods provides a significant cost advantage over other wide bandgap semiconductors, such as GaN and SiC [4]. However, two major obstacles stand in the way of realising commercial devices. The most significant of these two problems is the anisotropic low thermal conductivity of Gallium Oxide, 27W/mK in the [010] direction [5]. This is ~10% of GaN and has the potential to radically reduce the lifetime of power and RF devices via catastrophic self-heating[6]. RF operation is further constrained by a low theoretical maximum bulk electron mobility of 200cm^2/Vs, [7]. The development of β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs offers a potential way to circumvent these problems in β-Ga_2O_3 devices[8].

In this work, we characterise both the electrical and thermal properties of β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs. We begin by investigating the role of trapping in the HEMTs. Shifts in the threshold voltage, V_{th}, during capacitance-voltage measurements indicate significant charge trapping. The position of these traps is studied using transient-stress measurements. We then use nanoparticle Raman thermography to directly measure the buffer temperature of a TLM structure channel and extract the thermal resistance (R_{th}) of the devices.

DEVICES UNDER TEST

The modulation-doped constricted-gate HEMTs used in this study were fabricated by Zhang et. al. [8]. Modulation doping is necessary as β-$(Al_xGa_{(1-x)})_2O_3$ and β-Ga_2O_3 lack the spontaneous polarisation, and the resulting interface charge, possessed by GaN. A positive space-charge region, resulting from the ionization of donor dopants in the modulation doped layer, ensures the confinement of the 2DEG in β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs.

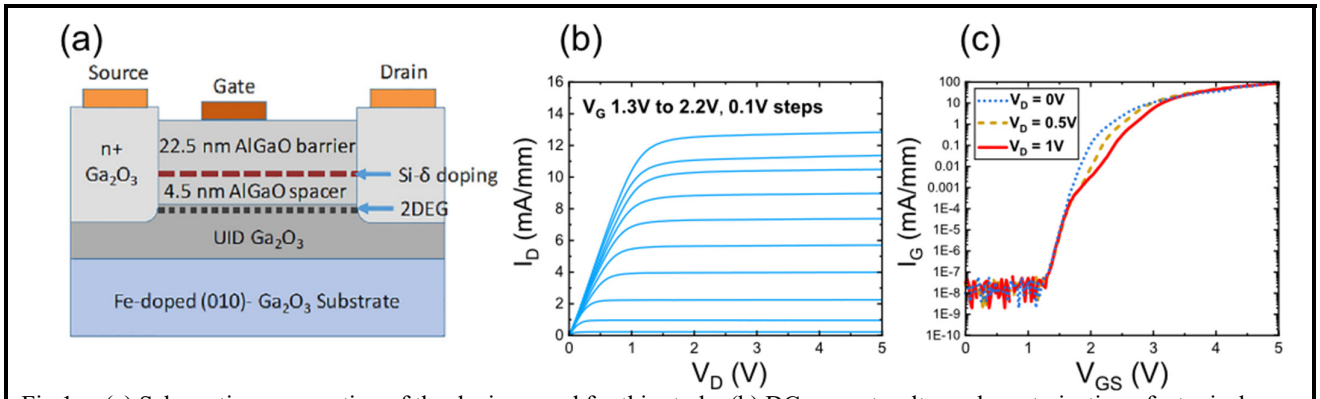

Fig.1. – (a) Schematic cross-section of the devices used for this study. (b) DC current-voltage characterization of a typical β-$(Al_{(1-x)}Ga_x)_2O_3$/ Ga_2O_3 HEMT device. (c) Gate leakage measured for three source-drain biases.

A schematic of the device cross section is shown in Fig. 1(a). It consists of a Fe-doped β-Ga_2O_3 insulating substrate, an unintentionally doped (UID) β-Ga_2O_3 layer, a β-$(Al_xGa_{(1-x)})_2O_3$ spacer, a Si-δ doped layer and a β-$(Al_xGa_{(1-x)})_2O_3$ barrier. Ohmic contacts are formed using a Ti/Au (30/130nm) metal stack, and the Schottky gate with a Pt/Au=30/120nm stack. The devices are single fingered, with dimensions W=5µm, L_G=3µm and L_{SG}=L_{GD}=2µm. The Hall mobility measured on this sample is 153cm^2/Vs along with charge density of 2.14x10^{12}cm^{-2}. The confinement of dopant electrons to the 2DEG has been confirmed by comparison of carrier densities extracted from temperature-dependent Hall measurements and Shubnikov-de Hass oscillations [8].

ELECTRICAL CHARACTERISATION

Fig.1(b) shows the resulting DC output characteristics with a maximum I_D of 0.6mA/mm at V_{GS} of 2.2V; the threshold voltage, Vth, was determined to be +1.3V. Low off-state gate leakage was observed, as shown in Fig.1(c) An I_D-V_G sweep taken for V_D=0.5V yielded a sub-threshold swing of 72.2 mV/decade (not shown); placing an upper limit on interface trap density of 0.95x10^{10} cm^{-2}eV^{-1}.

Forward bias capacitance-voltage measurements were used as a preliminary investigation into trapping in these devices. Fig.2(a) shows the resulting capacitance-voltage curves at room temperature. There is a large positive V_{th} shift between the first forward and reverse sweeps. Subsequent sweeps show a small hysteresis but retain the V_{th} offset. The V_{th} shift of the 1st sweep corresponds to a fixed trapped electron charge under the gate of 5.1x10^{11} cm^{-2} with a reversible electron trapping component of 7.2x10^{10}cm^{-2} seen in subsequent successive sweeps (red lines). Less than 50% of the trapped electrons could be detrapped with extended waiting time (the recovery saturating after about 20mins) when unbiased. Fig. 2(b) shows the result of attempting to detrap the electrons by exposing the device to a 300nm sub-bandgap UV source. Only about 50% of the electrons could be detrapped; longer exposure times made no further difference. This suggests that there are two distinct trapping sites under the gate with a comparable density. of 2.3x10^{11}cm^{-2}, but only one of which can be detrapped. The inability to recover the full capacitance-voltage hysteresis in devices has also been observed by Wong *et al.* in β-Ga_2O_3 MOSFETs and was attributed to a high density of electron traps in the Al_2O_3 dielectric and or at the Al_2O_3/Ga_2O_3 interface [9]. This cannot be the case here since there is no gate dielectric. We note that all the capacitance-voltage sweeps show a small increase in capacitance around V_{GS}= 2V; This is consistent with the real-space transfer of charge from the 2DEG into the β-$(Al_xGa_{(1-x)})_2O_3$/Ga_2O_3 spacer layer.

Drain transient-stress measurements were taken to investigate the time dependence of trapping during reverse gate and drain bias stress as shown in Fig. 3(a). Each stress condition was applied for 10 seconds and then the recovery was monitored for 100 seconds. A strong bias dependent fall in current was observed which recovered after about a minute. The location of the responsible trapping was determined by on-the-fly I_D-V_{GS} measurements allowing extraction of V_{th} and g_m. The impact of -3V gate stress on V_{th} is shown in Fig. 3(b). The observed transient negative shift can be explained in terms of trapping directly under the gate region, with negative gate stress depopulating traps under the gate. The repopulation of these traps in a time less than a second after stress leads to the subsequent positive shift in V_{th}. After 20s there is an increase in transconductance but no further change in V_{th}.

Furthermore, comparing V_{GS}= 0V, V_D= 0V condition with V_{GS}= -3V, V_{DS}= 20V (drain lag), from Fig.3(a), shows large drop indicating trapping in the gate-drain access region or gate region. This can also be observed with varying drain bias stress from 0 to 20V in 5V steps. Any change in the access region will impact measured transconductance g_m. Fig. 3(c) shows the measurements of transconductance following 20V drain stress, with an ON-state measurement condition of V_{GS} = 1.5V and V_D = 1V. There is no impact on the Vth, but a strong drop in transconductance which recovers in about 2 minutes, demonstrating that the primary location for these traps is in the drain access region.

The V_{th} shift and drop in transconductance confirms that traps are not only located under the gate but also in the gate-drain access region, most likely on the surface.

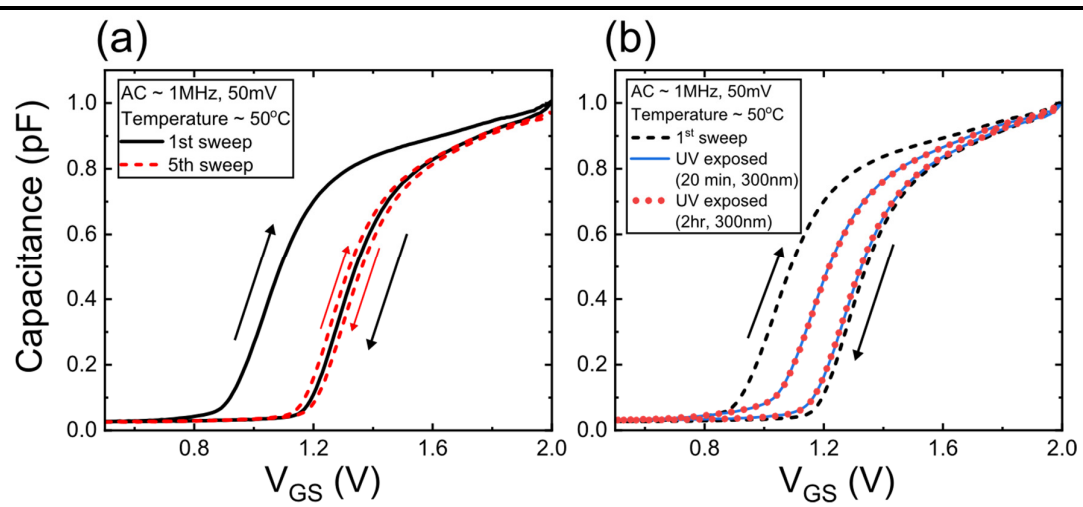

Fig.2. – (a) Room temperature capacitance-voltage measurements at f=1MHz and V_{AC}= 50mV. (b) Hysteresis recovered after exposing the device to 300nm UV source for 20 minutes and 1 hour.

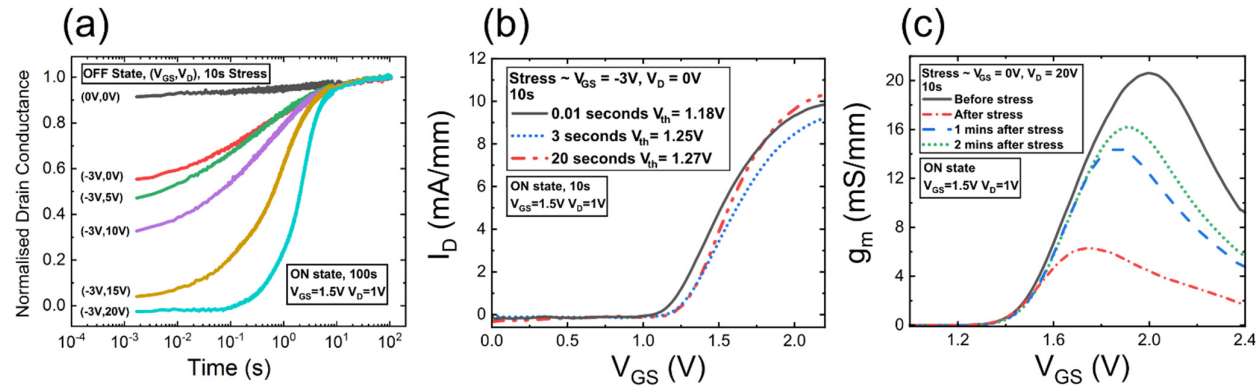

Fig.3. – (a) Stress-transient measurements taken for several (V_{GS}, V_D) stress conditions and normalized to static V_{GS}= 0V and V_D= 0V. t_{OFF}=10s and t_{ON}=100s.
(b) I_D-V_{GS} sweeps measured after 10-second gate stress of V_{GS}= -3V. The shift in threshold voltage was observed for 20 seconds in the ON-state.
(c) Transconductance measurements were taken after drain voltage stress of V_D = 20V.

THERMAL CHARACTERISATION

Device temperature assessment is critical considering the low thermal conductivity of the β-Ga_2O_3. Raman nanoparticle thermography provides an indirect, but accurate, technique for the extraction of channel temperature [10]. This involves the deposition of TiO_2 nanoparticles onto the device channel. During device operation, these particles will quickly reach thermal equilibrium with the channel and the shift in their Raman peak can be used to extract channel temperature. The low density and small size of the TiO_2 particles minimise their effect on channel temperature. A suspension of 99.98% purity 30 nm diameter TiO_2 particles was added to methanol. Sonication of ensured a uniform density of particles throughout the ethanol. The particle-ethanol suspension was drop cast onto the channel of a TLM structure with a 10µm source to drain spacing, as shown in Fig.4(a). A TLM structure was used as higher powers could be reached using an ungated channel. This is because the current through the HEMTs was limited by the enhancement mode properties of the gate region.

Fig. 4(b) shows the variation in channel temperature extracted from the TiO_2 nanoparticle Raman line-shift, with device power. The line-shift with temperature was evaluated by an unbiased calibration measurement at 25°C. A value of R_{th} = 66±2°Cmm/W was determined for the TLM; for a gated device this value would be higher due to the localization of heating at the drain-side of the gate consistent with the 25% higher reported thermal resistance reported by *Pomeroy et. al.* for β-Ga_2O_3 MOSFETs, measured using the same technique [11]. While R_{th} is lower compared to previously reported values it still suggests that device self-heating will be significant in later generations of Gallium Oxide HEMTs.

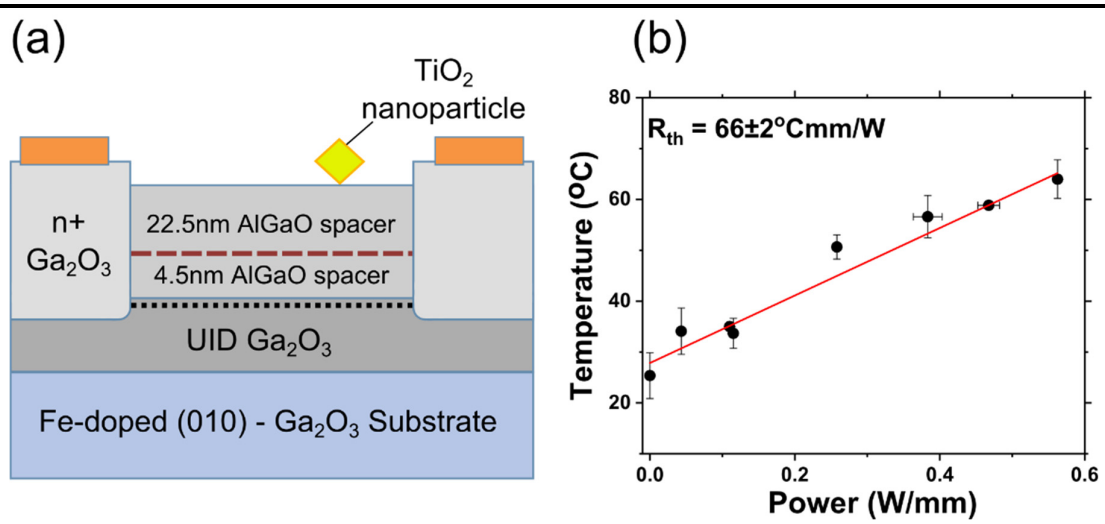

Fig.4. – (a) Schematic of the TLM structure used for Raman nano-thermography with the approximate position of the TiO_2 particle labelled. (b) Temperature extracted from TiO_2 Raman peak shift vs power.

CONCLUSIONS

Significant gate and drain charge trapping are observed in modulation-doped β-$(Al_xGa_{(1-x)})_2O_3/Ga_2O_3$ HEMTs. The location of these charge traps is determined to be both under the gate, and especially in the gate-drain access regions of the device, suggesting that surface passivation will be required. A thermal resistance of 66±2ºCmm/W is reported for a modulation doped TLM structure. Suppression of both electron trap states and device self-heating will be necessary for higher mobility, reliable Gallium Oxide devices.

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