Gross Die Per Wafer and Yield Optimization for GaAs ICs with Sub-Micron Features

Robbie Best and Shiban Tiku

Skyworks Solutions
Newbury Park, CA 91320
Contact: Robbie.Best@skyworksinc.com

Keywords: GaAs ICs, BiHEMT, Lithography, Reticle size, Yield

Abstract

In an effort to maximize gross die per wafer (GDPW) while improving yield, various steps were taken to implement changes in the reticle layout and stepper exposure conditions across multiple designs. This allowed us to satisfy high yield goals for the BiHEMT process in a high volume manufacturing environment.

INTRODUCTION

In IC processing that utilizes 5x lithography tools, reticle sizes of 20 to 25 mm are commonly used. A reticle size of 22 mm has been used at Skyworks with Canon FPA-3000 i5+ exposure systems for many GaAs IC technologies that use FETs as well as Bipolar transistors. Past technologies involved minimal wafer topography, and thus focus issues were not prevalent. However, with the introduction of the BiHEMT process, involving the fabrication of both Bipolar and HEMT devices on the same epitaxial substrate, challenges surfaced with regards to focus at various layers. These challenges were due to the fact that sub-micron features need to be printed at both the highest and lowest portions of the BiHEMT topography, which can span a few microns in z-height. Figure 1 shows a schematic of the typical topography involved in the BiHEMT process. Edge-field focus defects were observed, particularly on layers that use sub-micron features patterned at extreme points in the topography. For example, the base contact layer needs to be resolved not only at the top of the base pedestal (at the top of the topography), but also at the lower portion of the topography to form the bottom capacitor plate. On the other hand, the gate layer needs to be resolved only at the lower portion of the topography, but the resolution required is much finer. This paper explores the steps taken in light of these challenges to successfully maximize gross die per wafer while improving the end-to-end yield.

CHALLENGES

The primary challenge in the BiHEMT process involves imaging across multiple focal planes. This is induced by extreme topography in the BiHEMT design (Fig. 1) that utilizes both Bipolar (at the top of the topography) and HEMT devices (at the bottom of the topography) on the same epitaxial substrate.

Additionally, the BiHEMT process takes advantage of nLOF photoresist in order to achieve a retrograde resist sidewall profile by exposing the photoresist purposefully out of focus. Unfortunately, this makes establishing adequate depth of focus across multiple levels of the topography even more difficult. Further, the more out of focus a feature is exposed, the more its final dimensions can vary, thereby demanding tighter overlay control between layers.

Finally, this tolerance is stressed by lens aberrations such as lens curvature, distortion and astigmatism that worsen as the distance from field center to field corner increases.

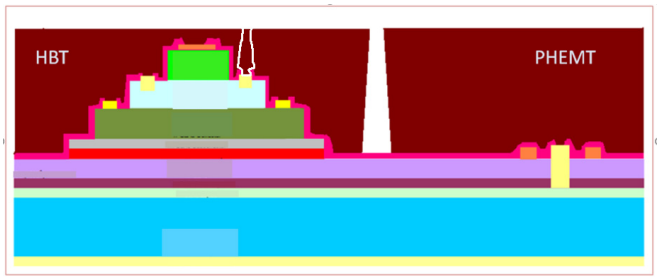

Fig. 1. BIHEMT topography.

APPROACH

In order to safely increase BiHEMT field size from 20 mm x 20 mm in consideration of these process challenges, we developed multiple solutions. To begin with, an in-house algorithm was developed to minimize the number of partial field die based upon photolithography tool capability. In parallel, overlay measurement methodology was developed to ensure appropriate field corner overlay control of critical features as the field size increased. Finally, a “focus invalid area” (FIA) parameter within the exposure recipe was optimized to mitigate risk of marginal focus on remaining partial fields of a wafer exposure sequence. These three solutions were implemented to minimize partial field die, mitigate risk of edge-field focus failures, and improve detection of overlay error.

Minimizing Partial Field Die

As field size changes, the wafer layout changes in terms of the number of rows and columns that are exposed. This determines the number of exposed fields along the edge of the wafer. By inputting various X and Y field dimensions and setting a threshold limit for the percentage of partial die allowed (Fig. 2), our wafer exposure algorithm can reduce the number of partial field die exposed (Fig. 3), maximize gross die per wafer, and reduce the number of total exposure fields to improve stepper throughput (Fig. 4). This relationship is exemplified in Figure 5.

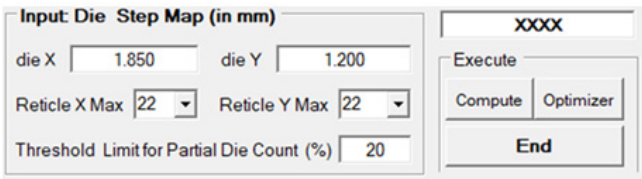

Fig. 2. Screenshot of algorithm input variables.

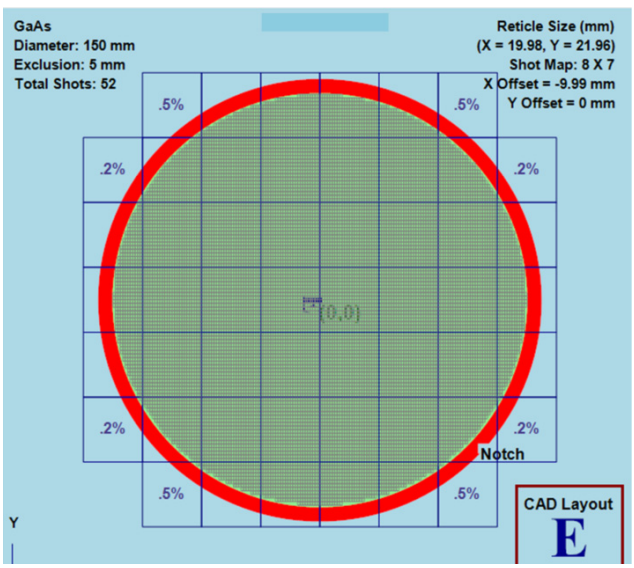

Fig. 3. Example of exposure shot map set to minimize partial field dies.

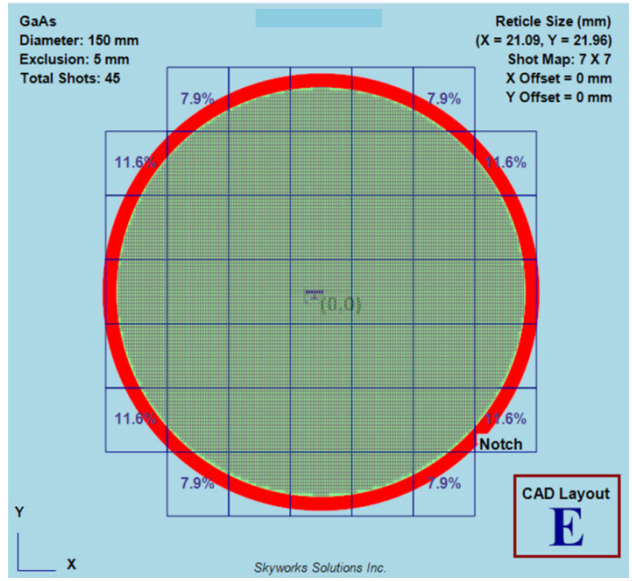

Fig. 4. The above image shows the exposure field layout optimized for stepper throughput. In other words, the total number of exposure fields is minimized.

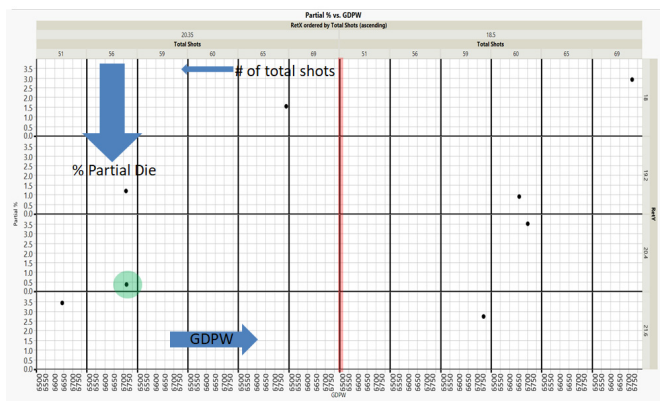

Fig. 5. Relationship between the number of GDPW vs. percentage of partial field die as a function of X/Y reticle field size (secondary X/Y axes) and the number of total exposure shots. The data point highlighted in shaded green shows the optimal condition, where the percentage of partial field die is minimized, GDPW is maximized, and the number of total exposure shots is reduced.

Mitigating Risk of Edge-Field Focus Failures

The greater the number of partial fields, the more likely it becomes that the measured focus and tilt for a partial field exposure is inadequate. The focus invalid area parameter represents the area of the wafer in which the stepper cannot accurately measure focus and tilt. For any given field outside the focus invalid area, five focus detectors are activated, landing on the center and corner of each field to establish the focal plane at which that field is to be exposed (Fig. 6).

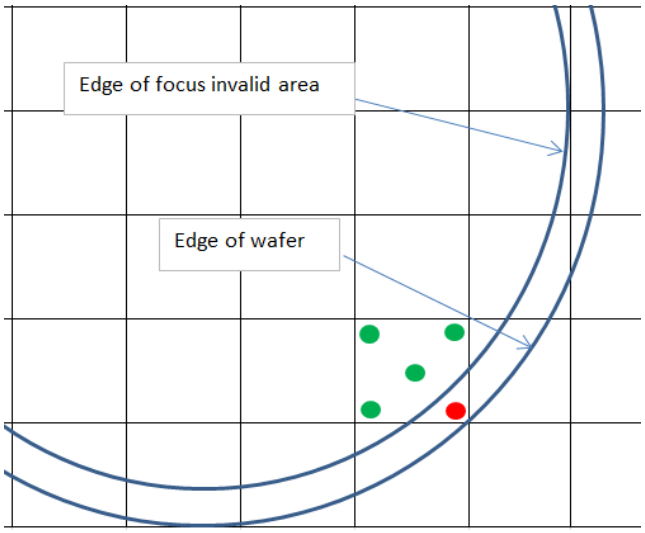

Fig. 6. A partial field with one channel (shown in red) inactive as it is inside the "focus invalid area."

When all channels are active, the focusing system can most accurately and precisely compensate field-by-field for the variability in wafer topography. However, when one or more channels lie on a portion of a field that is outside the focus invalid area, the system relies on the remaining active channels to determine the focal plane of a given field. As a result, both average focus (between the active channels) and die-by-die tilt become less repeatable across the wafer. As the focus invalid area is reduced, more focus channels lie on any wafer edge-fields that are present. After the reticle field size was optimized, the focus invalid area was reduced from 7 mm to 3 mm. This led to the use of as many focus channels as possible. Examples of some of these focus improvements are described below.

In our BiHEMT technology, the base contact (BC) of the transistor is susceptible to focus perturbations on portions of the structure closest to the wafer edge (Fig. 7). Figure 8 shows the improvements in focus as the focus invalid area was reduced.

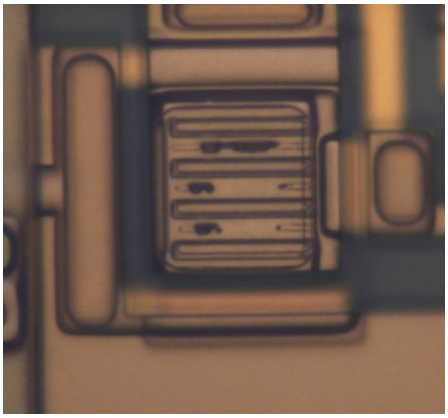

Fig. 7. Missing base contact due to poor focus.

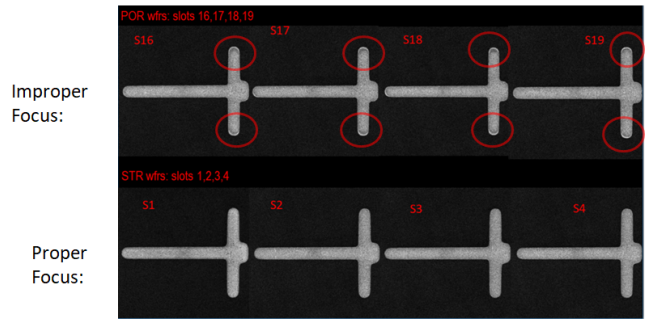

Fig. 8. SEM image showing marginal focus of BC (the top row, slots 16-19 exposed with FIA = 7 mm) compared to optimized Focus (the bottom row, slots 1-4, exposed with FIA = 3 mm).

The Contact Via (CV) layer, drawn to sub-micron geometries, is another feature that is highly sensitive to focus in the BiHEMT technology. The CV layer is patterned to multiple layers, and requires careful depth of focus characterization to ensure the via remains at dimension in the BiHEMT topography. Figure 9 (below) shows the improvement in depth of focus on partial fields as focus invalid area is reduced from 7 mm to 3 mm.

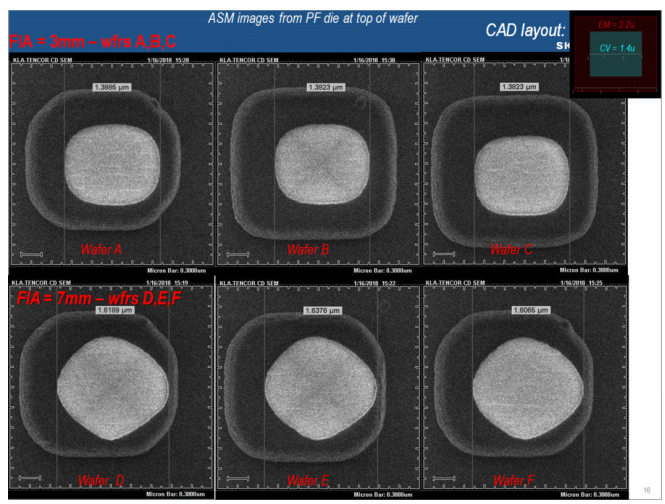

Fig. 9. The above SEM image (after resist strip) shows the same contact via feature on a partial field on six wafers. For the first three wafers (top row), FIA = 3 mm and the feature was exposed at the proper focus condition. For the last three wafers (bottom row), FIA = 7 mm and thus, the feature was exposed at a marginal focus condition.

The Gate Layer (GL) is patterned at the bottom level of the topography at sub-micron geometries, often in long serpentine "finger" patterns that require a carefully controlled retrograde resist profile. Perturbations in focus can easily lead to missing or displaced gate "fingers" as shown in Figure 10. By reducing the focus invalid area, yield loss due to missing GL was minimized.

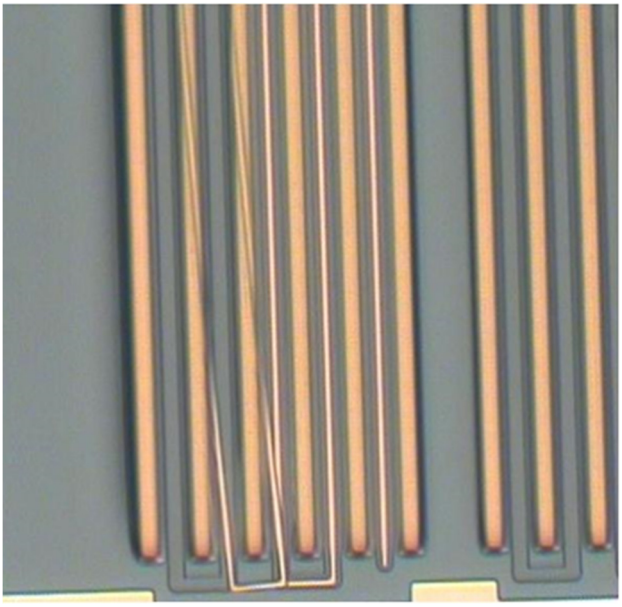

Fig. 10. Missing and displaced gate layer (GL).

Improving Detection of Overlay Error

Variations in CD between two layers can impact the overall overlay budget. Increased CD variation of two stacked layers reduces the overlay budget between them. In the BiHEMT technology, the base pedestal (BP) sits on top of the base contact. Both the base contact (BC) and the BP layer align directly to the emitter contact (EC), making the alignment between BC and BP indirect. To control overlay between BC and BP, an overlay box-in-box structure was created. In this investigation, a measurement routine was created to directly measure overlay between BC and BP as an indicator of overlay capability at larger BiHEMT field sizes. As shown in Figure 11, overlay distribution widens in field corners vs. field center due to stepper lens aberrations. This measurement structure is utilized to ensure that BC does not fall off of BP as field size increases.

CONCLUSIONS

As a result of these efforts, we have developed the tools and infrastructure necessary to confidently optimize GDPW while improving stepper throughput, consistency in device performance and product quality.

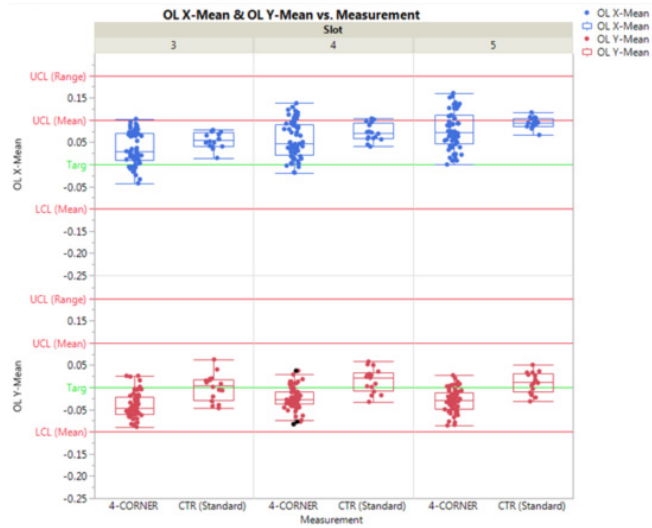

Fig. 11. The above data between wafers three, four and five (secondary x-axis) shows poor X and Y-overlay (primary y-axis) control in four field corners compared to the field center. The reticle field size of 20.520 µm X 20.710 µm was used in this example.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of colleagues in both the Advanced Technology Group and Process Engineering, particularly Ravi Ramanathan, Randy Bryie for his guidance, and Steve Mayer for his insight into Canon stepper theory of operation.

ACRONYMS

GDPW: Gross Die Per Wafer
IC: Integrated Circuit
GaAs: Gallium Arsenide
FIA: Focus Invalid Area
HEMT: High-Electron-Mobility Transistor
BiHEMT: Bipolar High Electron Mobility Transistor
PHEMT: Pseudomorphic-High-Electron-Mobility-Transistor
BC: Base Contact
BP: Base Pedestal
EC: Emitter Contact
CV: Contact Via