Volume Manufacturing of Highly Integrated System-On-Chip (SOC) InP-Based Photonic Integrated Circuits

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Abstract

We demonstrate volume manufacturing of highly integrated system-on-chip (SOC) InP-based photonic integrated circuits (PICs). Essential elements to the successful manufacturing of InP-based PICs are discussed as well as manufacturing capability and reliability of commercial devices which integrate >400 functions onto a single InP-based chip.

INTRODUCTION

Over the past few decades, the exponential demand to increase transmission capacity in optical communication networks has led to breakthrough developments in photonic integration offering an attractive path for scaling bandwidth while simultaneously providing a better cost than comparable discrete components [1]. Since the early 1990's this trend in optical communications has been to deploy networks with increased photonic integration as illustrated in Figure 1. The introduction of the first fully integrated multi-channel optical system-on-chip (SOC) 100Gb/s transmitter and receiver PICs in 2004 [2] helped surpass the bottlenecks observed in the networks at 10Gb/s. Each subsequent generation of commercial SOC InP-based PIC transmitters and receivers has increased both its functionality and density. InP PICs play a key role in telecommunication networks enabling an order of magnitude increase in data capacity per InP-chip every decade. These advances have resulted in significant benefits to the economics, power consumption, density, and reliability of high capacity Dense Wavelength Division Multiplexing DWDM systems.

This paper summarizes key design elements necessary to manufacture and deploy high-yield and reliable SOC based on InP- photonic ICs consistent with the data capacity needs of optical communication networks. We demonstrate yield performance consistent with enabling increased integration.

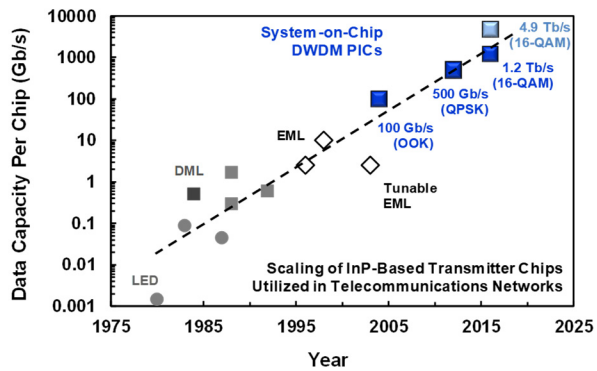

Fig. 1 Illustrates thedata capacity per chip trend in commercial optical networks for InP-based trasmitter chips. The data capacity per chip has doubled in an average of every ~2.2 years (fit to the data) for the last 30+ years enabled by the employement of photonic IC's. Since the introduction of the first fully integrated multi-channel optical system-on-chip (SOC) 100 Gb/s transmitter and receiver PICs in 2004, commercial system-on-chip (SOC) DWDM PICs have been essential to scaling (dark blue). The most reserch result demonstrating a SOC DWDM PIC capable of 4.9 Tb/s capacity is also shown (light blue).

MANUFACTURING OF SYSTEM-ON-CHIP (SOC) PHOTONIC INTEGRATED CIRCUITS

During the mid-2000's, efficient high-capacity coherent optical fiber communication became feasible. To date, several generations of commercial multi-channel SOC InP-based PIC transmitters (Tx) and receivers (Rx) have been developed and deployed based on compact PIC architectures that leverage coherent modulation [3]-[5]. Both 1.2 Tb/s (6 channels x 200 Gb/s per channel) transmitter and receiver PICs with independent widely tunable lasers per channel over the extended C-band were in manufacturing in 2016 [4], [6]. These photonic ICs were the first commercial fully integrated coherent transmitter and receiver PICs with integrated widely

tunable lasers, and the first commercial multi-channel PICs operating at 16 QAM.

A flow diagram showing the primary manufacturing steps to fabricate, test and qualify 1.2 Tb/s commercial PICs is shown in Fig. 2. The complexity of the manufacturing process is reflected in the number of actual operational steps within the Epitaxial, Wafer Fabrication (WFAB), Die Fabrication (DFAB), Assembly, Test steps (functional and DC test), Reliability (burn-in and screening) and full PIC performance test (all channels DC, RF test and link).

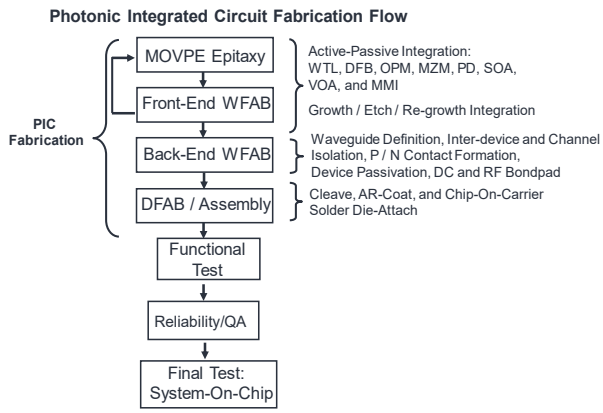

Fig. 2. Schematic flow diagram of the sequence of primary manufacturing steps to fabricate, test and package commercial PICs. WFAB: wafer fabrication; DFAB: die fabrication. Monolithically integrated components: widely tunable laser (WTL), distributed feedback laser (DFB), power monitors (PM), Mach Zehnder modulator (MZM), photodiode (PD), semiconductor optical amplifier (SOA), variable optical attenuators (VOA) and multi-mode interferometer (MMI).

Continuous advances in silicon and III-V semiconductor fabrication technologies have enabled a highly capable fabrication platform for InP-based PIC manufacturing.

Figure 3 compares the line yield (normalized per 10 mask layers) for a Si CMOS fab circa 1990's and multiple generations of transmitter SOC InP-based Photonic ICs. The line yield (LY) is calculated as:

$$LY = \frac{WO}{WO+SC} \quad (1),$$

where WO is the number of wafers completed during the period and SC is the number of wafers scrapped during the same period. To compare disparate fabrication processes, the line yield is normalized to yield per 10 mask levels by the relation:

$$LY_{10} = (\mathrm{LY})^{10/\mathrm{ML}} \quad (2),$$

where LY is the overall line yield, ML is the number of masking layers, and LY_{10} is the calculated line yield per ten layers. To aide a direct comparison note that the line yield excludes the crystal growth steps. Nevertheless, the yields of the PIC crystal growth processes are currently comparable to

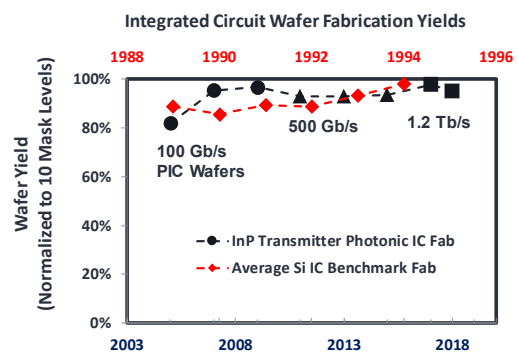

Fig. 3. Wafer fabrication yield (normalized to ten mask levels) for multiple generations of transmitter Photonic IC wafers compared to a benchmark Si CMOS fab (1989–1994).

the cumulative wafer fabrication yields.

Like Si electronic ICs, the data shows that line yields for four consecutive generations of InP-based PIC products are in the high 90% range (normalized to ten mask levels). In spite of important differences between InP PIC manufacturing and the Si IC industry (wafer size, multiple materials and epitaxial growth and regrowth steps, industry maturity), the wafer fabrication yields that can be achieved in a state-of-the-art InP PIC fab (e.g. Infinera Corporation) are now equivalent to that of Si CMOS circa mid 1990's [7][8] in large part due to adopting a methodology similar to electronic ICs, where designers are given a fixed (albeit limited) tool set to design within, resulting in a cost-effective manufacturing process.

At Infinera Corporation, multiple generations of PICs with different integration platforms are fabricated on the same fabrication line. To ensure performance and quality is achieved across all product lines, with high-yields, it was important to incorporate a continuous learning process and rigorous manufacturing control/methodologies, including gauge repeatability and reproducibility (R&R) studies. This has led to systemic improvements of the fabrication capability over multiple years. As of exit 2018, at least 90% of the in-line specifications for the 1.2 Tb/s product line have Cpk values > 1.33 (data not shown) [9].

Another essential enabling element to realize high-yield fully integrated system-on-chip photonic ICs is the reduction of "killer defects" incidents [10]. Yield calculations were performed on DC test data for four generations of SOC DWDM transmitter PICs fabricated at Infinera Corporation. Fits to the Murphy model [11][12][13] result in the killer random defect densities shown in Fig. 5. The defect density numbers for mature InP-based PICs, compare well with those in the Si industry circa early 1990's, and have a rate of

decrease (defect reduction learning) similar to what the Si industry achieved in 1975–1995 [14]. It is noted that the 1.2 Tb/s transmitter PICs has an improved yield compared to previous generation 500 Gb/s PICs, exemplifying defect reduction learnings as the 1.2 Tb/s PIC is largely an extension of the 500 Gb/s platform and hence, leverage the same volume learning curve [1].

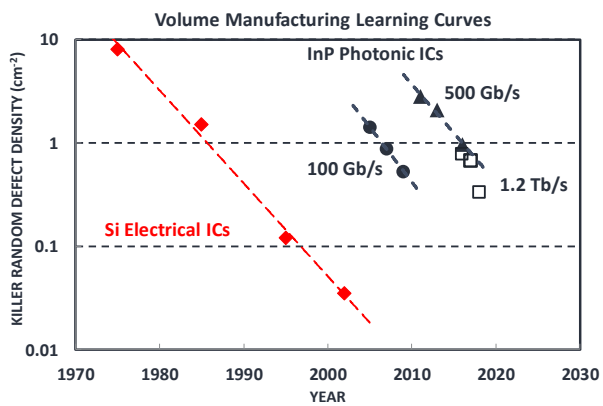

Fig. 5. Wafer fabrication yield (normalized to ten mask levels) for multiple generations of transmitter Photonic IC wafers compared to a benchmark Si CMOS fab (1989–1994).

Wafer-level testing of each die enables the identification of Known Good Die (KGD) to characterize and isolate the performance of optical functions and sub-elements within a PIC and help ensure quality control and product compliance. Furthermore, the fabrication of 1.2 Tb/s PICs integrates control and monitor signal elements to support the optimized performance of a multititle of optical functions.

The manufacturing capability of InP-based PICs developed at Infinera Inc has enabled economically viable SOC with integration levels > 400 functions [1],[15]. As of 2014 InP-based PICs with over 1700 monolithically integrated optical functions were demonstrated in a research lab, underscoring the scalability of the integration platform and fabrication processes [16]. To scale, SOCS will utilize a combination of higher order modulation formats, higher baud-rate, and increased channel counts. Already the next generation Tx PIC platform is 1 Tb/s per wave capable operating at 100 GBd × 32QAM and supports modulation formats with variable spectral efficiency [8][17][18].

Reliability of System-on-chip (SOC) Photonic Integrated Circuits

Each generations of commercial SOC DWDM PICs and modules have undergone extensive reliability testing and are qualified to Telcordia GR-468 standards [19]. An important value of SOC DWDM PICs is the elimination of optical couplings from a DWDM optical system, resulting in a substantial cost savings and reliability improvement (as the opto-mechanical fiber coupling joint is typically one of the least reliable elements of a photonic component). Infinera's fourth (1.2 Tb/s) generation coherent transmitter and receiver PICs enable >100x reduction in fiber couplings. Thus, the reliability of systems employing these SOC modules is greatly improved by virtue of the elimination of a substantial number of fiber couplings in the system. Fig. 6 shows the long-term operating stability for one of Infinera's earliest field deployed 10-channel, 100-Gb/s [1],[20].

The transmitter module has operated for over 100k field hours (equivalent to >11 years). The change in optical output power from each channel is calculated relative to the initial power from data recorded at deployment and shown overlaid in the plot (green). All 10 channels exhibit stable performance that is within +/-0.05dB. Similar data from the integrated sense elements for the applied per-channel VOA attenuation (data not shown) and DFB power change (green) are within this variation. Thus, the resulting output power stability results from the stability of each element within the PIC. The frequency stability (prior to correction from controls) from the same PIC shown in Fig 6 is within a 5 GHz range and is <10% of the range which can be compensated by the tunable DFB and corresponding control circuits. The data presented herein help establish that like electrical ICs, reliability of the photonic IC is far superior to that that of the equivalent implementation using discrete components [1],[20].

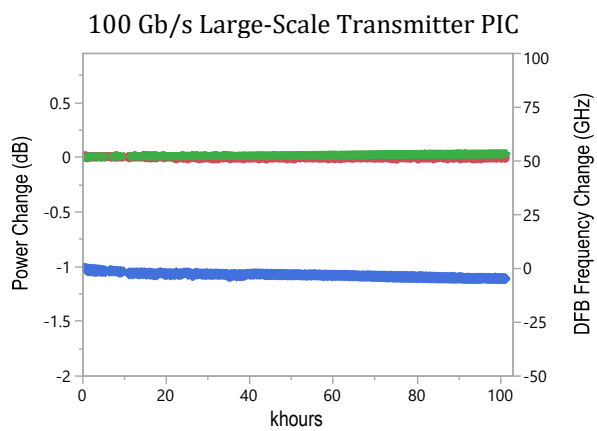

Fig. 6. Plots of reliability data from 100,000 hours (>11 years) for a field deployed 10-channel 100 Gb/s first generation PIC transmitter module. The PIC power change is <0.05dB; the uncorrected frequency change is < 5GHz which is less than 10% of the range that can be compensated by the tunable DFB and corresponding control circuits.

Conclusions

The successful demonstration of reliable and manufacturable high-channel count InP-DWDM PICs with a

path to 1 Tb/ per wave demonstrates a technology capability that can simultaneously achieve both optimal performance and high-yield. This is achieved by systematically reducing the killer defects with each SOC generation combined with the implementation of rigorous process control and manufacturing methodologies similar to those used in Si IC fabrication. The yields achieved point to an ability to continue to scale the bandwidth of PICs through integration of a high number of diverse optical functions per channel.

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