Yield Improvements in a High-Mix Fabrication Environment

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Abstract

Yield improvement, both line yield and on wafer DC electrical test yield, is a critical activity occurring in every semiconductor fabrication facility. While the overall goal is consistent - 100% yield - differing environments (i.e. lower mix higher volume or higher mix lower volume) require different approaches in order to maximize the effectiveness of the work to get to that goal. This paper discusses two pieces of work related to improving yield in a higher mix environment. The first part discusses the impact of flat-finders on InP wafers (wafer handling impacting line yield) and the second part discusses using the correlation between on-wafer DC testing and PCM testing to drive down cycle time for process improvements (impacting electrical test yield).

INTRODUCTION

MACOM Technology Solutions' Central Fabrication Facility in Lowell, MA has a very wide range of technology platforms supporting a hugely diverse product portfolio. These technology platforms include Si-bipolar transistors and diodes, GaAs PIN diodes, Schottky diodes, varactors, GaAs pHEMT, AlGaAs PIN switches and InP lasers. Running all of these technologies in one fabrication facility requires careful material management. Coupled with that is the need to tailor the monitoring of product performance across a large number of technology platforms running simultaneously. We previously reported on adapting our process control methodology to account for such a diverse manufacturing environment [1]. In this paper we report on the work being done to improve line yield on the InP products, as well as the approach taken to improve cycle time for evaluating process improvements our GaAs IC product line to improve electrical test yields.

WAFER HANDLING

MACOM fabricates lasers for GPON and Data Centre Applications using InP substrates. Prior to 2015, MACOM was not producing InP substrates in volume production. Table I compares the material properties of InP, GaAs and Si [2]. Comparing the microhardness and the fracture surface energy of InP to Si, the material properties of InP point to a more 'fragile' material, with more careful handling required. Indeed, there are numerous publications reporting on efforts to minimize GaAs wafer breakage [3-5], which, from the material properties shown in Table 1, is more robust from a handling perspective than InP.

The problem statement in this instance therefore is that InP wafers were breaking at a higher rate than the starting substrates for the other technology platforms. Starting considerations included individual pieces of processing equipment and/or specific wafer processing steps in making the lasers. No clear tool/process commonality was initially apparent. Of course, the drive to find root cause of broken wafers is complicated by the fact that wafers can be damaged at one stage of the process, but not actually break until further on in the process. It was observed that a significant portion of the broken wafers had edge chips around the flat of the wafer, from which the break line propagated as shown in Figure 1. Such chips can be caused by a number of different events. Collisions of the wafers within cassettes or impact when loading into processing tools are just some examples. Indeed, in the first instance of this investigation, some tool loading discrepancies were identified and corrected. However, they were clearly not the sole cause of the wafer chips being observed. Flat-finders were also highlighted early on in the investigation as a potential root cause for micro dents in the wafers. They are used multiple times in the process to orient the flat of the wafers for some tools, to find wafer IDs and for any edge inspections. There are many models throughout the fabrication facility – all manual.

TABLE I
MECHANICAL PROPERTIES OF THE SUBSTRATE MATERIALS [2]

Parameter	InP (100)	GaAs (100)	Si (100)
Microhardness (GPa)	4.3±0.2	6.9±0.3	11.2±1.0
Fracture Surface Energy (J/m^2)	0.63	0.78	2.55

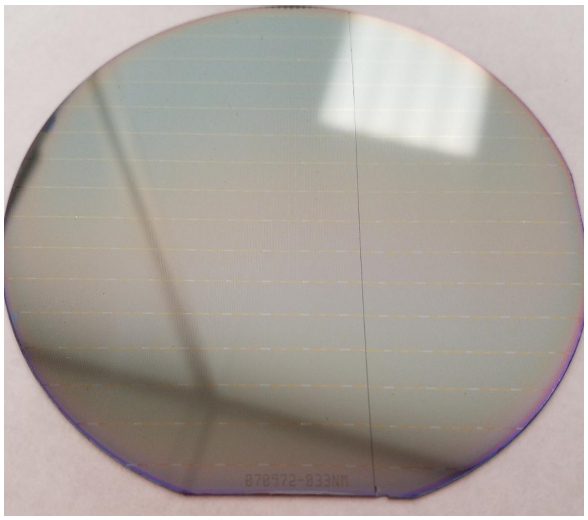


Fig. 1: Example of broken InP wafer with chip at the flat of the wafer

Experiment I was designed to validate the hypothesis that flat-finders could lead to increased InP wafer breakage by inducing chipping on the edge of the wafers. Using an InP mechanical wafer, and focusing on the flat of the wafer, images were taken at 20X, prior to any flat finding as shown in Figure 2(a). The wafer then went through one revolution of one of the suspected flat-finders and the images were retaken and stitched together - Figure 2(b). Dents were clearly visible on the flat of the wafer following the flat finding operation. At this point the relevant flat-finders in the fabrication facility were taken apart, fully inspected, cleaned and scheduled for upgrade where required.

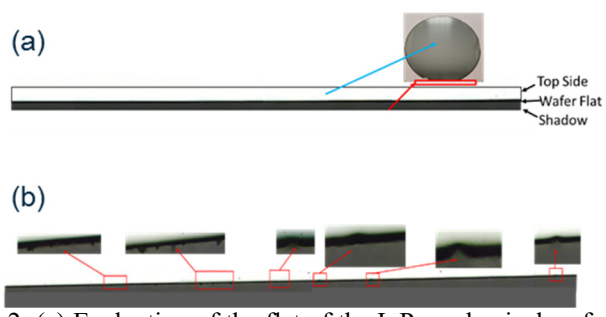


Fig. 2: (a) Evaluation of the flat of the InP mechanical wafer prior to any flat finding. (b) Identifying dents/chips found at the flat of the wafer following one rotation on the manual flat-finders. This was a flat-finder with a Delrin roller and no steps (Type B).

Experiment II investigated the impact of differing types of flat-finders using the same methodology. All of the flat-finders were cleaned using the protocols developed as a result of Experiment I. Three types of flat-finders were evaluated. Type A was an automatic flat-finder demo which was used for evaluation and comparison. Type B had Delrin rollers with no steps (used on the wafer presented in Figure 2 – but now through the full cleaning procedure). Type C flat-finders had polyurethane rollers with step build up.

The results articulating the impact of 150 rotations on a wafer for each of the three different types of flat-finders are summarized in Table II. Figures 3 and 4 show the accompanying pictures for Type C (with steps) and Type A (automatic flat-finder) respectively. Varying types of damage were observed. The dents were small deformations that occurred in the wafers, small chips began to formulate at times, and some pre-existing dents became bigger. The dents do eventually become chips, which cause the wafers to be at a higher risk for breakage. 150 was the number of revolutions chosen as a real representation of how many rotations the wafer would see in any given process.

TABLE II

IMPACT OF DIFFERENT FLAT-FINDER TYPES INVESTIGATED IN THIS WORK ON THE INP WAFERS FOLLOWING 150 REVOLUTIONS

Category	Type A	Type B	Type C
New Dents	0	3	0
New Small Chips	1	~2	~8
Bigger Dents	0	1	0

Type C flat finder (with the steps) had the most negative impact on the wafers. In discussions with the vendor, this was not surprising as the steps increase the level of impact of the wafers with the flat-finder, and for the more fragile InP wafers this results in increased chipping. Type B does impact the wafer to a much lesser level, as it does not have the steps. The wafers still do come into contact with the supporting rails that are a part of the build of the flat-finder. However, using an automatic flat-finder results in the least amount of impact to the wafer as the areas in which the wafers came into contact with the flat finder also are minimized. In addition, it allows wafers to be aligned using a steady and adjustable rate of rotations, as well as eliminating any contribution of human variation. In all cases, the wafers do come into contact with the wafer carrier in the flat-finding events, regardless of the type of flat-finder. As a result of this work, stepped flat-finders are no longer used on the InP product line.

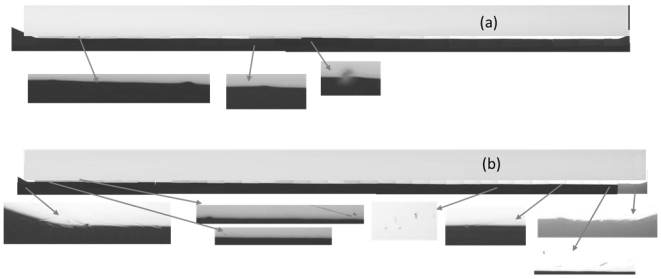


Fig. 3: Evaluation of the InP mechanical wafer (a) prior to and (b) following 150 revolutions on flat-finder Type C. Chips are formed as a result of the flat-finding.

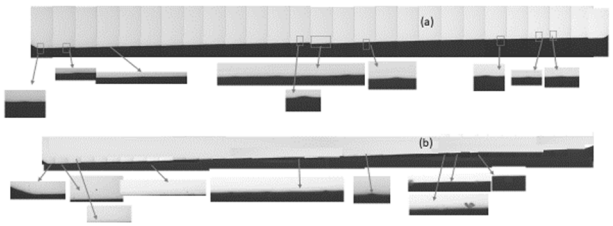


Fig. 4: (a) InP mechanical wafer prior to the automatic flat-finder, and (b) following 150 flat finds using automatic flat-finder (Type A). It is notable that most of the new occurrences on the wafer were debris, and minimal damage.

ON WAFER TESTING

In many production environments, on-wafer DC testing is seen as a capacity constraining, cost increasing exercise with little return on investment. This is arguably the case in a lower mix higher volume fabrication facility where the input variables are being kept constant and electrical testing of the final packaged parts is in place to catch any excursions that may occur (not caught by other process controls). However, in a fabrication facility with a higher mix of products, it cannot be assumed that there will be a steady stream of any one type of product for continuous process performance readout. Implementing on-wafer DC test therefore allows a faster, clean readout of the performance of the fabrication facility, across all of the varying products and technologies. From a timing perspective there is no delay in waiting for the packaged product test (which can be up to 6 weeks in some cases). From an engineering perspective the potential assembly impacts do not have to be decoupled. A second big advantage of using on wafer DC test is to evaluate process improvements on the product performance. Even this, however, can take longer than desired with complex devices requiring many process steps before reaching end of frontside processing for device testing and characterization.

There is one approach that can be useful in order to reduce the time to getting the first device performance evaluations of process improvements. By investigating the relationship between the in-line process control monitor (PCM) data and the on-wafer DC electrical test data, we have provided our integration and process engineers with in-line readout points to do targeted process development in short loop mode.

Figure 5 demonstrates the relationship found between the PCM leakage parameter SD_IL and the product parameter Ilk1_8 (device leakage parameter) for one of our GaAs IC products. It is clear that the PCM leakage parameter correlates to the product leakage parameter. Also, it is clear that the leakage parameter itself is correlating to the subsequent overall DC yield of the wafer: decreased SD_IL PCM leakage predicts decreased leakage levels in the product die, resulting in higher DC yield of the wafer.

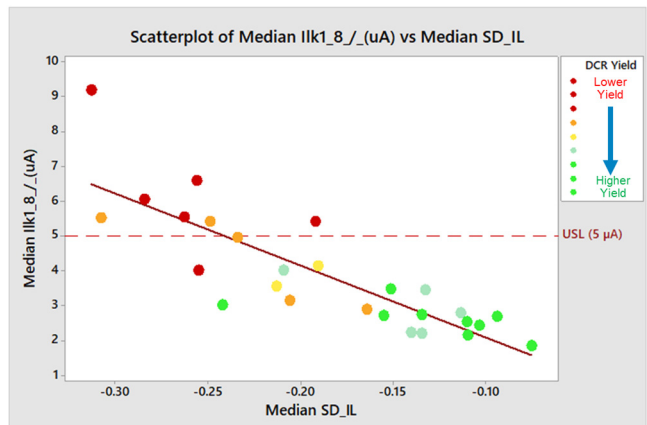
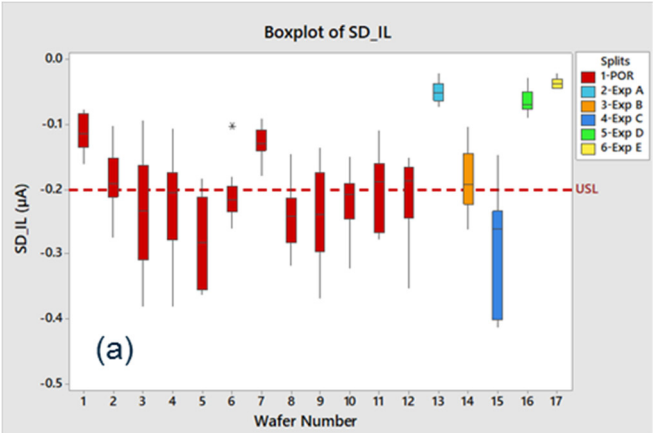


Fig. 5: Correlation of the Final product leakage parameter Ilk1_8 measured at DC test versus the corresponding PCM leakage parameter SD_IL, and their relationship with on wafer DC test yield. For reduced leakage at both PCM and on wafer test, on wafer DC test yield is increased.

These correlations are extremely powerful. There is now a readout point in-line in the fab (PCM), which will directly impact the on-wafer DC test yield. Any process changes in the fabrication facility to improve the leakage can be verified using the PCM structure without having to wait for a long period of time. With the knowledge of the correlations shown, the likelihood of the process changes giving the desired result at electrical test, although not a certainty, is more likely. Figure 6 demonstrates the approach being implemented in our fabrication facility using the correlations shown in Figure 5. Figure 6(a) demonstrates the PCM parameter performance for lots fabricated with the process of record (POR), and those with alternate processing at a particular step. Experiments A, D and E clearly lead to reduced SD_IL PCM leakage. As predicted by the correlations shown in Figure 5, the wafers with the reduced PCM leakage subsequently demonstrate improved on wafer DC- test yield, shown in Figure 6(b). This was deduced as a function of short loops around the PCM results with increased confidence that the experimental results would lead towards the end goal of increased DC test yield. It is estimated that

this prediction reduced the process development cycle by 2 weeks.



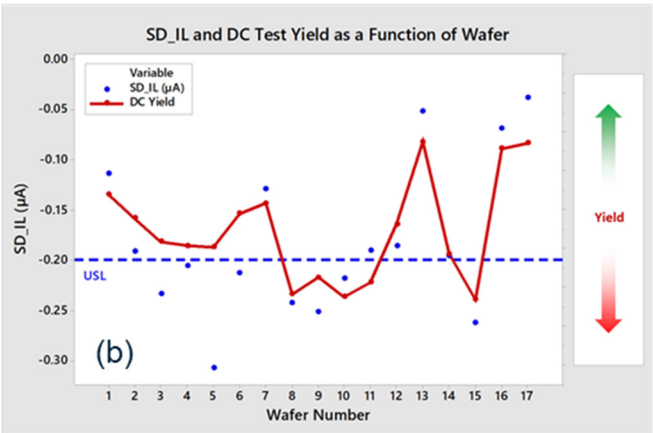


Fig. 6: (a) Boxplot of PCM leakage parameter SD_IL performance for wafers processed with POR and those with experimental splits demonstrating lower leakage levels for the experimental splits. (b) Mapping of the results in (a) to on wafer DC test yield.

This approach does, of course, have its limitations. The correlation between the PCM parameter and the on-wafer DC test parameter must be found in the case of each product. It cannot be assumed. The ability to observe such a correlation can be reduced by the nature of the yield loss mechanism and/or the structural difference between the PCM device and the product device. The approach therefore is not a one approach solution for all. However, as is pertinent to this paper, in the case of a higher mix lower volume fabrication facility, using this methodology where possible is hugely valuable in the time acceleration it brings to process yield improvements.

Conclusions

This paper described two pieces of work with regards to yield improvement in a high product mix fabrication environment. An investigation into the impact of flat-finders on InP substrates demonstrated that they can induce chipping on the edge of the InP wafers, resulting in wafer breakage. We also demonstrated the ability to use PCM performance to predict on-wafer DC test yield allowing the PCM data to be used as a readout of the ability of process improvements to increase product yield. This is especially pertinent in the high mix manufacturing environment where a continuous stream of product through the line cannot be assumed.

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Acronyms

GPON: Gigabit Passive Optical Network
DC: Direct Current
PCM: Process Control Monitor
POR: Process of Record
InP: Indium Phosphide
GaAs: Gallium Arsenide
Si: Silicon