Systematic Data Cleaning Methodology for Datasets by Fading Out Unknown Process Issues

Peter Gretz[1*], Franck Bourgeois[1], and Michael Hosch[1]

[1]United Monolithic Semiconductors GmbH, Wilhelm-Runge-Strasse 11, 89081 Ulm, Germany
[*]e-mail: peter.gretz@ums-ulm.de, phone: +49 (0) 731 505-3176

Keywords: Systematic Analysis, Epitaxial Delta-Doping, GaAs, pHEMT, double recess

Abstract

Process Control Engineers all over the world face the same problem with different interactions in process and epitaxial variances at the same time in production. The possibility to separate the different influences on the electrical MMIC performance requires a deep level understanding of device physics and the process step influences, as well as the physical mechanisms behind and a high epi growth accuracy. This paper will address a method to separate in the data set different production process influences from epitaxial impacts to find a significant and precise correlation between the epitaxial delta-doping level and the transistor drain current level.

INTRODUCTION

The sensitivity of GaAs pHEMT technologies to process influences increases with the complexity of their structure. This can be well observed when looking to the evolution of the GaAs FET technology from a GaAs MESFET via a single recess GaAs pHEMT to a more process and semiconductor surface sensitive double recess GaAs pHEMT technology for high power applications.

The results shown in this paper were summarized on a GaAs double recess technology developed at UMS GmbH with a double-sided Silicon delta-doped channel. The sheet carrier density (Ns) in the channel is measured on single growth runs by the epitaxy supplier with a destructive reverse processing approach on single epitaxial wafers. Thereby, the first two top layers of the epitaxial layer sequence are etched away and afterwards the Ns is measured by hall measurements.

SYSTEMATIC DATASET SELECTION AND PREPARATION

The drain-source current level of a pHEMT (Ids) is defined by the delta-doping level of its epitaxy. But the accuracy of the correlation between the channel sheet carrier density (Ns) and Ids suffers on intermixing of the epitaxial growth and process fluctuations as well as metrology on epitaxy and device level. Fig.1 illustrates huge variations to nearly 20% in Median(Ids+_FET) and Median(Vg100_FET) for various delta-doping levels from Epi batch to Epi batch and growth run to growth run as well as the process fluctuations within a single growth run. Where Median(Ids+_FET) represents the Ids at a Vgs of +0.8V and Median(Vg100_FET) is the pinch off Voltage(Vgs) at Idss/100. See the parameter also graphically presented in Fig.3. The median values are determined from 20 measured PCM's on each wafer. There is no clear correlation of Ids+ and Vg100 with the epitaxial doping levels visible, if all available data in an epitaxy delivery batch is taken into account. The root causes are not restricted to doping adjustments in-between of single growth runs, as can be seen for example in the delivery batch 011-M. There was one growth run of seven epitaxial wafers with higher Ns around |2.25|E12 cm-2 and the next two growth runs of fourteen wafers were grown with the tool settings for a lower Ns of |2.17|E12cm-2. Both epitaxial tool settings show wafers with equally high and low current level plus outlier in both directions on the lower doped growth runs indicating additional powerful influences on the current level of the transistors.

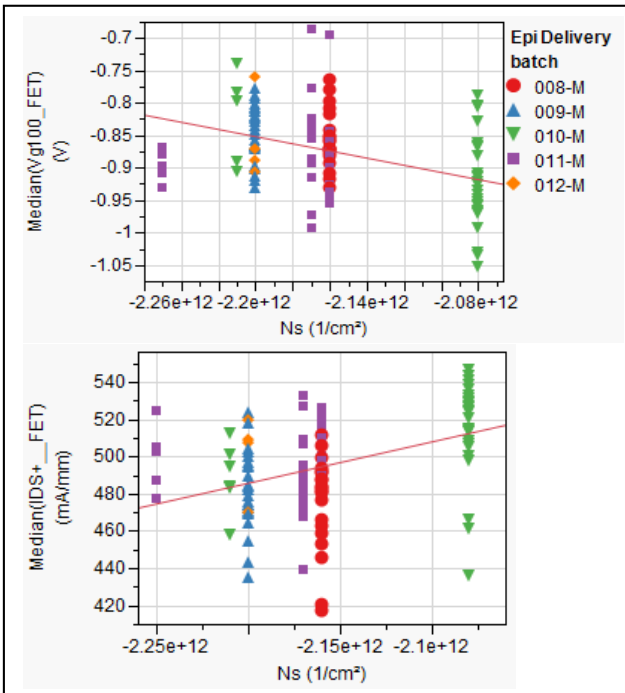

Fig. 1. Vg100 and Ids+ correlated with Ns

The correlation accuracy increases with the following different methods:

1) Increase sampling rate for measurement of Ns
2) Reduction of process fluctuations
3) Pre-selection of the most significant data
4) Selection of electrical parameter with direct link to doping level

1) Increase sampling rate for measurement of Ns

Ns measurements are usually done on an epitaxial wafer by etching back the highly doped cap layer to measure only the channel doping. It is therefore a destructive measurement method, which increases the single wafer price strongly as the metrology efforts and destroyed wafer amount increases.
This method would make sense for a limited period to generate some statistics, if a correlation moves unexpectedly in the wrong direction. Another possibility is to drive stronger doping variations on single growth runs to provoke variations with the high risk to generate expensive unusable material.

2) Reduction of process fluctuations

Process influences on DC parameter are frequently linked to various differing process steps and tools at the same time. Correlations with tools, bad periods and the interaction of two or more tools in-between several processes can be therefore simply ineffective and extremely time consuming. Especially, if different process issues occurs at the same time.

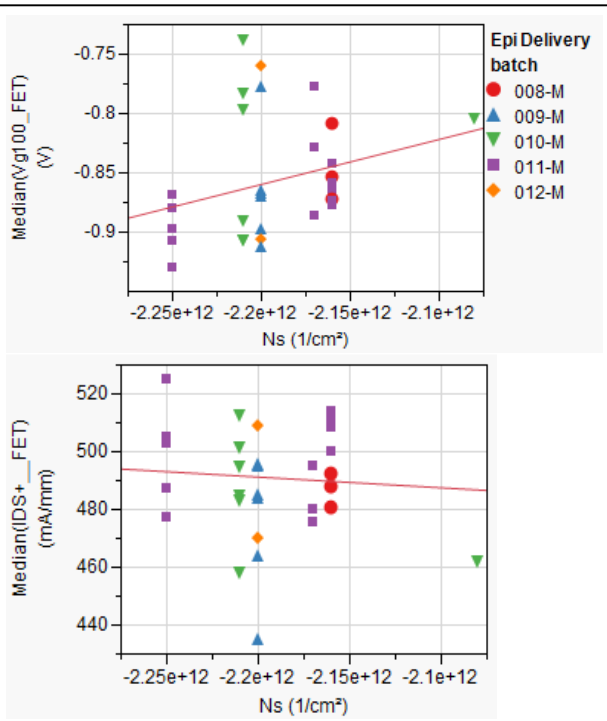

Fig. 2. Ids+ and Vg100 correlated with Ns after pre-selection

3) Pre-selection of the most significant data

Epitaxial growth sisters (abbreviated "EpiSis" in the following) are the single wafers grown in the same epitaxial growth run. Considering only single growth runs, where the Ns is measured on an EpiSis will directly result in an increased correlation accuracy, as can be seen in Fig. 2. The correlation accuracy enhanced, as Ids tend to higher values for higher doping levels, due to an increased number of charge carriers in the channel.

4) Selection of electrical parameter with direct link to doping level

This method starts at the end of the process at the investigation of the PCM parameters itself. Fig. 3 illustrates the transfer characteristics of PCM transistors on three wafers grown in the same epitaxial growth run. The DC characteristics differ for each single EpiSis although the channel doping level is equal.

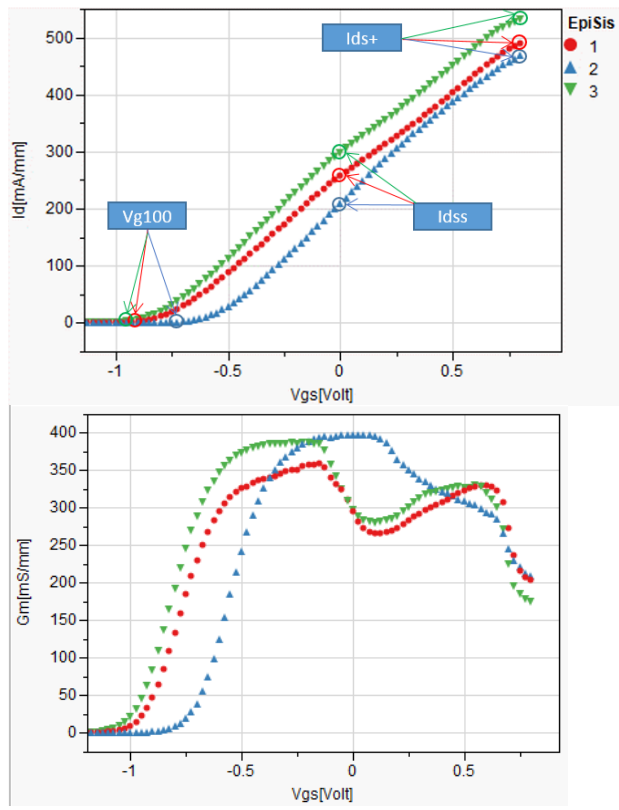

Fig. 3. Differences in DC transfer characteristics of 3 wafers grown in the same epitaxial growth run

Several assumptions can be extracted from Fig. 3.

a) Ids+ and Idss show strong variations for the same epitaxial growth run
b) Physical regularities of the device indicates that curve 2 is negatively affected by an unknown issue, as you have less current for the same doping level.

There is an unwanted mechanism behind, which reduces the sheet carrier density in the channel.

c) Vg100 is almost the same for curve 1 and 3. Curve 1 seems to be negatively influenced by process, due to less current for almost the same pinch off voltage in comparison with curve 3. Vg100 is therefore the most precise parameter for correlations with the epitaxial doping level.

d) EpiSis 3 has the highest current level (Ids) over the whole range of the gate source voltage (Vgs) and represents therefore the best case with the lowest damage related to process issues.

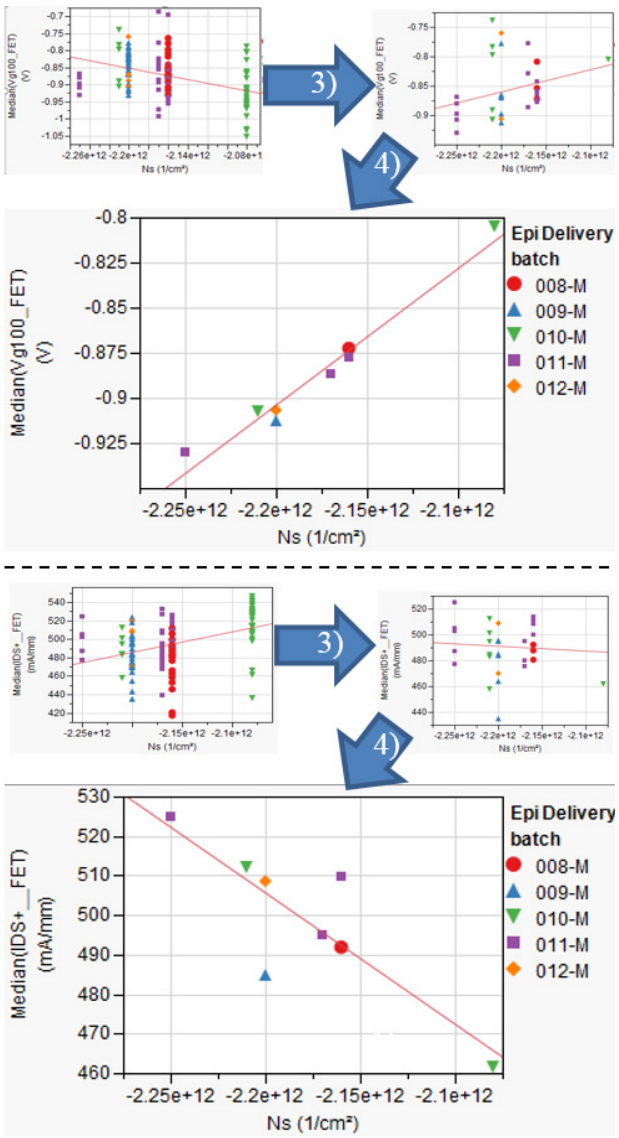

Fig. 4. Ids+ and Vg100 correlated with Ns

It is often useful at the start of a correlation to use only data, where the most direct relations are available. This paper concentrates therefore on the last two methods, as the first two methods are either very cost-intensive or have many unknown variables, which leads to a high time consumption with an unknown outcome.

The combination of the previous restriction of the database (method 3) and the collected information out of the DC curves (method 4) results in a precise correlation between Median(Ids+_FET), Median(Vg100_FET) and the doping level, as can be seen in Fig. 4. The correlation accuracy strongly increases using only PCM data of EpiSis wafers with an available destructive Ns measurement and the selection of the wafer with the most negative Vg100 value, as the identified suspect wafers with curves 1 and 2 in Fig.3 are removed. The well fit of the wafers emerged out of the methodology over various Ns variations inside and in-between of Epi delivery batches delivered in a period of one year validate the functionality of the method described in this paper. Especially, the three wafers of three different epi growth runs with higher Ns variations in the Epi delivery batch 011-M and the two wafers in the Epi delivery batch 10-M underpin the accuracy of the fit.

Furthermore, method 4) outlines with abbreviation considerations from the best transistor performance with the most negative Vg100 for each EpiSis clearly different process issues and additional process deviations. This shows Fig. 5.

$$\%dev(Vg100)=\frac{\text{Median(Vg100) of EpiSis - Median(Vg100) of best EpiSis}}{\text{Median(Vg100) of best EpiSis}}*100$$

$$\%dev(Idss)=\frac{\text{Median(Idss) of EpiSis - Median(Idss)of best EpiSis}}{\text{Median(Idss) of best EpiSis}}*100$$

$$\%dev(Ids+)=\frac{\text{Median(Ids+) of EpiSis - Median(Ids+) of best EpiSis}}{\text{Median(Ids+) of best EpiSis}}*100$$

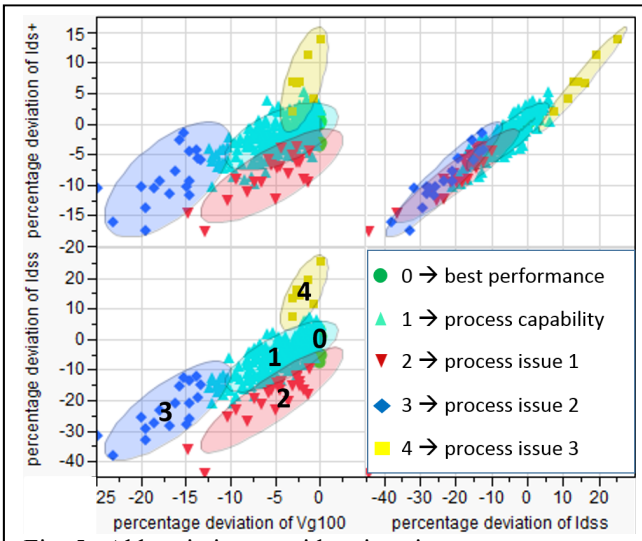

Fig. 5. Abbreviation considerations in percentage deviations of Vg100, Idss and Ids+

Explanations to the single categories of Fig. 5:

- 0 → Best performance:
  - Origin for abbreviation calculations, due to the point mentioned in 4.d). Fits to the picture of EpiSis 3 in Fig. 3
- 1 → Process capability:
  - ~90% of considered Wafer are lying in this area
  - All other areas are atypical and represent different process issues
- 2 → Unknown process issue 1:
  - fits to the picture of EpiSis 1 in Fig. 3
- 3 → Unknown process issue 2:
  - fits to the picture of EpiSis 2 in Fig. 3
- 4 → Unknown process issue 3:
  - new unknown DC characteristic
- Points in between of those areas are probably affected by interaction of several process issues

CONCLUSIONS

This paper illustrates a systematic method to analyze data by excluding process issues in comparison of the transistor DC transfer characteristics and shrinking the dataset in combination with physical knowledge of the device. This enables in first order a better correlation of the epitaxial sheet carrier density in the channel (Ns) with the current (Ids) on transistor level to targeting the right doping level on epitaxial growth side.

In a second order, different process issues can be extracted in a methodological way, which facilitates also the choice of material for investigations of their origin by physical analysis.

ACKNOWLEDGEMENTS

The authors would like to thank the people in production line, who generated the database for these correlations.

REFERENCES

ACRONYMS

Vgs: Bias voltage between Gate and Source contact
Ids: Current level measured between Source and Drain contact
Idss: Ids at Vgs = 0V
Ids+: Ids at Vgs = 0.8V
Vg100: Vgs at Idss/100
Ns: sheet carrier density in the channel
pHEMT: pseudomorphic High Electron Mobility Transistor
PCM: Process Control Module
EpiSis: Wafers grown in the same epitaxial growth run
%dev(Vg100): percentage deviation of Vg100 in-between of the best performance wafer and another wafer of the same epitaxial growth run
%dev(Idss): percentage deviation of Idss in-between of the best performance wafer and another wafer of the same epitaxial growth run
%dev(Ids+): percentage deviation of Ids+ in-between of the best performance wafer and another wafer of the same epitaxial growth run