High-Volume pHEMT Yield Improvement Through Mitigation of Incomplete Removal of InGaP

Robert Waco, Yiping Wang, Chang'e Weng, David Punsalan, Ron Herring

Qorvo, Inc.
2300 NE Brookwood Parkway, Hillsboro, OR. 97124
Robert.Waco@Qorvo.com (503) 615-9439

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Abstract

This paper identifies individual root cause of several fabrication-induced defects under the gate metal of pHEMT products. In each case, InGaP, used as an etch-stop layer when forming the gate, was inadequately removed. Residual InGaP between the gate metal and the channel caused wafer scrap and product die sort yield loss. Scrap events occurred due to numerous out of spec EFET and DFET-related parameters measured on process control monitor (PCM) test structures and at an inline DC test point. Additionally, wafers passing the PCM test criteria, suffered significant yield loss at product die sort testing. Root cause analysis ultimately revealed manufacturing changes or variation, as the source of the InGaP non-removal.

INTRODUCTION

In semiconductor manufacturing, a quick response to a process excursion is essential to contain the problem, find the root cause, and implement a permanent, corrective action. Given a parametric failure on a PCM test structure or product die at die sort, there may be multiple causes to consider. In some situations, failure analysis is needed to get closer to the origin of the failure. In this paper, several case studies, all related to the same interface in a pHEMT gate contact, will be covered. Specifically, all examples are related to an InGaP layer, which did not get properly removed (InGaP non-removal) during the gate processing. Cases which all fail the same electrical parameter were found to have different assignable causes. In some cases, die sort wafer maps shed light on the mechanism, eliminating several other possible models, resulting in a single root cause. This paper shows a process module or single process step can be susceptible to multiple process problems. When a permanent correction action is implemented, the process becomes more robust.

This paper will outline the pursuit to find the origin of a defect, causing product die yield loss and wafer scrap. Through the use of parametric analysis, wafer map review, failure analysis, process flow dissection, and experimentation, the root-cause was discovered leading to a permanent fix eliminating any chance of reoccurrence.

PROCESS BUILD-UP

In the construction of the EFET and DFET gate module, photo lithography defines the gate opening, followed by etch, which lands on an InGaP layer. InGaP is used as an etch-stop to ensure the Schottky layer thickness remains as supplied by the epi vendor, thus providing on-target EFET and DFET pinch-off voltages, VpE and VpD, respectively. The InGaP is wet etched with NH_4OH then HCl and immediately processed through the gate metal deposition to for the transistor gates. It is critical to have a clean interface between the gate metal and the Schottky layer. Thus, removal of all InGaP and short queue time from InGaP etch to gate metal deposition is imperative. Seen below, Figures 1 shows the lithography and etch defined gate opening that stops on InGaP.

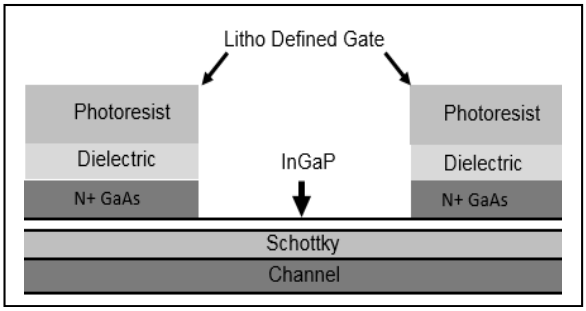

Fig. 1: Lithography and etch defined gate, prior to InGaP etch.

Seen below, Figure 2 shows the InGaP removed from the wet chemistry, the metal gate deposited, and field metal and photoresist removed.

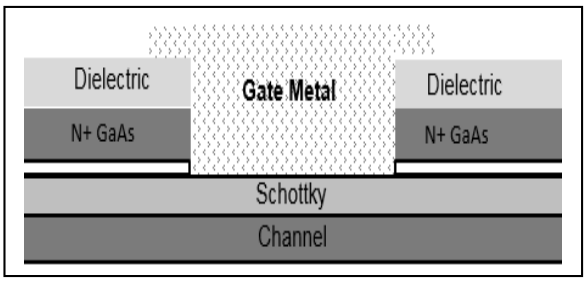

Fig. 2: Post gate metal deposition and photoresist strip / liftoff. InGaP is completely removed from under the gate metal.

PARAMETRIC FAILURES

Depending on the severity of InGaP non-removal and the mechanism that caused InGaP to remain beneath the gate metal, there are several different parametric signatures. If InGaP remains under the EFET gate metal, the first E-Gate Platinum deposition is blocked from diffusing toward the channel. The diffusion is critical to set the transistor's pinch-off. Inadequate diffusion results in reduced VpE, making the EFET more like a DFET. If InGaP remains under the DFET gate metal, the Titanium barrier metal "super-diffuses" towards the channel. This enhanced diffusion results in more positive VpD, making the DFET more like an EFET.

Gross InGaP non-removal that impacts the entire wafer surface, or a large portion of the wafer, can be caught with a process control monitor (PCM) test structures at an inline DC test point. The transistor failures will be related to VpD, VpE, and likely see a degradation in forward voltage (Vf), and ideality (Idlty). If the problem is less severe, such as around the edge of the wafer, it seldom overlaps a PCM test structure. In these cases, the failures will be caught at Die Sort. The failing signature for the DFET transistor is related to low switching current (speed). The failing signature for the EFET transistor is related to low pseudo-VpE measured on a test FET in the circuit.

These correlations were determined from wafer scrap events, die sort yield loss and failure analysis of transistors from wafers with these signatures. These correlations will be discussed more throughout the failure analysis and root cause analysis sections. These will be designated as Case #1, #2, and #3.

Case #1: Full wafer scraps. In the case of PCM failures, several lots were tested at the inline DC test step and showed failures for positive VpD and other lots for more negative VpE. This resulted in full lot scraps at this inline PCM test step. A wafer was sent to failure analysis to help determine the cause.

Case #2: Minimal PCM failures; die sort yield loss around the edge of the wafer. Failure mode is DFET transistor with low switching current.

Case #3: Similar as case #2 in GFA (Gross Failing Area) and failure mode. This was revealed after the corrective action had been put into place to eliminate Case#2.

Die Sort Yield loss pattern in cases #2 and #3 are similar to the GFA seen below in Figure 3.

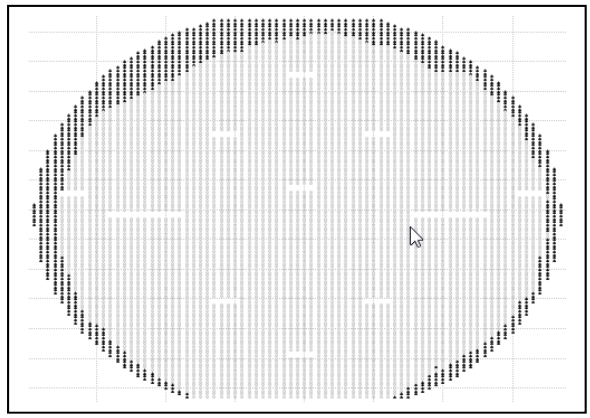

Fig. 3: Wafermap example of a low yielding wafer at product DC sort. The dark regions around the edge of the wafer shows failures due to slow DFET switching speed.

FAILURE ANALYSIS

In Case #1, with gross failures in the PCM, representative wafers were brought to failure analysis, where a focused ion beam (FIB) was used cut through the gate defect and provide an image that would indicate the reason for failure. It should be noted, that Scanning Transmission Electron Microscopy (STEM), and Spectra Analysis worked best for high resolution images and identification of the material (InGaP) under the gate metal. In cases #2 an #3, overlap of the GFA at die sort and the PCM test structures made failure analysis significantly easier than having to analyze the circuit and isolate a defective FET, as the PCM exhibited a similar parametric signature as the failing die in the circuit. Wafers exhibiting the failures in the PCM were brought to failure analysis as part of the yield analysis investigation.

In each of the three cases the FIB/STEM revealed a defect under the gate metal (as seen in Figure 4). The Spectra Analysis of the defect identified the material between the gate metal and the Schottky layer as InGaP (as seen in Figure 5).

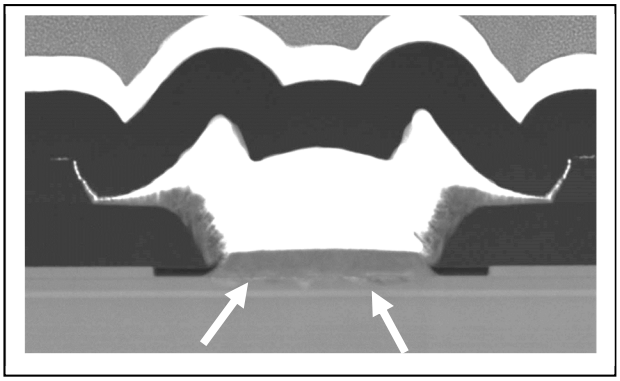

Fig. 4: STEM image of an EFET with residual InGaP (white arrows), blocking the Platinum diffusion to the Schottky layer.

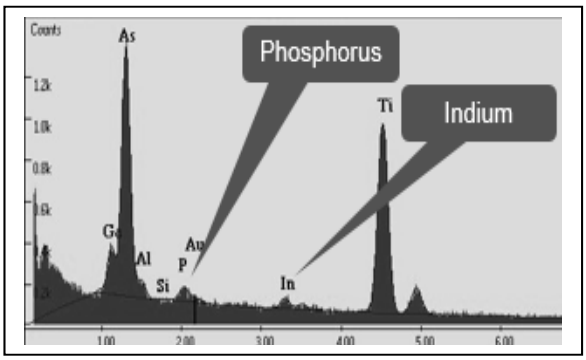

Fig. 5: Spectral Analysis indicated Indium and Phosphorus (InGaP) in the GaAs defect area.

ROOT CAUSE ANALAYSIS

This section details the three different root causes for the three failure modes caused by InGaP non-removal.

Case #1. In this case, gross PCM failures for positive VpD and negative VpE caused wafer scraps on several lots that were tested at the inline DC test step. After the failure analysis indicated the failures were due to InGaP non-removal, the gate lithography, etches, cleans and gate metal deposition were examined.

The failures stopped as the investigation was underway. The commonalty analysis revealed all lots were processed after a preventative maintenance event (PM) on the wet bench (sink) used to etch InGaP. Among many tasks involved in this PM, the tanks are cleaned with "Piranha Clean" (Sulfuric / Peroxide) to remove the organics from the sink, as there is photoresist on these wafers that are processed in this tool. The data revealed the most affected lot was run after the PM and the failure signature diminished as the bath life increased and more wafers were run. Following the next bath change, 6hrs later, all lots returned to nominal parametric behavior. After a thorough investigation, it was found that the post piranha clean rinse was inadequately removing the acid prior to a fresh bath pour of NH_4OH. This made the NH_4OH ineffective in its ability to remove Indium oxides and thus blocked (or micro masked) the HCl etch from removing InGaP. The cleaning procedure in the PM involves a manual spray rinse of the tank followed by 3 tank fill / dumps of DI water. In order to determine the effective removal of piranha chemical, the pH of the NH_4OH tank was measured after each fill/dump rinse. It took 5 fills and dumps for the tank DI water to measure the same as the incoming (control) DI water. This proved the root cause was inadequate rinsing of the tank post Piranha Clean.

Case #2. With the gross failures and wafer scraps eliminated, focus turned to the final yield loss area to be investigated. The yield loss existed around the edge of the wafer. The GFA was always to one side of the wafer, showing some sort of misalignment was involved. Occasionally, the GFA would cross through a PCM and this data revealed a signature similar to that of InGaP non-removal. Failure analysis confirmed this to be the case. The most significant finding in the investigation was a commonality of the PVD tool that sputters the Egate metal, just prior to the Dgate module construction. This is a multi-chambered tool, however, wafers with the GFA were always from one specific metal sputter chamber. Inspection and measurement of the chamber shield revealed it was slightly misaligned to one side. An experiment, deliberately misaligning the chamber shield to one side and then the other, proved misalignment of the shield to cause the failure. The experiment showed sputtered metal as far out as the wafer's bevel. Product die adjacent to this region showed InGaP non-removal related failures at die sort. In addition to shield misalignment, the maximum opening was found to have an impact as well. Over time, the shield opening widens by erosion from repeated bead blasting in the shield cleaning maintenance procedure. In cases where the shield opening is too large, failures can occur around the entire edge of the wafer. The larger opening in the shield allows metal to be sputtered further out to the edge of the wafer, in the area, such as the bevel, where there is no photoresist coverage, thus no possibility of clean lift-off. The remaining metal at the wafer edge remains exposed in the subsequent processing steps. Specifically, when the alternate gate module is processed through the plasma etch step, the edge metal impacts the InGaP etch by interacting with NH_4OH sink chemistry (exposed edge Egate metal impacts Dgate InGaP removal for example).

Case #3. Not long after the elimination of failures from Case #2, a similar signature of edge die failures for DFET

switching speed arose. The failures only happened on the process flow containing both EFETS and DFET transistors (a DFET-only sub-flow did not exhibit the GFA). This implied that there is an interaction between the EFET metal in the flow, deposited before the DFET construction, and the failures on DFETs, similar to Case #2. The investigation revealed tiny holes in the Dgate photoresist after the develop step. The holes were found around the extreme wafer edges. The mechanism was the Dgate etch burrowing through the holes and exposing the underlying E-Gate metal from previous processing. Thanks to prior knowledge from Case #2, it was known that even the smallest amount of metal exposed on the wafer during InGaP etch, the etch will be blocked in a large area round that region. In this case, although the holes were extremely small and all the way out to the edge of the wafer, the retarding of the InGaP etch impacted several die at the edge of the wafer.

The fix for this process marginality was discovered by a Lithography Engineer who was running an experiment on a previous generation pHEMT process, known as QPED. The experiment involved a backside rinse on a develop track (to remove backside particles). It was found that adding a backside rinse recipe caused InGaP non-removal problems on QPED, which had been previously unaffected. The findings were tested using an engineering split lot. Inspection showed the backside rinse recipe that caused InGaP non-removal was splashing DI water onto the frontside of the wafers, eroding the solvent rich photoresist at the edge of the wafer and exposing this area to be etched by the Dgate etch. As previously mentioned, the metal exposed retards the effectiveness of the InGaP etch in and around the vicinity of the exposed metal. The process was made more robust with learnings from margin study experiments related to the photoresist coat and backside rinse.

SUMMARY

Multiple case studies were covered, where unique electrical failure modes were all due to an incomplete removal of an InGaP layer under the gate of a pHEMT device. There were various and unique reasons that occurred in the manufacturing process which ultimately caused yield loss and wafer scraps. In each case, a fix was implemented resulting in a more robust process.

This paper has demonstrated the importance of reacting quickly to major scrap events and die sort yield loss. Through the use of failure analysis, die sort wafer maps, and keeping an open mind that there may be many sources of defects that cause a similar parametric signature. This case, it was InGaP non-removal. The elimination of each source to the defect has created a robust, high yielding process.

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ACRONYMS

pHEMT: pseudomorphic high-electron mobility transistor
DFET: Depletion-mode field effect transistor
EFET: Enhancement-mode field effect transistor
PCM: Process Control Monitor
InGaP: Indium Gallium Phosphide
GFA: Gross Failure Area