Templated Liquid Phase Growth Combined with MOCVD for Growth of Crystalline III-V's Directly on Oxide and Nitride Surfaces

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Abstract

Initial results of a material growth scheme to potentially directly integrate crystalline III-V semiconductor based devices on amorphous oxide and nitride surfaces, are reported here. "Remote" islands of crystalline InP are first grown on Si/amorphous SiO2 wafer using Templated Liquid Phase (TLP) growth process. Mesas of indium are deposited on the chip, followed by phase transformation to single crystalline InP in presence of phosphine. This pre-grown III-V layer is then used as a seed for MOCVD overgrowth in order to obtain single-crystal compound semiconductor film on amorphous substrates. This growth scheme would potentially allow to leverage the significant advances made in III-V based electronic and optoelectronic devices, by inexpensive and high yield integration with CMOS and silicon integrated photonics platforms.

INTRODUCTION

The integration of III-V active components with CMOS and silicon integrated photonics platforms remains a challenging and costly process. Many current state of the art approaches proceed via wafer bonding of an active layer and subsequent etching of the III-V growth substrate, adding significant processing cost, time, and yield reduction. Despite these drawbacks, the devices which are placed on the substrates are excellent quality, and this approach enables tiling multiple different materials over a silicon wafer on a chip-level scale.

Recently, a procedure by which growth of single crystalline III-V mesa's directly on non-epitaxial substrates such as metals, silicon dioxide, and silicon nitride [1-6] has been developed. This growth approach, termed Templated Liquid Phase (TLP) growth, is carried out by first depositing a patterned group III template in the desired location, and then heating in an ambient of the desired group V. Through tuning of the growth process, a single crystal of the III-V will grow in each template. The key advantage of this process the ability to directly grow a single crystalline III-V material in the desired geometry and location via a monolithic process. Using this approach, we have demonstrated growth of InP, InAs, GaP, and other III-Vs [5]. Additionally, we have used TLP to demonstrate InP FETs [3,4] and neuromorphic devices on Si/SiO_2 [4].

Here, we present a process which uses TLP growth of InP on SiO_2 and Si_3N_4 to first create a "remote" crystalline InP surface on the insulator surface. Using those templates, we then epitaxially grow InP using selective area MOCVD on the InP mesa. While MOCVD InP on TLP InP is used as a demonstration, this approach is general, and could enable to use of MOCVD epitaxial layer growth on oxides and nitrides through a "remote substrate" approach.

RESULTS AND DISCUSSION

Templated Liquid Phase Growth: Overview

First, we introduce the templated liquid-phase (TLP) growth technique for crystalline InP growth on any substrate. Figure 1 schematically illustrates the general TLP process flow. Indium mesas of the desired geometry are deposited on SiO_2 (thermally grown) or Si_3N_4 (LPCVD deposited) on Si handle wafer, and capped with SiO2. The entire chip is then taken to a CVD furnace and heated to the growth temperature (above the melting point of indium), and phosphine is introduced as precursor for phosphorus. InP precipitates in each template, and the phosphorus flux is controlled to maintain the supersaturation such that the rate of nucleation is less than the rate of growth, to obtain a single crystal in each template. With time, the entire indium in the template is transformed to InP. Figure 2 shows SEM images of TLP growth of InP in an indium template at various stages of growth, starting with a single nucleus, and ending with the circular template geometry defined by the indium mesa.

TLP InP Optoelectronic Quality

Steady-state photoluminescence curves of this TLP InP is shown in Figure 3 (a), and compared with that of a commercially available InP wafer. Good quality of the grown material is indicated by comparable peak position and full width at half maximum. Quantitative photoluminescence analyses in Figure 3 (b) show the TLP InP to be of competitive optoelectronic quality, with the theoretical maximum of the open circuit voltage being 45 mV within that of InP wafer under similar illumination conditions.

Selective Area MOCVD InP Growth on TLP InP

The capping SiO_2 layer is etched away by dilute HF etching, and these TLP-grown InP mesas are then taken as seeds to epitaxially grow InP using MOCVD. Figure 4 (a) illustrates the general concept. Top-view SEM images of some mesas grown with TLP and regrown with MOCVD are shown in Figure 4 (b). Clearly, a faceted crystalline geometry is observed to be showing up, indicating the single-crystal nature of the template underneath. The growth condition, however, gives rise to stacking faults, and thus needs to be optimized to potentially give InP with better morphology.

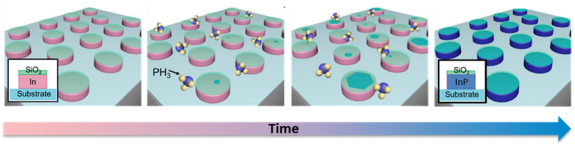

Fig. 1. Schematic of the TLP growth process.

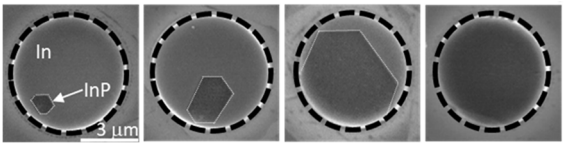

Fig. 2. SEM image of InP nucleating in indium template and gradually growing to completely transform the indium entirely to InP.

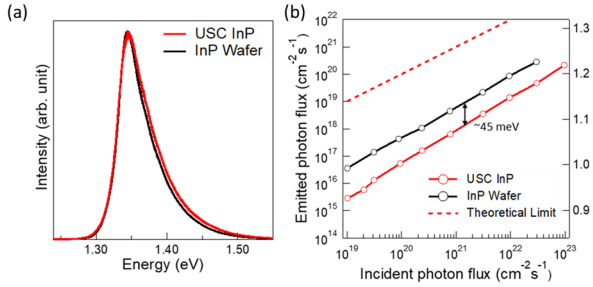

Fig. 3. (a) Steady-state PL of TLP InP compared with that of InP wafer, indicating similar qualitative characteristics, (b) External photoluminescence efficiency of TLP InP compared with that of InP wafer, indicating competitive opec-circuit voltage characteristics.

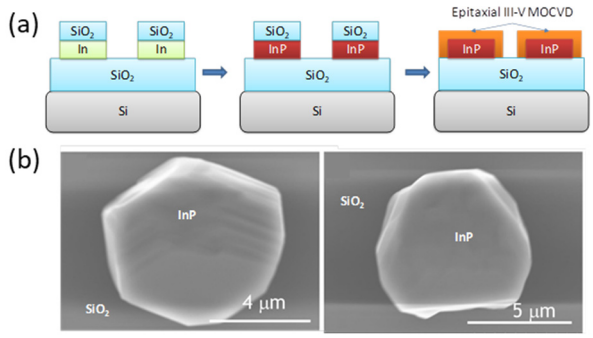

Fig. 4. (a) Schematic illustrating TLP growth of InP single crystalline mesas on SiO_2 followed by epitaxial growth using MOCVD on the mesas. (b) Representative SEM images after both TLP and MOCVD of InP have been carried out.

CONCLUSIONS

In summary, a potentially new method of integrating III-V active devices with Si CMOS and silicon integrated photonics is introduced. Single crystal templates of InP are first obtained on amorphous oxide and nitride surfaces using templated liquid phase method. TLP InP shows optoelectronic quality similar to that of commercial single-crystal InP wafer. Using the TLP InP as seeds, InP is regrown epitaxially using MOCVD, thus opening a potential inexpensive way of integrating high-performance III-V devices on Si. While InP on InP is used as a demonstration, this approach is general, and could enable to use of MOCVD epitaxial layer growth on oxides and nitrides through a 'remote substrate' approach.

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ACRONYMS

TLP: Templated Liquid Phase
MOCVD: Metal-Organic Chemical Vapor Deposition
LPCVD: Low Pressure Chemical Vapor Deposition
SEM: Scanning Electron Microscopy