Layer transfer of high-voltage, GaN-on-GaN pn diodes through epitaxial lift-off

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Abstract

An epitaxial lift-off (ELO) process based on bandgap-selective photoelectrochemical (PEC) wet etching of an InGaN release layer was used to transfer high-voltage GaN pn diode device structures from native GaN substrates to copper thermal carriers. Bonding of the transferred devices was performed using a low-temperature sintered silver nanoparticle paste. Very similar pn diode device characteristics were observed before and after layer transfer, and optical as well as electrical methods were used to verify a 30% reduction in thermal impedance for the transferred devices. The feasibility of bulk GaN substrate reuse has also been demonstrated.

INTRODUCTION

Epitaxial lift-off has been widely explored for III-nitride devices as a means to improve optical, thermal and mechanical device performance characteristics, as well as to enable heterointegration of GaN components with other device technologies. ELO has previously been carried out on high dislocation density GaN films grown on non-native substrates such as sapphire or SiC. The recent emergence of large-diameter, native GaN substrates has stimulated development of vertical GaN power devices that require low dislocation density to reach their full potential. Vertical GaN architectures offer the possibility of compact, multi-kV switching devices with substantially reduced R_{on} and higher switching speeds compared to conventional, Si-based power electronics [1].

Epitaxial lift-off is an enabling technology for emerging GaN-on-GaN power electronics as it addresses multiple device performance and economic barriers. The thermal impedance of native GaN substrates limits the maximum power density, which leads to larger die sizes. Layer transfer of GaN epitaxial structures to high thermal conductivity substrates such as copper or diamond can enable higher power densities. The native GaN substrate can also be reused after ELO [2], which can mitigate the considerable substrate cost.

The design and composition of the release layer is critical to maintaining high material quality when growing GaN-on-GaN ELO structures. Release layer materials such as CrN [3] or Nb_2N [4] have been successfully applied to GaN ELO from non-native substrates such as sapphire or SiC but have a large mismatch relative to bulk GaN. In this work we have used release layers composed of InGaN, with compositions and thicknesses that are pseudomorphic on native GaN. As described in more detail previously [5], selective etching of the InGaN release layer is carried out using bandgap-selective PEC wet etching using KOH solutions. The release layer is illuminated through the backside of the bulk GaN substrate using photon energies below the bandgap of GaN, which are selectively absorbed in the InGaN release layer. The photogenerated holes facilitate the oxidation and electrochemical dissolution of the release layer. Using a perforation process, we have lifted off wafer-scale GaN films from 2-inch bulk GaN substrates, as illustrated in Figure 1.

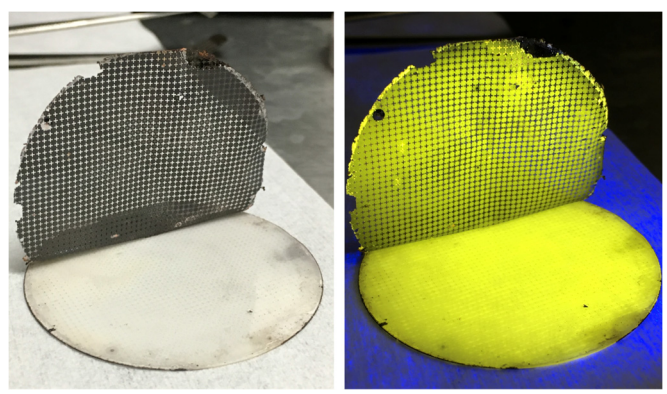

Fig. 1. Photographs of a fully released GaN epitaxial film from a two-inch bulk GaN wafer. The wafer shown at right is under ultraviolet illumination to stimulate luminescence of the lifted-off GaN film and substrate. The released GaN foil is supported by a plated, perforated metal support layer.

EXPERIMENTAL

Figure 2 (a) shows the epitaxial layer structure used for high-voltage pn diode fabrication. Samples were grown by MOCVD on bulk GaN substrates produced by HVPE. The ELO structure contains an i-InGaN release layer beneath the n+ GaN cathode layer. Nominally identical structures (not shown) were also grown on bulk GaN substrates without a release layer for comparison to the ELO structure. Figure 2

(b) shows a schematic cross section of the fabricated pn diode device. The device fabrication process has been described previously [6] and uses a shallow trench etch and triple nitrogen implant for edge termination to support high-voltage operation. Low-resistance p-GaN ohmic contacts were patterned using evaporated Ni/Au (20/500 nm) annealed at 600 C under nitrogen gas. The top surface of the devices was passivated with sputter-deposited SiN_x. Evaporated Ti/Al/Ni/Au (30/100/50/50 nm) was deposited on the backside of the GaN control wafer (without release layers) to form the cathode contact, while evaporated Ti/Au (40/100 nm) was used for the ELO backside n-type contact.

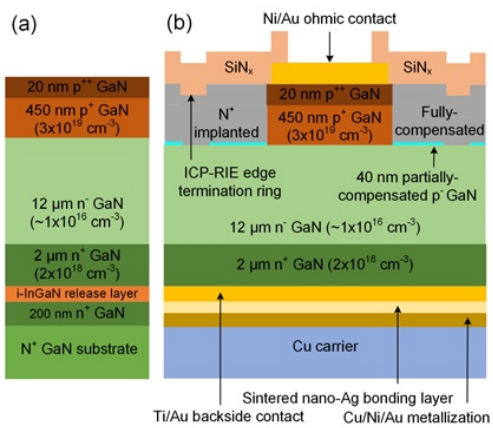

Fig. 2. High-voltage GaN pn diode heterostructure (left) and bonded device structure (right) [7].

The epitaxial lift-off process involves first encapsulating the fabricated devices on the GaN substrates with sputter-deposited TiW-Au seed metal and a 25-µm plated metal support layer [5]. This structure protects the devices during the ELO process and supports the semiconductor film after lift-off and during the layer transfer process. Cross-shaped perforations were formed in the metal support layer and were etched through the semiconductor layers down to the release layer using a combination of dry and wet etching. The ELO process was performed in KOH solution, with the GaN sample acting as the anode and with a Pt cathode, as shown in Figure 3. The bulk GaN substrate was illuminated from the backside using filtered UV wavelengths that transmit through the GaN substrate but absorb in the InGaN release layer, driving the photoelectrochemical etching process. Etching of the release layer occurs through all of the perforations across the wafer, which are typically spaced on a 1-mm or larger pitch.

Figure 4 (a) outlines the processing steps for transferring the lifted-off GaN foil to a Cu submount. As described previously, after lift-off a Ti/Au n-type contact was blanket evaporated on the nitrogen face of the released GaN foil. A layer of Kapton tape was then applied to the top, plated surface of the metal support layer. Sintered nanosilver paste [7] was used to bond the lifted-off device film to a Cu carrier followed by annealing at 260 °C for one hour. The nanosilver paste forms a robust bond with excellent electrical and thermal conductivity at relatively low bonding temperatures. After bonding, the Kapton tape is peeled off and the metal encapsulation layer is removed by wet chemical etching that is selective to the device structure beneath.

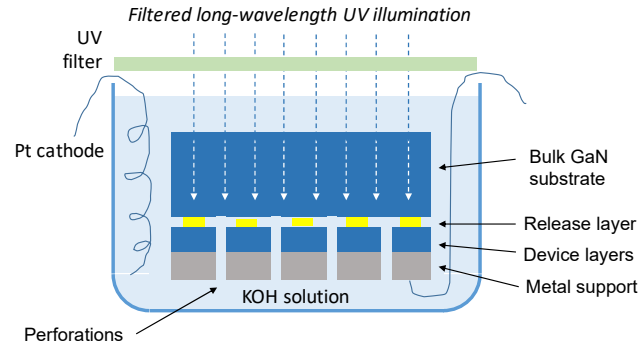

Fig. 3. Experimental setup for ELO by photo-electrochemical wet etching of the InGaN release layer.

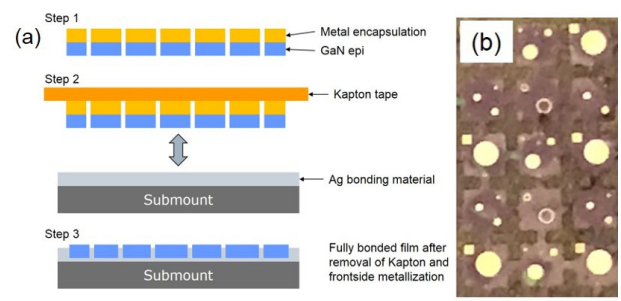

Fig. 4. (Left) Process flow for layer transfer and bonding of the released GaN foil. (Right) Image of bonded GaN pn diode structures.

RESULTS

Figure 5 (left) shows a comparison of measured current-voltage characteristics for pn diodes fabricated on bulk GaN substrates without a release layer (control), and after ELO and layer transfer. The I-V curves are very similar, with modestly higher current in the control devices at higher biases. Seen at right are the extracted ideality factors and on resistances for the two devices. The ELO diodes have slightly higher on resistance (0.5 $m\Omega cm^2$ vs 0.2 $m\Omega cm^2$), which can be attributed to the use of unannealed n-type contacts on the ELO devices. The ideality factors are identical for the two devices, which is significant since the ideality factor is sensitive to defects and recombination centers in the depletion region. The ELO process, layer transfer and bonding processes have not introduced defects that measurably impact device performance.

The reverse bias current-voltage characteristic, shown in Figure 7, is also sensitive to material quality and defects. The motivation for using bulk GaN substrates is to achieve low dislocation density and enable devices with low reverse bias

leakage current and high breakdown voltage. Both control and ELO devices shown in Figure 6 exhibit abrupt breakdown at approximately 1.3 kV. The failure mechanism in both cases was found to be due to imperfect edge termination, rather than defects within the diode junction region.

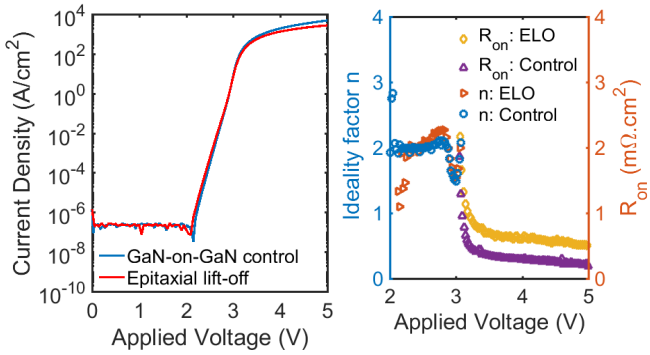

Fig. 6. Shown for both control and epitaxial lift-off pn diodes: (a) measured current-voltage characteristics, (b) ideality factor and specific on-resistance.

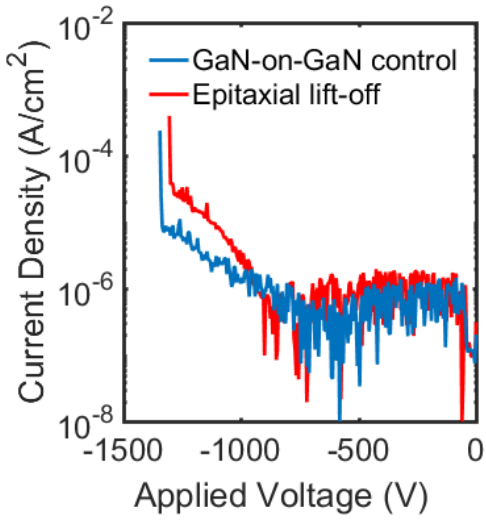

Fig. 7. Reverse bias current-voltage characteristic for control and epitaxial lift-off pn diodes. Both devices show similar reverse breakdown voltages of approximately 1300V.

An important motivation for the GaN layer transfer process is to improve the device thermal transfer characteristics. We have compared the thermal impedance of epitaxial lift-off and control pn diodes using two different methods. The first is to use the temperature dependence of the diode electroluminescence as shown in Figure 8 at left. The peak wavelength of the electroluminescence can be seen to shift to longer wavelengths at higher bias currents. From this wavelength shift (due to the band gap's dependence on temperature), the junction temperature can be estimated and plotted vs power density, as shown at right for ELO and control devices. The thermal impedance, estimated using a linear fit to this data, is 30% lower for ELO devices (9.4 vs 13.8 mK·cm²/W). A second method (data not shown) was also used to estimate the junction temperature using the temperature dependence of the I-V characteristic. The I-V characteristic was extracted using pulsed I-V measurements for devices at different quiescent bias currents. This approach yielded similar estimates of 8.5 and 12.4 mK·cm²/W for ELO and control devices, respectively [7].

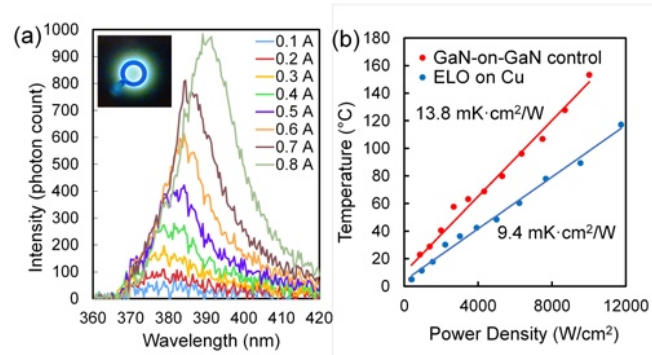

Fig. 8. Shown at left is the electroluminescence of ring-contact pn diode structures under different bias currents. The wavelength shift is used to characterize junction temperature and thermal impedance of GaN-on-GaN control and layer-transferred devices, as shown at right. The bonded ELO devices have 30% lower thermal impedance [7].

As a further validation of the power handling capabilities of the layer-transferred diodes, Figure 9 shows the current-voltage characteristics measured under high forward current injection conditions. A 324-µm ELO device was able to pass 6.5 A of current, while a 550-µm ELO device supported a current of 10 A at a forward bias of approximately 5 V [8]. For comparison, similar control devices measured on the original bulk GaN substrate required a 1-mm diameter to pass 10 A of current [9]. The potential for die size reduction is a key advantage of the ELO process.

The ability to reuse the bulk GaN substrate after ELO is also an important pathway for cost reduction. As an initial test of feasibility, we have fabricated and tested similar pn diode structures both on prime bulk GaN substrates as well as on bulk GaN substrates reclaimed after an ELO process. Approximately 50 µm of material was removed by chemical mechanical polishing of the bulk GaN substrate after ELO, carried out in collaboration with Sumitomo Electric. Figure 10 shows the forward and reverse current-voltage characteristics for similar devices measured on prime and reclaimed substrates [2]. The devices are nearly identical, demonstrating that the ELO and multiple MOCVD growth processes did not damage the bulk GaN substrate. Future work will demonstrate multiple substrate reuses with reduced polishing requirements.

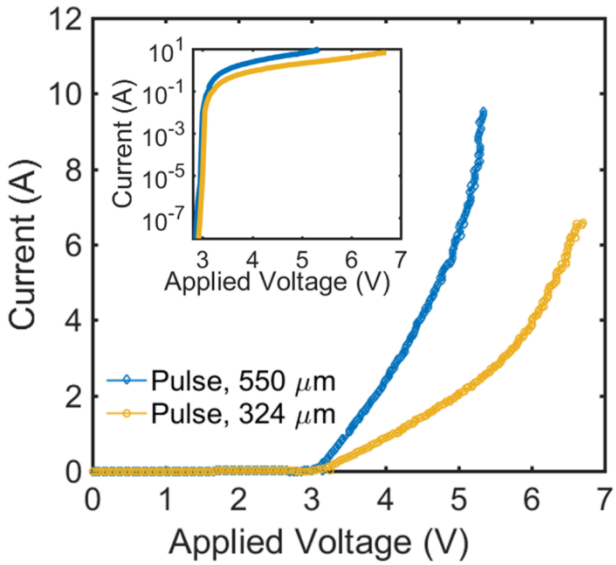

Fig. 9. Measured forward-bias pulsed current-voltage characteristics, illustrating the high-current carrying capability of devices after epitaxial lift-off.

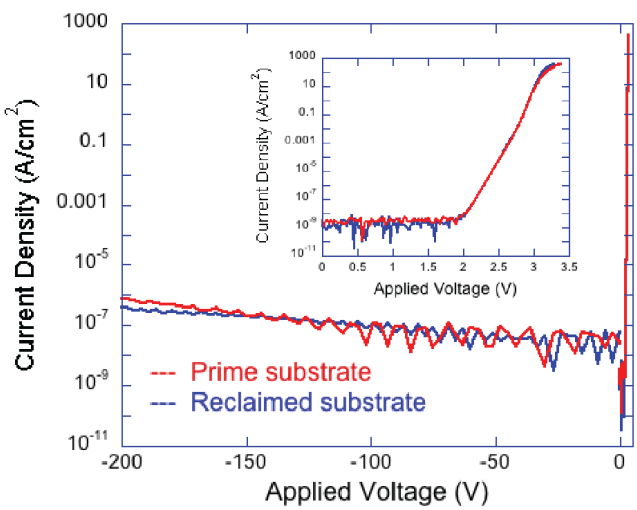

Fig 10. Comparison of measured current-voltage characteristics for a GaN pn junction diode fabricated on a prime GaN substrate and a GaN substrate subjected to epitaxial lift-off, repolishing, and growth and fabrication of a second pn junction diode [2].

Conclusions

A wafer-scale epitaxial lift-off process has been demonstrated for the transfer of GaN epitaxial layers and devices from bulk GaN substrates to thermally conductive copper carriers. High-voltage GaN pn diodes have been fabricated as a vehicle to evaluate layer transfer performance. Epitaxial lift-off devices were found to have nearly identical performance to similar control devices fabricated and tested on bulk GaN substrates. ELO diodes bonded to copper substrates with sintered nanosilver showed a 30% reduction in thermal impedance, validated using both electroluminescence and pulsed I-V thermal measurements. ELO diodes showed a substantial improvement in ability to carry high forward injection current, which enables appreciable die size reduction. The feasibility of bulk GaN substrate reuse after ELO has also been demonstrated, with identical pn diode characteristics measured on prime and reclaimed GaN substrates.

Acknowledgements

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References

[1] I. C. Kizilyalli, A.P. Edwards, O. Aktas, T. Prunty, and D. Bour, IEEE Trans. Electron Dev. 62 (2), 414 (2015).

[2] H. Amano, et. al., J. Phys. D., 51 (16), 163001 (2018).

[3] J.-S. Ha, et al., IEEE Photonics Technol. Lett. 20, 175 (2008).

[4] D. Meyer, B. Downey, D. Katzer, N. Nepal, V. Wheeler, M. Hardy, T. Anderson and D. Storm, IEEE Trans. Semicond. Manuf., 29 (4), 384 (2016).

[5] C. Youtsey, et al., Phys. Stat. Solidi B, vol. 254, no. 8, 1600774-1-6 (2017).

[6] J. Wang, et al., IEEE Electron Device Letters 39 (11), 1716–1719 (2018).

[7] Zhang, Z. and Lu, G.Q., IEEE Trans. Electron. Packag. Manuf. 25 (4), 279–283 (2002).

[8] J. Wang, et al, Int'l Symp. On Compound Semiconductors, paper We1D1.5, Cambridge, MA (2018).

[9] J. Wang, et al, Appl. Phys. Lett. 113, 023502 (2018).

Acronyms

HVPE: Hydride vapor phase epitaxy
ELO: Epitaxial lift-off
MOCVD: Metal organic chemical vapor deposition
PEC: Photoelectrochemical
I-V: Current-voltage