GaN quasi-MMIC HPAs with IPDs on HRS using via first TSV process

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***Abstract* — In this paper, integrated passive devices(IPDs) were fabricated on high resistivity silicon (HRS) substrate with >10 kohms/sq sheet resistivity. The electrical connection between the circuit components to the back side metal was made by through silicon via (TSV) process. With the IPDs and GaN HEMT devices, quasi-MMIC high power amplifier(HPA) was designed and fabricated. The HPA shows 16.6 dB small signal gain, 40.5 dBm peak output power at 3.6 GHz.**

Index Terms — Integrated passive device, Through Silicon Via, GaN HEMT, power amplifier

I. Introduction

To support the requirements of 5G communications, the HPAs need to have high output power, high linearity, high efficiency, low cost and small form factor. [1]

The quasi-MMICs fabricated by hybrid integration of low cost IPDs and high power transistors is one of the most promising technologies for the next generation telecommunication systems. [2] The other solutions such as hybrid HPAs on a printed circuit board(PCB) or monolithic microwave integrated circuits(MMIC) are either too bulky or too costly.

Small foot print IPDs have been developed on high resistivity silicon(HRS), glass, semi-insulating GaAs substrates or as a form of low temperature co-fired ceramic (LTCC). Performance wise, all the above technologies are feasible for high frequency applications. However, in terms of the manufacturing cost and mass production capability, HRS and Glass substrates are better than LTCC or GaAs. [3] Also for high power applications, HRS is more feasible candidate than glass or GaAs substrates because of the superior thermal conductivity of silicon wafers. [4]

IPDs on HRS have been demonstrated with or without TSV. [5, 6] IPDs on HRS with 1000 Ωcm resistivity without TSV is commercially available through an open foundry. [7] To reduce the RF transmission loss, increasing the resistivity of HRS is desirable. Also, to further reduce the foot print of HPAs, it is essential to have TSV process to connect the circuit components on the front side of the substrate to the back side metal.

In this work, IPDs on HRS substrates using via-first TSV process have been demonstrated. The sheet resistance of the 525 um HRS wafers have been maintained >10 kohms/sq throughout the fabrication process. The compact HPAs have been designed and assembled using the IPDs and GaN HEMT devices.

II. Fabrication Process and measurement results

FZ HiRes silicon wafers with 10 kΩcm bulk resistivity was used. About 120 um deep trench was formed on the HRS surface and it was filled with electro plated Cu with TaN diffusion barrier layer. This trench will become a TSV after thinning the wafer by back grinding. After coating the planarized surface with SiNx film by using PECVD, NiCr resistor was formed with sputtering and conventional lift off process. The resistivity of NiCr film was measured 30 ohms/sq. The first metal layer with 0.45 um thick Au layer was formed with e-beam evaporation and lift off process. 3 um thick Au interconnect metals were fabricated with patterned electro-plating. The metal-insulator-metal (MIM) capacitors were formed between the 1st and 2nd interconnect metals with 2900 A thick SiNx dielectric layer. The spiral inductors were fabricated between the 2nd and 3rd interconnect metal layers with W-PR, spin coated dielectric film as a planarization layer manufactured by JSR inc.

After the final passivation and pad opening process, the wafer was bonded to a carrier Si wafer for backside processing. By grinding the backside of the HRS wafer down to 100 um thickness, the bottom of the Cu filled trench was revealed to the surface of the back of the wafer and it forms the TSV. The thickness of the wafer, 100 um, was decided to make the thickness of the IPDs and the commercially available GaN HEMT discrete transistors to be the same. After grinding and polishing the backside, electro-plated Au layer was formed to make electrical connection between the circuit components and the ground plane through TSV. Figure 1 shows the schematic diagram of the IPD process. Once the input and output matching circuits are fabricated using IPDs, HPAs are assembled by hybrid integration of IPDs with GaN HEMT devices [8]. Figure 2 shows the assembly procedure of quasi-MMIC HPA. The GaN HEMT device and IPD circuits were bonded to the package base metal by AuSn eutectic and Ag epoxy, respectively.

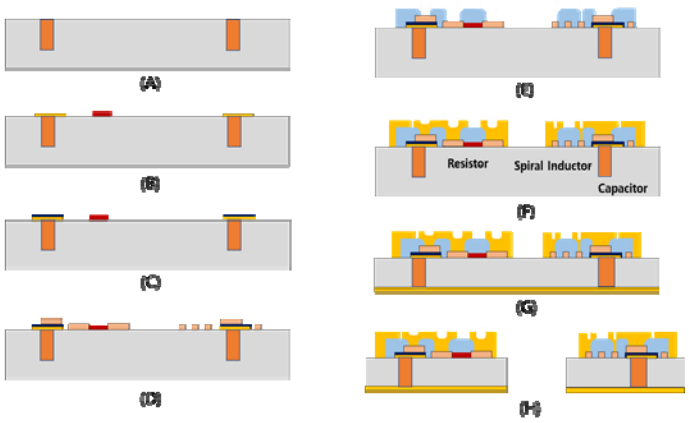

Fig. 1. Fabrication procedure of IPDs on HRS wafers with via first TSV process in alphabetical order. (A)Trench etch and Cu fill, (B) NiCr resistor(red) and metal 1(yellow), (C) SiN_x dielectric layer, (D) metal 2, (E) WPR passivation, (F) metal 2 interconnect, (G) back grinding and metallization, (H) singulation

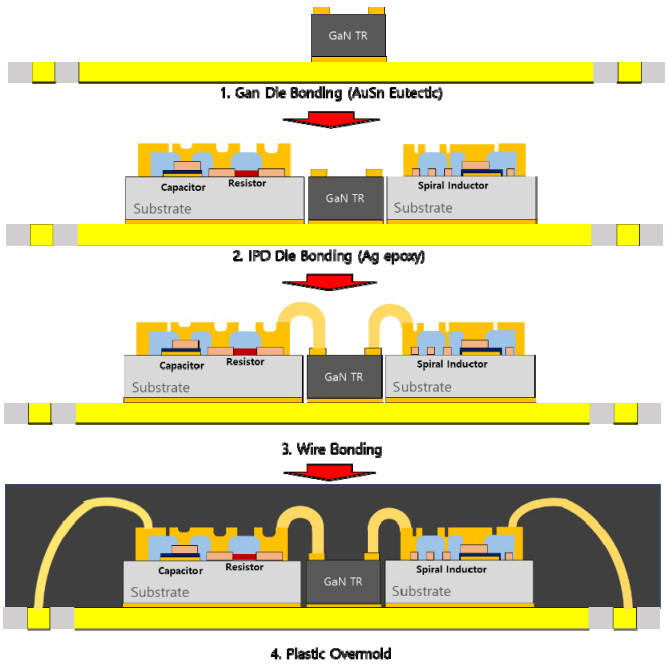

Fig. 2. Process flow of quasi-MMIC assembly by hybrid integration of GaN HEMT devices and IPDs

As shown in figure 3, the HRS wafer was mounted on a blue tape and IPDs were diced with a diamond saw. Figure 4 shows the fabricated RLC passive devices and a cross section of a spiral inductor. The W-PR layer on top of the 2nd interconnect metal coil successfully planarized the topology.

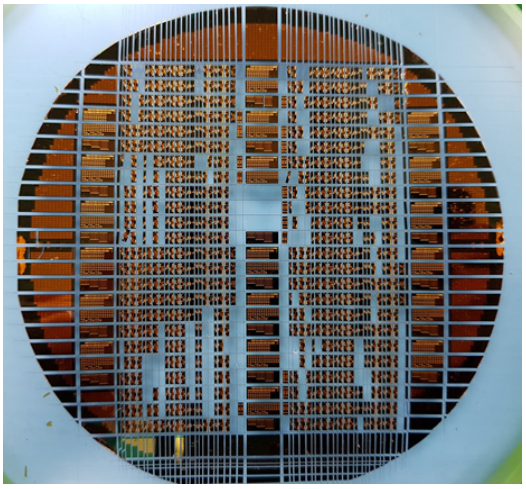

Fig. 3. Fabricated IPDs after dicing and partial die picking

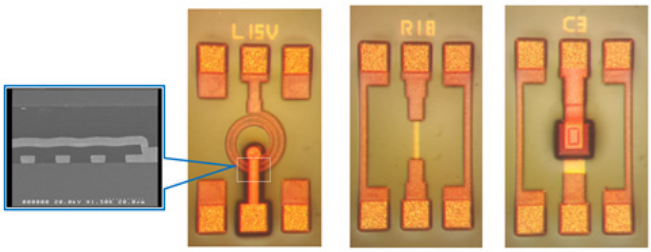

Fig. 4. Fabricated passive devices and the cross section of a spiral inductor.

To extract the intrinsic parameters of fabricated RLC passive devices, de-embedding parasitic components of the electrical pads was performed. As shown in figure 5, the measured and simulated results are reasonably well matching.

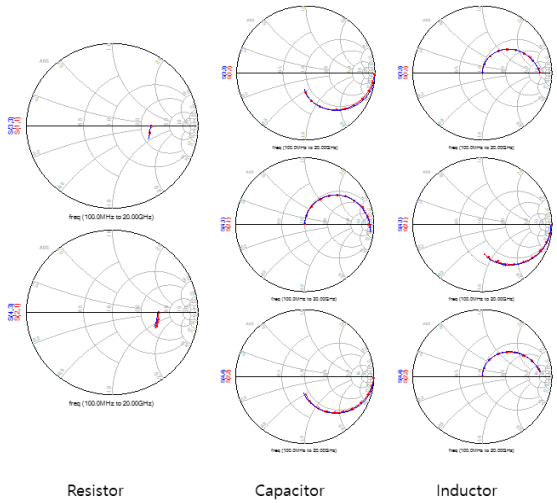

Fig. 5. S-parameter data of RLC devices after de-embedding pad parasitics. Measured (blue line) and simulated (red line) data

III. Results and Discussions on Hybrid packaged HPAs with IPDs and GaN HEMT

To verify the performance of the fabricated IPDs, s-band quasi-MMIC HPA was designed and fabricated. Fig. 6 shows the picture of a fabricated HPA. CGH60008D GaN HEMT device manufactured by Wolfspeed Inc., was used.

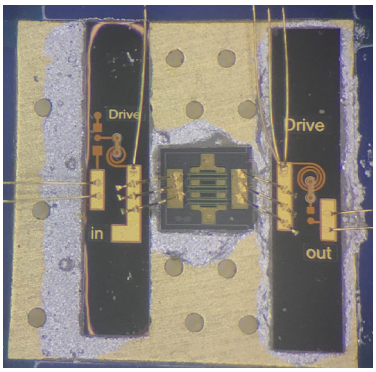

Fig. 6. Optical microscope picture of a GaN quasi-MMIC HPA with Si IPDs

RF characteristics of the GaN quasi-MMIC HPAs were measured using Keysight E3863B PNA. Fig. 7 shows the S21 gain of the simulated and measured data before and after plastic overmold from 2 to 5 GHz range. The S21 gain is shifted after plastic overmold for high frequency range. The peak S_{21} gain of fabricated amplifier was still reasonably well matching to the designed data and was measured as 16.6 dB at 3.6 GHz.

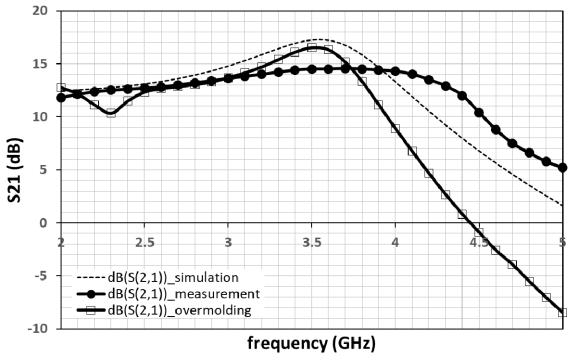

Fig. 7. S21 gain comparison between simulated and measured data before and after plastic overmold for 2 ~ 5 GHz range.

The main reason of the discrepancy was because the simulation was done without considering the plastic overmold material. To see the high power performance and linearity of the HPAs, the output power (Pout), gain, efficiency and adjacent channel leakage ratio(ACLR) were measured with LTE signal at 3.5 GHz center frequency. The peak power was measured as 40.5 dBm. Figure 8 shows the screen capture of the performance at 3.5 GHz center frequency with 33 dBm Pout, which is 7.5 dB back off from the peak Pout.

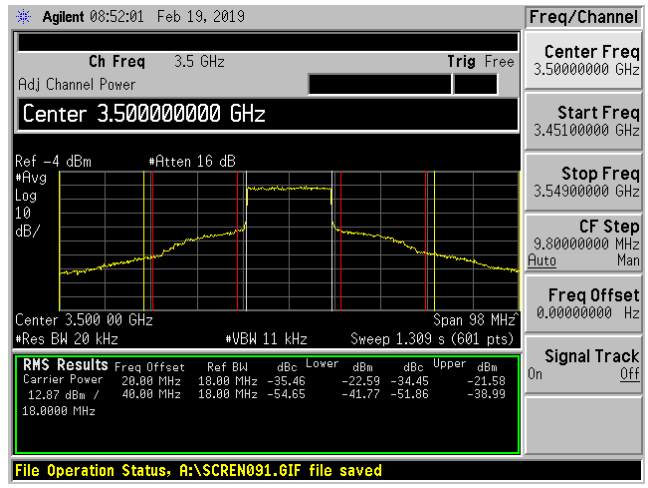

Fig 8. Screen capture of RF test with LTE signal input at 3.5 GHz center frequency and 33 dBm Pout

The gain, drain efficiency, ACLR at 20 MHz band were measured as 8.8 dB, 24.3 % and -34.5 dBc respectively.

From this result, it becomes clear that the RF loss through the silicon wafer is insignificant and thus the resistivity of the HRS substrate has been kept high enough through the fabrication process. The IPD process with via first TSV can be used for low cost manufacturing of high performance and small foot print quasi-MMIC HPAs.

IV. Conclusion

In this report, high performance IPDs were demonstrated on HRS wafers with >10k ohms/sq resistivity and via first TSV process. The intrinsic parameters of the IPDs after de-embedding pad parasitic components were well matched to the simulated data. With this IPDs, hybrid packaged GaN quasi-MMIC HPAs were designed and fabricated. Excellent RF performance of HPAs was measured. The IPD process developed in this work can be applied to manufacture high performance HPAs for the next generation telecommunication systems where high performance and small foot print of HPAs are required with reasonably low manufacturing cost. Using the automated chip embedding technique on top of the same basic fabrication process, high power HPAs with wafer level packaging process has been designed and the fabrication is in progress.

Acknowledgement

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