A High Uniformity, High Yield 0.15 μm pHEMT Technology Manufactured by KrF 248 nm Stepper

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Abstract

In this paper, we report a 0.15 μm pHEMT process whose gate is defined by DUV stepper. Compared with traditionally used e-beam writer, this technology features high throughput and low cost which is suitable for production of commercial MMICs (Monolithic microwave integrated circuit), especially for future 5G mm-Wave applications. After process optimization, excellent device performances such as, P_{out} (output power) of 553 mW/mm, Gain of 11 dB and PAE (power added efficiency) of 50% were achieved at 30 GHz. A consistent CP (chip probing) yield > 98% was achieved with a very tight control of gate process at Wavetech.

INTRODUCTION

Traditionally E-beam lithography was used to realize 0.15 μm gate or beyond for pHEMT technology, but low throughput and high cost are issues which need to be addressed for high volume production. By leveraging UMC's advanced photolithography technology, Wavetek is the first to lead industry volume production in using DUV (Deep Ultraviolet) stepper to define 0.15 μm E-mode & D-model pHEMT optical gate. This is suitable for future 5G mm-Wave MMIC which requires high volume & low cost production capability [1, 2, 3]

DEVICE STRUCTURE & PROCESS

The SEM (Scanning electron microscope) cross-section image of our 0.15μm pHEMT device is shown in Fig. 1. The E-mode (Enhancement mode) & D-mode (Depletion mode) pHEMT of Vth/Vp (threshold voltage/pinch off voltage) are about 0.3 V and -0.69 V respectively. The Vth/Vp map obtained by the wafer probe test can be found in Fig. 2 & 3. The standard deviations of Vth & Vp is around 13mV, which is comparable to that of Wavetek's 0.25 μm pHEMT technology. This demonstrates a good gate control capability of our DUV stepper lithography process and gate etching process.

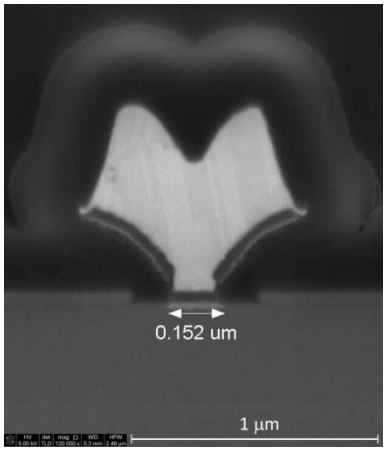

Fig. 1. The cross-section SEM image of 0.15 μm gate.

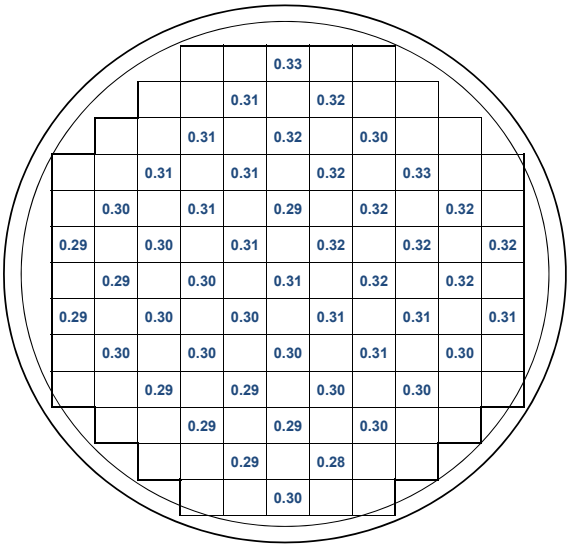

Fig. 2. The wafer map of 0.15 μm E-mode gate.

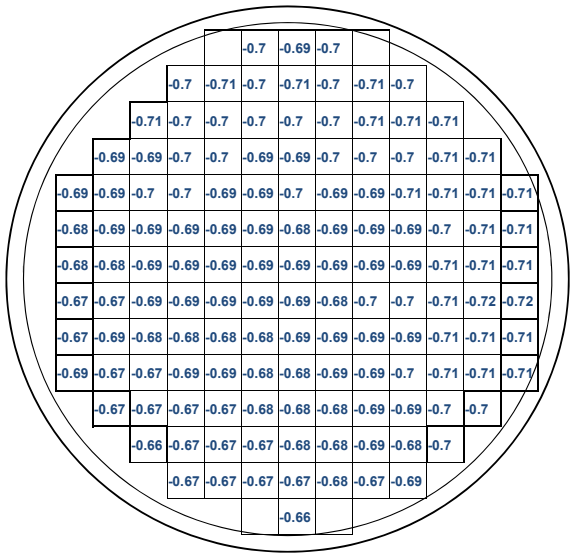

Fig. 3. The wafer map of 0.15 µm D-mode gate.

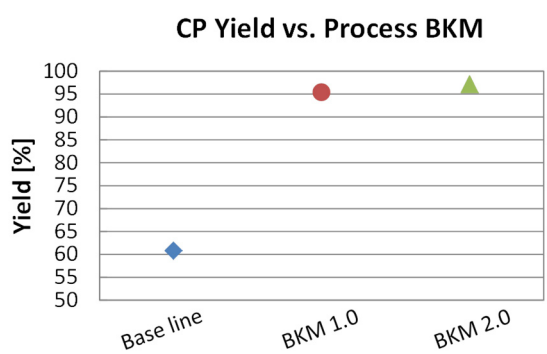

Fig. 4. CP yield improvement by effect process BKM.

GATE YIELD

As shown in Table I, our CP test conditions & targets on D-mode pHEMT are listed and described for items IDQ (Quiescent drain current), IDS_LEAK, and IGS_LEAK that can be further analyzed with the contribution rate. As shown in Fig. 4, we handled two kinds of process BKM (Best known method)) to achieve higher CP yield. By implementing BKM 1.0, yield can be improved by around 2~30 % while, BKM 2.0 can further enhance additional 3~5% to obtain the final yield of 99.33%. The stable yield trend chart with data collected over time can be found in Fig. 5.

Table I. CP Test conditions of 0.15 µm D-mode pHEMT

Test items	Source	Drain	Gate	Target
IDQ	0 V	2 V	0 V	40 mA
IDS_LEAK	0 V	4 V	-1.3 V	0.5 µA
IGS_LEAK	2 V	2 V	-1.5 V	5 µA

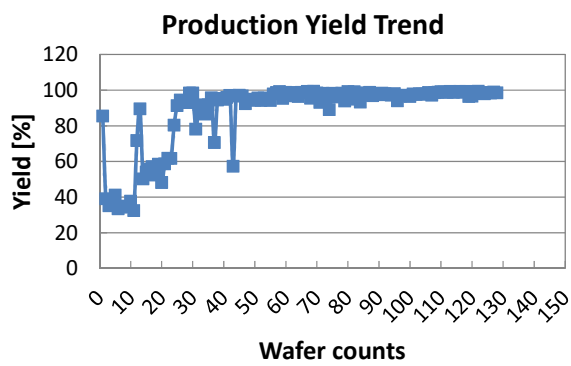

Fig. 5. CP yield improvement by effect process BKM.

Fig. 6 shows the IDS_LEAK distribution across 6-inch wafer. It is obvious that 99.33% of the shots on the wafer are within our spec (0.5µA). The low yield loss (smaller than 1%) demonstrates that the gate pattern is well controlled by our optimized BKM. [4, 5]

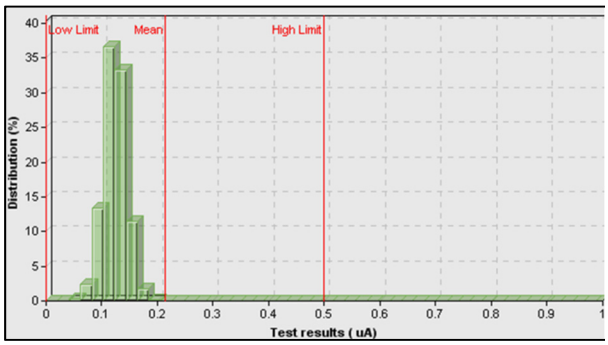

Fig. 6. IDS_LEAK yield loss distribution of 99.33% device.

DC & RF PERFORMANCE

The DC transfer curve of E-mode pHEMT with 4x75um gate finders was presented in Figure 7 that Ids= 350 mA/mm at Vgs=0.9V and maximum extrinsic transconductance (Gm max) = 850 mS/mm at Vgs=0.72V. The typical ft (cut off frequency) of 100 GHz and fmax (maximum oscillation

frequency) of 177 GHz are regularly achieved in E-mode devices which shown in Figure 8.

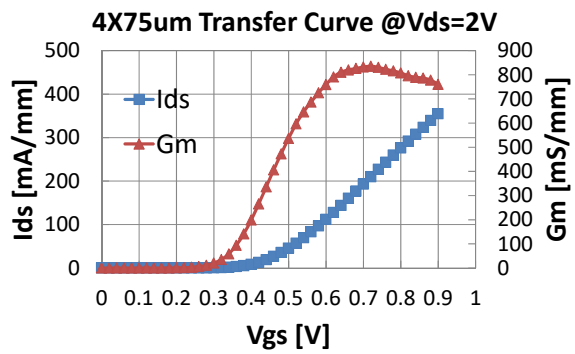

Fig. 7. DC transfer curve of WTK 0.15um E-mode 4x75um device.

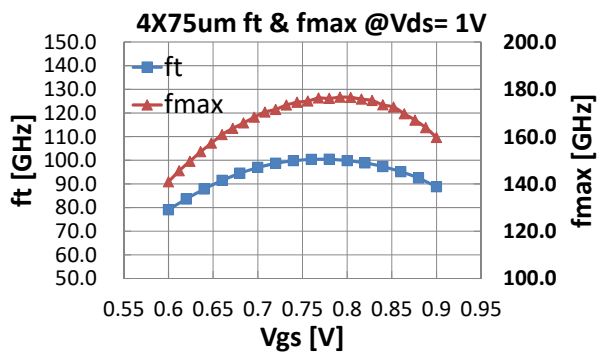

Fig. 8. ft & fmax of WTK 0.15um E-mode 4x75um device.

Noise Performance

Fig. 9 illustrates the frequency sweep of noise figure performance of a D-mode device with gate configuration of 4x40 um tested under the biasing condition of Vds=2V & Ids=10 mA.. Excellent NFmin value of 0.38 dB & associated gain of 13.5 dB are measured at 12GHz simultaneously

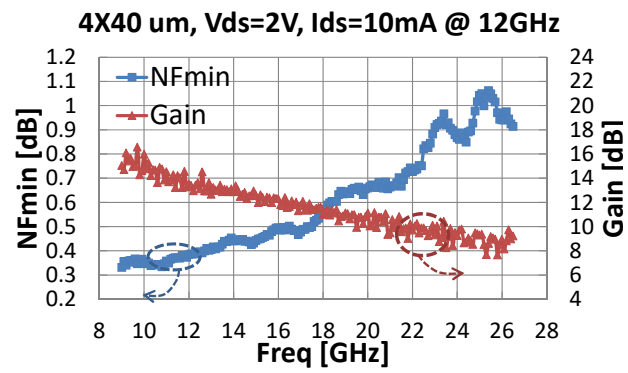

Fig. 9 Yield trend chart showing stable yield with BKM 2.0.

Power Performance

For a 4x75 µm E-mode device biased at Vds of 5V with current density of 72A/mm, its minimum noise figure (NFmin) at 28 GH is found to be below 1 dB. To verify the performance of the presented 0.15 µm E-mode pHEMT process using DUV stepper, a one-stage common source power amplifier has been designed. The common source connected transistor is the amplification stage, which employs a 4x75 um-finger (a total gate periphery of 300-µm) device. Several series and shunt transmission lines are used for input and output matching networks. The capacitors are adopted for dc block and bypass networks. The power amplifier draws 60-mA quiescent DC current from a 5-V supply voltage. The measured power sweep results are presented in Fig. 10. The measured P_{SAT} (saturation output power) is 22.2 dBm and the peak power added efficiency

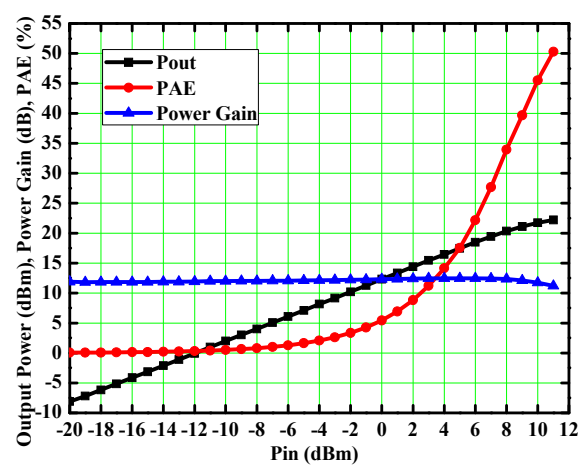

Fig. 10 Power sweep of one-stage common source power amplifier.

(PAE) is up to 50% at 30 GHz. The power density greater than 553 mW/mm can be achieved. The experimental results show that our 0.15 μm technology can serve as a good platform for the demanding mm-wave circuit designs.

CONCLUSIONS

This paper presented the first production worthy DUV defined 0.15um E-mode pHEMT technology, which results in a high production yield consistently exceeding 98 %. The superior performance and cost-effectiveness make WTK's 0.15 um E-pHMET foundry process to be a high potential candidate for future 5G mm-Wave MMIC applications.

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ACRONYMS

CP: Chip probing
BKM: Best Known Method
IDQ : Quiescent drain current
PAE : power added efficiency