Development of stepper solutions for new IoT device challenges

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Abstract

To meet various process requirements from growing IoT devices, Canon released FPA-3030i5+ and FPA-3030EX6. Both of these are based on the new FPA-3030 platform that is an upgrade of the proven FPA-3000 platform. These steppers have new functions that enable processing of multi-sized wafers, scratched wafers, and transparent wafers. They also offer a new alignment system that detects alignment marks on the backside of wafers.

INTRODUCTION

Internet of Things (IoT) is a major topic in the world. IoT requires many leading edge interconnected devices, sensors and actuators communicating information from physical devices to the cloud. Increasing growth in the sensor and MEMS markets require expansion in fabrication capacity and creation of new chips that adopt new processes making new functional requirements for the equipment.

Canon manufactured i-line steppers (FPA-3000i4, i5, i5+) and KrF steppers (FPA-3000EX4, EX5, EX6) in the 1990s that were widely used in 8-inch System on Chip (SoC) and DRAM production lines. FPA-3000 series can handle wafer sizes up to 8 inches and these steppers have widely been used for non-silicon wafers fabrication after 12-inch silicon wafer processes matured in SoC and DRAM production.

As 12-inch processes ramped up, Canon supported customer demands for wafer sizes less than 8-inch and non-silicon wafer processes through refurbished equipment business. However, it has become more difficult to satisfy customer demands due to electronic parts discontinuation and termination of support for the software development environment. To enable continued, sustainable chip production through usage of the FPA-3000 series, Canon has release the FPA-3030i5+ i-line stepper in 2012 and the FPA-3030EX6 KrF stepper in 2016. The FPA-3030 platform is an upgrade of Canon's proven FPA-3000 platform of steppers and is designed with updated electronic parts and software that enables new development of functions, an updated user interface, and long-term parts availability.

In this paper, we will introduce new functions that have been developed for FPA-3030 series steppers to solve process challenges in fabricating leading-edge IoT devices.

TABLE I
SPECIFICATION OF FPA-3030

	FPA-3030i5+	**FPA-3030EX6**
Wafer Size	8,6,4,3 inch	
Resolution	<0.35um	<0.15um
NA	0.63-0.45	0.65-0.50
Reduction Ratio	5:1	
Exposure Field	22x22 ~ 17x26mm	
Overlay Accuracy	<40nm	<25nm
Exposure wavelength	i-Line	KrF
Reticle Size	6 inch or 5 inch	6 inch
Throughput	8inch / 60shots >105wph	8inch / 60shots >121wph

DUAL SIZE WAFER HANDLING SYSTEM

Previous FPA-3000 systems were configured to handle a single wafer size of 8-inch, 6-inch, 4-inch or 3-inch. However, there are many requests for handling multiple wafer sizes in one stepper. To meet this requirement, Canon developed a dual wafer size wafer handling system. This system automatically changes the size of the wafer that the machine can control in about 10 minutes after a mechanical switch is flipped and machine parameters are updated.

Figure 1 shows the dual size wafer chuck. When set to handle a 3-inch wafer, only vacuum 1 is active. And when settings are changed to handle a 4-inch wafer, both vacuum 1 and vacuum 2 become active. The setting is changed back and forth through machine parameters.

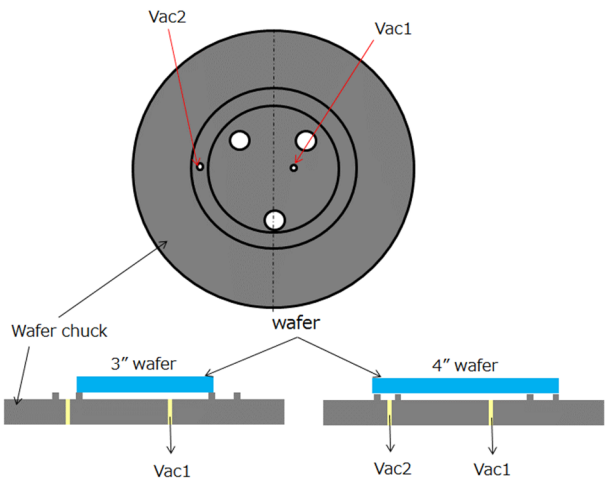

Fig. 1. Dual size wafer chuck

ADVANCED TEMPLATE LEARNING

Another advanced function is the ATL (Advanced Template Learning) function that uses artificial intelligence to detect damaged alignment marks exhibiting random scratch noise caused by fluctuations in the MEMS fabrication process. Figure 2 shows typical scratch noises on alignment marks. ATL is a powerful new alignment function that automatically optimizes alignment parameters to detect damaged marks.

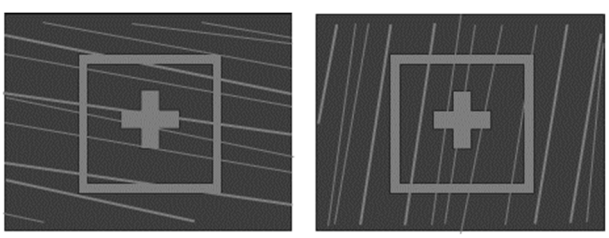

Fig. 2. Alignment mark with scratch noises

With ATL, AI creates a mark template that is more similar to the actual mark image automatically during user production. With more data and feedback, a better mark template is created. Figure 3 shows the correlation between the template mark shape and the actual mark shape over multiple iterations. As optimization time (that is learning count) increases, the correlation ratio increases up to 96.6%. That means the mark detection ratio increases and, therefore, the chance of alignment error decreases.

ATL is also used before production, not during production. For example, user runs 25 sample wafers for AI learning, then good template is acquired and production is done with the template.

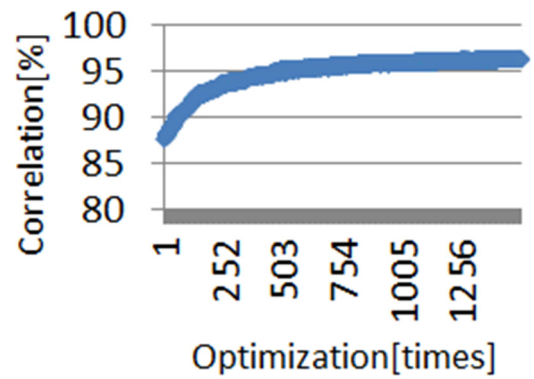

Fig. 3. Improvement of mark correlation by ATL

THROUGH SILICON ALIGNMENT

Canon has also developed new functions such as a Through Silicon Alignment option that provides detection of wafer alignment marks that are underneath (backside) the wafer by scanning through the wafer via infrared light.

As shown in Figure 4, front side alignment is done by a Through The Lens (TTL) alignment scope system (B/C Scope) that observes the alignment marks on top of the wafer. However, backside alignment is done by Through Silicon Alignment (TSA) via an Off-Axis-Scope (OAS) that observes the alignment marks on the backside of the silicon wafer. The wavelength used in measurement is 633nm for the B/C Scope, and infrared light is used for the TSA Off-Axis-Scope system.

Figure 5 shows experimental results of the overlay error of the TSA alignment system. This is evaluated in the following steps. First, the primary exposure is done, then the wafer is etched, flipped and re-entered into the stepper. Then, after the wafer is aligned with TSA detected backside alignment mark, the secondary exposure is done. The overlay error is measured through an external instrument. Hence, the overlay error of 3 sample wafers is less than 121 nm.

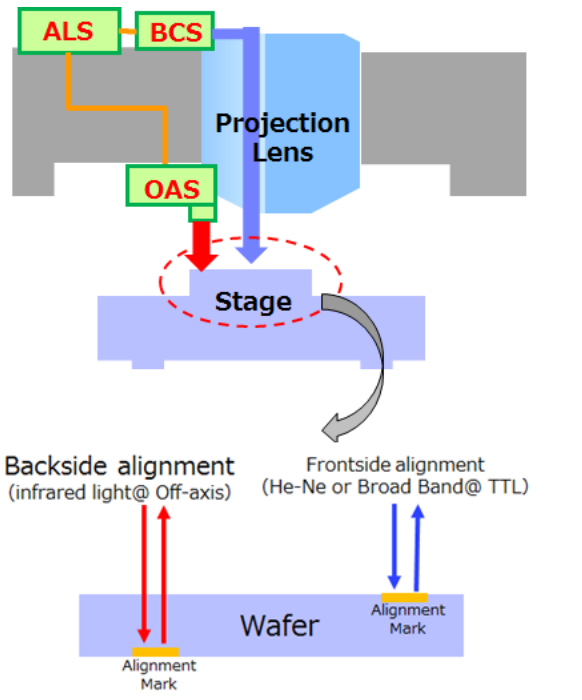

Fig. 4. TSA alignment method

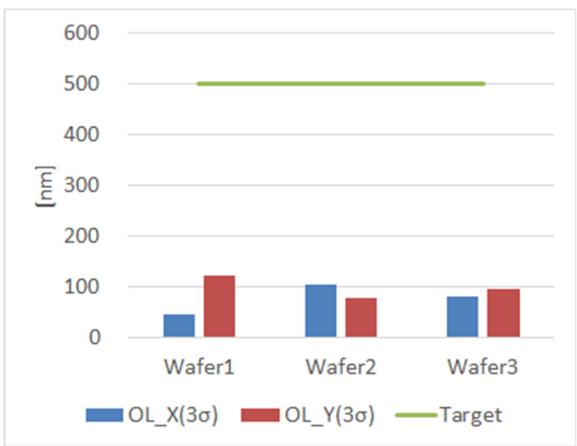

Fig. 5. TSA alignment overlay error

ANTI-REFLECTION WAFER CHUCK

Transparent wafers that almost entirely refract exposed light (ex. Wafers made of Sapphire, Glass or SiC) are used in some processes. The reflected light from the wafer chuck deteriorates CD uniformity and causes an undesired resist pattern on the wafer.

Canon has developed an anti-reflection wafer chuck to solve this problem. The anti-reflection wafer chuck reduces reflectance by diffusing light at the chuck surface. Figure 6 shows a schematic diagram of the anti-reflection chuck. A wafer is supported by many pins in order to avoid contamination. Top surfaces of the pins have small structures to scatter exposure light while maintaining the flatness of the wafer.

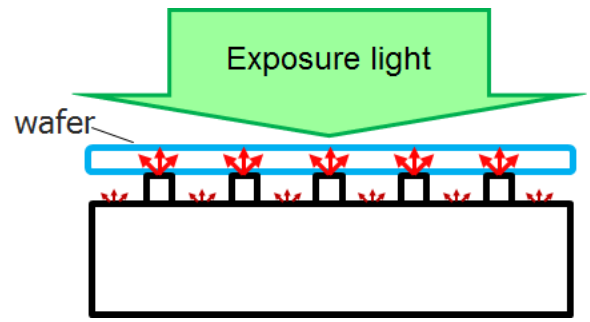

Fig. 6. Anti-reflection wafer chuck

Figure 7 shows the reduction ratio of exposure light reflectance. Reflectance is reduced to 0.35 times by the anti-reflection chuck.

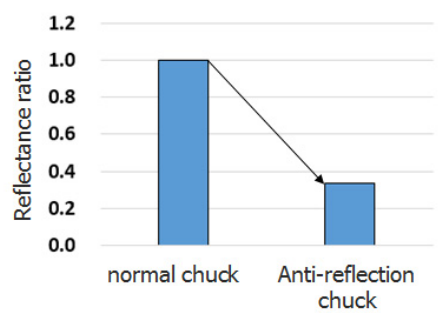

Fig. 7. Reduction ratio of reflectance

CONCLUSIONS

To meet various process requirements from growing IoT devices, Canon released new steppers with new functions.

1) Dual size wafer handling system

An 8 inch wafer handling setting can be changed to a 6 inch setting (or the reverse) wafer handling system in about 10 minutes. Also from 4 inch to 3 inch (or the reverse) is possible.

2) Alignment solutions for scratched wafers.

Alignment mark template are optimized by AI learning, and the correlation between template and real image is improved. This function is a promising solution for assisting in alignment to scratched or damaged wafers.

3) Backside alignment system.

Using infrared light, backside alignment is possible, where a vastly improved overlay performance was attained.

4) Anti reflectance chuck for even transparent wafers.

By usage of an anti-reflection wafer chuck, reflectance is reduced to 0.35 times compared to that of a normal chuck, and this results in better imaging performance for transparent wafers.

Canon is committed to supporting the required manufacturing equipment needed to support the growth of IoT devices and other semiconductor industry innovations.