Application-Specific, Comprehensive Technology and Product Qualification of GaN on Silicon Power Conversion Devices

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Abstract

Based on low-cost, large diameter silicon substrates, normally-off Gallium Nitride (GaN) on silicon (GaN on Si) power conversion transistors are available on the market today. Based on a high electron mobility transistor (HEMT) device structure, these devices behave very differently from their silicon-based counterparts. Such differences make GaN HEMT devices sometimes more sensitive and sometimes more robust to the stresses applied in typical power conversion applications. This paper will cover an application-specific method used by Infineon Technologies to qualify such devices for use in power conversion systems. A typical application profile will be studied and specific GaN on Si HEMT sensitivities (failure modes) and strengths (relative to the application stresses) will be discussed. Device test-to-failure data will be shared as will the results of degradation models for key failure mechanisms. This data will be provided in the context of a comprehensive qualification methodology for technology and devices.

INTRODUCTION

Based on knowledge of silicon device failure mechanisms, qualification procedures have been published by JEDEC (Joint Electron Device Engineering Council) [1] and other institutes (e.g., automotive qualification standard Q101 from the Automotive Electronics Council). These procedures define tests, stresses, durations and sample sizes used to qualify silicon power semiconductor products. The choice of qualification test stresses and conditions is often based on the underlying knowledge and models of silicon device failure mechanisms. Due to fundamental differences between silicon MOSFET and GaN HEMT device structures, materials and behaviors, it is insufficient to apply the existing silicon-based JEDEC or AEC-Q101 qualification tables to GaN devices. Next, 4 components of a comprehensive GaN qualification will be proposed.

OUTLINE OF 4 DIMENSIONS TO CONSIDER IN GAN ON SI DEVICE QUALIFICATION

The first of the four qualification elements is the application profile. Assuring reliable operation of GaN HEMTs to the planned quality level and lifetime requires close cooperation between supplier and user. It all starts with describing the stresses from which a device can suffer during operation in a specific topology. A complete application profile also lists all relevant system level requirements such as output power profile versus time, time at various temperatures and at different relative humidity, and hard or soft switching for a partial list. Resultant stresses on the devices are described in great detail [2,3].

The second element of qualification is the quality requirements profile. This is a general description of the application, customer target lifetime, maximum allowed cumulative failure rate, definition of parametric drift limits, required electrostatic discharge (ESD) rating, operating humidity requirements, and moisture sensitivity level (MSL) rating.

The third qualification element is composed of reliability investigations during development. During the development of Infineon's CoolGaN™ devices, GaN-specific failure modes were thoroughly studied. Failure modes were segregated into two categories: intrinsic failures (those due to inherent wearout of device structure and materials) and extrinsic failures (those due to defectivity or very high process variability). The goal of the reliability investigations is to discover the intrinsic and extrinsic failure mechanisms for each relevant stress, and to find a path of process/design/test changes.

The fourth dimension of qualification is composed of degradation models for key failure modes of GaN devices. These allow predicting failure rates under stated stress conditions and lifetimes. We will later consider degradation models for several key failure mechanisms of GaN devices.

APPLICATION PROFILE

Telecom rectifier (AC-DC) sockets have fairly stressful operating conditions. Such systems are required to operate for long duration in the field with ambient temperatures varying on a large scale and humidity that can reach quite high levels. This application represents a good use case for GaN device qualification, as operating conditions can reach extreme levels. Figure 1 provides a high-level summary of a 2.5 kW telecom rectifier system and the related stresses seen by the power transistors in the PFC section. Three temperature regimes are required to simulate a four-season operation. Four

Telecom rectifier AC-DC socket	
Key device parameters, topology	2.5 kW, 230 V line, CCM hard-switching
Expected lifetime	15 years
Operating lifetime	100 %
Environmental conditions	
Relative humidity	85 %
Profile of ambient temperature (in the box) -% of operating time at each temperature	15 % @ -27.5 ˚C 60 % @ 15 ˚C 25 % @ 72.5 ˚C
Profile of Load conditions % of operating time at each load condition	5 % standby, no load 40 % @ 10-30 % load 50 % @ 30-80 % load 5 % @ 80-100 % load
Device electrical conditions	
Drain source voltage (V_{ds})	Average during off = 400 V Peak depends on I_{LOAD} (max = 460 V)
I_{GS+}	Average = 15 mA Peak = 625 mA for 50 ns
V_{GS}	Average = -3 V Peak = -10 V for 10ns
I_D	Load current average 50% duty-cycle
PWM frequency	65 kHz

Fig. 1: High-level overview of Telecom rectifier application profile

load conditions are described from standby to 80-100% load to cover all possible output conditions of the system. As some device reliability factors are temperature and/or load dependent, it is important to include these in the application profile. The heart of the application profile is a table (see Figure 2) which lists current and voltage stresses in detail. In this table, only the lowest temperature condition is shown (the information for the other ambient temperature operating conditions such as 25 ˚C and 72 ˚C are not included for clarity of this exposition however are also required for a complete reliability analysis). The corresponding time at each load condition is provided, as well as for each load condition the average and peak voltage (during off state) and current (during on state) are described.

Ambient temperature	$R_{DS(on)}$	Load condition	On/off state [average/peak]	Total time duration in this condition [h]	Off: V_{DS} [V]	Off: V_{GS} [V]	On: V_{DS} [V]	On: I_G [mA]	On: I_{load}	P_{lo} [W
-27.5	0.05	Standby	On state average	4.93E+02			0.05	15	1	0.0
			On state peak	6.41E-01			0.075	625	1.5	0.1
			Off state average	4.93E+02	400	-3.0				0.0
			Off state peak	6.41E-01	410	-10.0				0.0
		10-30%	On state average	3.94E+03			0.2	15	4	0.4
			On state peak	5.12E+00			0.3	625	6	0.9
			Off state average	3.94E+03	400	-3.0				0.0
			Off state peak	5.12E+00	420	-10.0				0.0
		30-80%	On state average	4.93E+03			0.5	15	10	2.5
			On state peak	6.41E+00			0.7	625	14	4.9
			Off state average	4.93E+03	400	-3.0				0.0
			Off state peak	6.41E+00	440	-10.0				0.0
		80-100%	On state average	4.93E+02			0.6	15	12	3.6
			On state peak	6.41E-01			0.9	625	18	8.1
			Off state average	4.93E+02	400	-3.0				0.0
			Off state peak	6.41E-01	460	-10.0				0.0

Fig. 2: Details of device switching operation including temperature, voltage and current stress for telecom rectifier application

KEY BEHAVIORS/ FAILURE MODES DIFFERENT FROM SILICON DEVICES

In this section, we will discuss several of the most important failure mechanisms that apply to GaN HEMTs, but not to silicon power FETs. The first we will consider is DC bias lifetime. That might seem surprising since silicon devices are also prone to DC bias failure; for that reason, high temperature reverse bias (HTRB) testing is performed. With respect to failure modes under DC bias, the difference between silicon and GaN HEMT devices is that GaN HEM's - when tested at accelerated voltage and temperature conditions - exhibit a failure rate that depends strongly on voltage. Figure 3 displays accelerated stress time-to-failure data with DC bias and temperature stress applied to samples of Infineon's 190 mΩ CoolGaN™ 600 V e-mode HEMTs. Based on a model extracted from the 5 datasets shown on the left, a simulated application condition (dashed line) of 480 V and 125 ˚C is considered which shows lifetime of 55 years at failure rate of 1 FIT which meets a goal of 15 years.

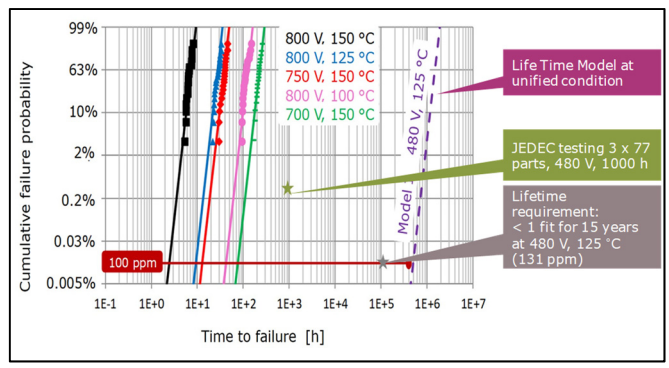

Figure 3: Weibull plot showing cumulative fraction of sample failure vs. failure time for DC Bias (5 series on the left) and modeled operation at 480V, 125C (dashed line).

Note the strong dependence of failure time on bias; devices at 800 V and 125 ˚C all fail in less than approximately 30 hours while devices at 480 V and 125 ˚C are projected to fail at approximately 2 million hours. So although the GaN devices can non-destructively withstand voltage stress much higher than their silicon counterparts, their lifetime at such high voltages is limited. The model shows a lifetime greater than three times the target. The green star indicates the typical qualification time and failure fraction detectable with existing silicon qualification methods - they are insufficient to predict useful life. The gray star indicates the target lifetime that is 15 years at 100 parts per million (ppm).

A second key new degradation mechanism for GaN devices is switching SOA (also known as dynamic high temperature operating life or DHTOL). Along with other semiconductor manufacturers, Infineon has published [4] long-term application switching data, showing stable device

operation (measured as steady case temperature) in hard switching (boost) application over time periods from 1,000 to 3,000 hours.

But 3,000 or even 10,000 hours (corresponding to 18 - 60 weeks) of typical application is obviously not enough to make conclusions for the duration of the intended design lifetime which typically spans years. Therefore, Infineon set up a test platform [5] that allows accelerated stress at higher than designed voltage and current to investigate if the reliability of long-term hard switching operation can be predicted. The device damage in the test circuit was limited in order to allow failure analysis of devices which destruct under test. This circuit operates devices in a hard switching boost configuration such as might be experienced in a PFC or other application circuits.

The Infineon test platform allows testing at accelerated bus voltage up to 700 V (versus typical use condition of 420 V), and at higher than rated device current. Above a certain threshold of peak I-V conditions in testing of samples under accelerated hard switching, device failure did occur over time. A model was extracted that allows failure rate prediction as a function of current, voltage, and frequency. The results of this model are distilled into a repetitive switching SOA curve (Figure 4) that enables circuit designers to avoid operation in I,V combinations that threaten premature failure.

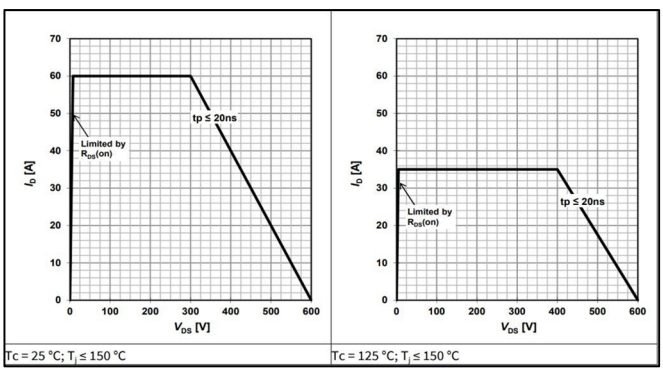

Figure 4: Repetitive hard switching SOA curves define the region of I,V operation in which premature failure is avoided.

Additional accelerated testing was performed with CoolGaN™ HEMTs also in a soft switching operating condition such as routinely occurs in DC-DC converters with an LLC architecture as well as with other topologies. In this case no failures were observed at and beyond those operating conditions at which failures had occurred during testing under accelerated hard switching. This shows that the switching trajectory or locus is very important with respect to possible failure during device dynamic operation (see Figure 5).

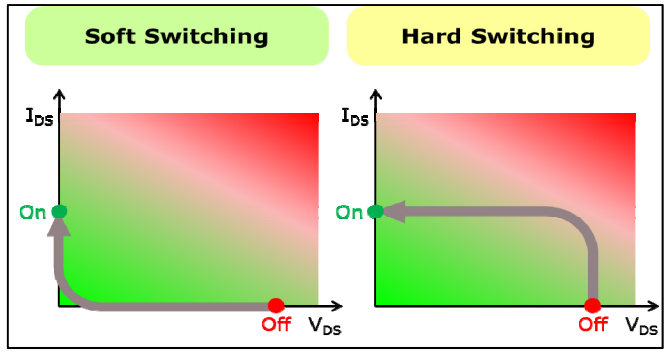

Fig. 5 : For switching SOA the path traversed through I,V matters. Soft switching (left) avoids occurrence of possible switching SOA failure while caution must be taken when operating with hard switching (right).

GaN on Si Device Qualification Elements

At the outset, we referenced existing silicon device qualification requirements [1]which typically include approximately nine standard stress tests (HTRB, HTGB, etc). In addition to these JEDEC tests, as part of technology qualification activities, Infineon has performed ten additional investigatory tests. These were performed to accelerated conditions to stress gate passivation and gate dynamic behavior. Accelerated humidity test was also performed, and behavior over wide temperature range was examined. As an additional risk reduction measure, Infineon's qualification also included eleven different tests at up to 2-5 times the JEDEC specified duration to ensure that unexpected failure or drift behavior would not occur at longer test times. Finally, in addition to the DC bias life and switching SOA models previously referenced, two additional models were generated. These models enable prediction of gate degradation and temperature, humidity and bias (THB) degradation behavior.

Summary/ Applicability to Other Applications.

We have demonstrated how Infineon CoolGaN™ devices are expected to meet typical industry lifetime and quality (cumulative failure rate) targets when operated in totem pole, hard switching PFC topology according to the telecom rectifier application profile. Nevertheless, CoolGaN™ HEMTs fit many other applications and can also be used as a general switch with few exceptions [3].

Conclusions

An application-specific qualification method has been proposed which features an application profile, quality requirements profile, reliability investigations during development and degradation models for relevant failure mechanisms. Examples and results for two such models were shared and a summary of standard and risk reduction-based stress tests were provided. Taken together, these elements

comprise a comprehensive qualification for GaN HEMT devices used in power conversion applications.

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ACRONYMS

HEMT: HIGH ELECTRON MOBILITY TRANSISTOR
JEDEC: JOINT ELECTRON DEVICE ENGINEERING COUNCIL
AEC-Q: AUTOMOTIVE ENGINEERING COUNCIL, QUALITY
ESD: ELECTRO STATIC DISCHARGE
MSL: MOISTURE SENSITIVITY LEVEL
HTRB: HIGH TEMPERATURE REVERSE BIAS
DHTOL: DYNAMIC HIGH TEMPERATURE OPERATING LIFE