JEDEC Guidelines and Standards for Compound Semiconductors

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Abstract

In recent years, the compound semiconductor community has been calling for the development of guidelines and standards specifically for compound semiconductors for a variety of applications, including RF and microwave, power conversion, and optoelectronics. The US-based world-wide microelectronics industry standards development organization, JEDEC, founded in the early 20th century, has been continually "developing test methods and product standards that have proved vital to the development of the semiconductor industry." JEDEC already has developed a comprehensive array of guidelines and standards through its various committees including JC-14 Quality and Reliability of Solid State Products, JC-13 Government Liaison, and the newly formed JC-70 Wide Bandgap Power Electronic Conversion Semiconductors. While some of these guidelines and standards are directly applicable to today's compound semiconductor industry, some may not adequately address the special properties and requirements of wide bandgap compound semiconductor technologies such as SiC and GaN for applications such as RF power, space, and power electronic conversion. In response, JEDEC created a new committee to address the demand for new and expanded guidelines and standards. In this talk, I will cover some of the history of JEDEC semiconductor guideline and standard document development, the structure of some of the relevant JEDEC committees, member company and subject matter expert participation, achievements to date and outlook for future activities.

INTRODUCTION

The compound semiconductor (CS) community needs guidelines and standards for the same reasons that the silicon semiconductor community does. Guidelines and standards are needed for reliability, quality, testing and characterization, datasheet, and many other aspects. A natural place for the CS community to turn for meeting this need is the JEDEC Solid State Technology Association.

JEDEC

JEDEC was created in the early 20th century to formalize solid state device standardization. JEDEC has its origins all the way back to 1924 with the Radio Manufacturers Association [1]. JEDEC is the global leader in developing open standards for the microelectronics industry, with more than 3,000 volunteers representing nearly 300 member companies. JEDEC brings manufacturers and suppliers together to participate in over 100 committees, subcommittees and task groups, with the mission to create standards to meet the diverse technical and developmental needs of the industry. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world [2]. JEDEC documents are available for download from its website.

JEDEC is an independent incorporated Association governed by a Board of Directors (BoD), which is comprised of individual Directors representing JEDEC member companies. The JEDEC BoD is responsible for establishing appropriate committees to address guidelines and standards. The two types of committees are (1) service committees and (2) product committees. Service committees address a specific subject that may impact a range of product types; for example, package outlines, terms and definitions, government standards, and international standards. Service committees establish liaison with other JEDEC committees and with agencies outside JEDEC. For service committees, the first digit of the two-digit committee designator is the number 1. Product committees address a specific type of product. Examples include test methods, device specification format and minimum content, pinouts, interface requirements, and applications. Product committees establish liaison with other JEDEC committees and with agencies outside JEDEC. For product committees, the first digit of the two-digit committee designator is the number 2 or higher [3].

There are currently 11 active JEDEC committees, as shown on the JEDEC web site: 5 service committees and 6 product committees. The scopes of the committees are described in JEDEC document JM18, "JEDEC Committee Scope Manual." Some previous committees and subcommittees have been rolled up into others, and some have been made inactive. The scopes of some of the various current active committees can sound very different: for example, compare JC-11, "Mechanical Standardization" and

JC-15, "Thermal Characterization Techniques for Semiconductor Packages." This is partly because the various committees arose to meet the specific needs of people and entities who fueled them with their time and energy.

JEDEC started creating standards long before the CS industry even existed. Even since the advent of the CS industry, many of the standards were primarily driven by the silicon community simply because it was larger and the technology was more mature. Of course, this did not preclude the CS community from employing the silicon-based JEDEC standards; many of them are heavily used, for example, JESD47, "Stress-Test-Driven Qualification of Integrated Circuits." However, CS devices have special properties that may require some of the standards to be modified or to have entirely new standards created.

GaAs for Power Amplifier Modules

The need for guidelines and standards for the GaAs community evolved out of the GaAs Reliability Advisory Council and its establishment of the GaAs Reliability Workshop in 1985, over 30 years ago. That council dissolved and reformed as JC-50, "Gallium Arsenide Compound Semiconductors." JC-50 went inactive in 1994 when it transformed into the currently active JC-14.7 "Gallium Arsenide Reliability and Quality Standards" sub-committee, under the general JEDEC semiconductor committee JC-14 "Quality and Reliability of Solid State Devices and Associated Microelectronic Products" [4]. Ten years later, in an effort to reflect the expansion of the GaAs industry to include many more semiconductor material systems, the GaAs Reliability Workshop changed its name to the Reliability of Compound Semiconductors (ROCS) Workshop. It is interesting to note that originally, GaAs was addressed by its own product committee, and evolved into being addressed by a service subcommittee for reliability and quality. The scope of the original JC-50 committee, as archived in JM18, included FETs and IMPATT diodes, as well as analog and digital ICs, both microwave and high speed, as well as LEDs, lasers, and optical sensors. In comparison, the scope of JC-14.7 mainly deals with FETs, MMICs, and power amplifiers.

JC-14.7 is currently responsible for the following documents:

- JEP118 "Guidelines for GaAs MMIC and FET Life Testing" (1993)
- JESD226 "RF Biased Life Test" (2013)
- JESD237 "Reliability Qualification of Power Amplifier Modules" (2014)
- JEP110 "Guidelines for the Measurement of Thermal Resistance of GaAs FETs" (1988)

JESD226 and JESD237, created within the last 6 years, JEDEC "standards" (JESD), which are essentially prescriptive documents that call out specific tests, methods, and sampling plans to qualify products. This is in comparison to JEDEC "guidelines," or more accurately, "publications" (JEP), which read like white papers or literature reviews of failure mechanisms and possible reliability test methodologies and analyses that could be employed, rather than prescriptive qualification tests. The documents address the Power Amplifier Module (PAM), which, as the document states, has the unique aspect of possessing compound semiconductors. The scope states amplification as the core function, while acknowledging that the PAM may be used for other functions such as switching, power control and filtering. The document does not specifically call out GaAs as the CS content in the PAM, although it does refer the reader to JEP118, "Guidelines for GaAs MMIC and FET Life Testing."

JESD237 is essentially the PAM version of JESD47, namely, how to qualify a device. Much of the content of JESD47 is essentially re-used, but with some modifications and updates. Notably, the device requirement of the HTOL is replaced by "Life Test," with RF biased life (RFBL) being preferred, and HTOL, HTSL, and ELFR shown as alternates. RFBL is, of course, more appropriate for CS than a DC HTOL test, because it better represents how the module is actually used in typical applications. JESD226 then details the RFBL test methodology for RF CW, pulsed or modulated bias. This is intended to supersede the stalwart high temperature operating life (HTOL) test, which is one of the bias modes in standard JESD22-A108 "Temperature, Bias and Operating Life" and one of the most well-known tests in the qualification test suite called out in JESD47.

Also, interestingly, the humidity-related testing, "Humidity (Pick One)" (THB, HAST, UHAST, or AC) replaces the humidity section of JESD47. While JESD47 also says that one can pick THB or HAST, JESD47 declares that HAST should be run for 96 hours, while JESD237 declares the HAST requirement as "equivalent to 1000 hrs THB." This seemingly subtle difference makes all the difference for CS: the "equivalence" of THB-1000hrs and HAST-96hrs in JESD47 actually has its roots in humidity-related testing of microelectronics with aluminum back-end metallization. Those results showed that the failure mechanism is aluminum corrosion, which has an activation energy of approximately 0.7 eV, which is what leads to the approximate "equivalence" of THB-1000hrs and HAST-96hrs. But CS technologies often use gold metallization! In addition, the metallization layout, electric fields, chip passivation, devices design, and many other factors, can be very different, even within the CS realm. This, of course, can lead to different activation energy values for CS [5]. Therefore, JESD237 states that if one wants to use HAST, that the duration should be chosen to be equivalent to THB-1000hrs based on the empirically-determined activation energy. This gives the CS the freedom they need to accurately characterize the technologies of interest.

Wide Bandgap Power Electronic Conversion Semiconductors

The CS market for power electronic conversion is growing rapidly and is projected to continue and then some. Gallium

nitride (GaN) and silicon carbide (SiC) are the currently the most prominently used CS technologies for this application (heretofore referred to as "GaN for Power" and "SiC for Power"). One of the first well defined call for standards was manifest at the APEC 2017 Industry Session [6]. Eventually, the GaN Standards for Power Electronic Conversion Devices Working Group (GaNSPEC DWG) was born, with impetus from many entities including companies such as TI and Infineon, and with sponsorship by PowerAmerica, JEDEC, the IEEE Power Electronics Society (PELS), PSMA and the IEEE Electron Device Society (EDS). After significant progress, further discussions were conducted with JEDEC and it was eventually decided that the efforts of GaNSPEC DWG would be transitioned into the newly formed JEDEC product committee: JC-70, "Wide Bandgap Power Electronic Conversion Semiconductors."

The JC-70 scope covers power conversion discrete devices and integrated circuits fabricated from both wide bandgap and ultra-wide bandgap semiconductors. It explicitly states that RF/microwave amplification and signal conditioning applications are generally not covered. Two subcommittees have been formed so far: JC-70.1 is for GaN and JC-70.2 is for SiC. Each subcommittee has been structured with three task groups: TG 1 covers reliability and qualification procedures, TG 2 covers datasheet elements and parameters, and TG 3 covers test and characterization methods. The task groups have been tasked with developing guidelines first, to be followed by prescriptive standards.

One example of a CS-specific aspect that is being addressed by subcommittee JC-70.1, that is not being addressed by any other committee, is charge trapping in GaN. Charge trapping in GaN can manifest as a dynamic on-resistance (RDS(ON)) increase, which could lead to unstable increase in conduction losses that might result in failure [7]. Covering this aspect self-evidently involves collaboration between the three task groups: The Test and Characterization TG needs to define the details of how to measure dynamic RDS(ON) consistently and appropriately, the Datasheet TG needs to specify how to account for the transient behavior of RDS(ON), and the Reliability TG needs to specify the reliability and qualification test method to ensure reliability in typical fielded applications. In January 2019, the JEDEC Board of Directors approved by acclimation the first publication of JC-70, "Dynamic On-Resistance Test Method Guidelines For GaN HEMT Based Power Conversion Devices" (JEP173), sponsored by the JC-70.1 GaN Power Electronic Conversion Semiconductor Standards Subcommittee. Other GaN-specific mechanisms are being addressed, including charge injection, hot electron, and time-dependent breakdown (of the GaN itself, similar to TDDB), and according JEDEC documents are currently in development.

Subcommittee JC-70.2 is addressing SiC-specific mechanisms of concern. For example, basal plane dislocations (BPDs) can become nucleated and grow by operating a SiC MOSFET in third quadrant mode (negative drain voltage and current). This BPD accumulation can lead to an increase in the magnitude of the body diode forward voltage, which can lead to increased power dissipation and possibly reduced lifetime in fielded applications. In addition, the threshold voltage (VTH) of SiC MOSFETs can drift over time, as a function of gate bias voltage and temperature, due to the charge trapping interface and near-surface trap states in SiC-based oxide gates. This VTH stability of SiC MOSFETs is also being addressed by JC-70.2, as are some other SiC-specific physical mechanisms.

TODAY'S NEEDS

The need for guidelines and standards for GaN for RF and microwave applications is one of the most critical unmet needs of the CS community. A wide variety of GaN suppliers and researchers from government laboratory and academia have reported numerous failure mechanisms including the inverse piezo-electric effect GaN cracking, which is accelerated by voltage and temperature [8], ohmic contact degradation, which is accelerated by temperature and DC current [9], source-connected second field plate void coalescence, which is accelerated by temperature and RF stress [10], hot electron degradation accelerated by drain bias and operation in the "semi-on" condition [11] and others. These various effects can be seen on the devices of some OEMs and not others and, can display widely varying activation energies and intrinsic lifetime predictions [12], and can depend strongly on the electrical bias applied, including DC versus RF stress, and perhaps even the RF amplification mode (for example, Class A, Class AB, etc.). The time is ripe for the construction of guidelines and standards for this complex reliability story.

The need for guidelines and standards for optoelectronic devices may benefit from more development. The recent enormous surge in the VCSEL market that plays such a prominent role in the iPhone X may bring even more attention to the need for standards. It is interesting to note that there already was a JEDEC committee JC-23 on Optoelectronic devices, but that committee is listed as inactive in the current revision of JEDEC manual JM18S. Likewise, the inactive JC-50 on GaAs CSs was to have covered LEDs and lasers. However, JEDEC would be delighted to reactivate these committees or forms new ones if industry needs and interest merit it.

CONCLUSIONS

While great strides have been made towards developing guidelines and standards for compound semiconductors, much more work needs to be done. The silicon and GaAs community have already benefitted tremendously from the activities of JEDEC. The rapid development of new CS technologies and applications only amplifies, to use a pun, the need for guidelines and standards. JEDEC member

companies are strongly encouraged to empower bright and motivated people to work collaboratively on this effort that will benefit OEMs and customers. Input is needed both from the supplier and end-user sides. Developing these documents can be informative, enlightening and rewarding for the people who work on them and the entities they serve.

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ACRONYMS

CS: Compound Semiconductor
ROCS: Reliability of Compound Semiconductors Workshop
JESD: JEDEC Standard Document
JEP: JEDEC Publication
RFBL: Radio frequency biased life
PAM: Power Amplifier Module