GaN High-Performance Low-Leakage *p*-Islet MPS Diodes Enabled by PAMBE-Based Selective Area Growth

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Abstract

Two most widely used techniques to fabricate GaN *p-n* structures are: ion-implantation and ICP-RIE etching followed by regrowth. However, both the techniques inextricably suffer from higher leakage current due to defects and leakage paths created, while the latter introduces reduction in current density in the damaged areas. These high-defect yielding techniques can be avoided by using our PAMBE-SAG protocol developed earlier. In this paper we designed and successfully demonstrated the PI-MPS diode structures using the PAMBE-SAG methodology for the first time.

INTRODUCTION

Of late GaN has generated a lot of enthusiasm in the scientific community for high-power applications because of its wider bandgap and higher critical electric field than widely used semiconductors like Si and SiC. Although the incipient GaN devices like HEMT were lateral and heteroepitaxial in nature, because of well-known issues like current collapse, dynamic on-resistance, inability to support avalanche breakdown [1], and CTE mismatch due to heteroepitaxy, the focus shifted from lateral GaN devices GVPDs on bulk GaN substrate. In addition, GVPDs have advantages like higher current density, increased miniaturization possibility, and enhanced reverse blocking voltages.

Two key techniques in fabricating buried *p-n* structures for the GVPDs and ET structures are: (i) ion-implantation, and (ii) *p*- or *n*-layer growth followed by ICP-RIE and regrowth. Mg, the widely used *p*-dopant in GaN, being a deep dopant (activation energy, E_A: 160~240meV), has a very low activation rate, typically only around ~ 1% [2]. Ion-implantation has its inevitable shortcoming of lattice damage. Post-implant SMRTA procedure, reported recently [3], repairs some of the damages, but the lattice damage is obviously not completely healed. In the latter technique, the plasma etching damage due to ICP-RIE is unavoidable. The lattice damages invariably give rise to leakage sites along the *p-n* interfaces and sidewalls. These leakages are detrimental to the device on three counts, namely, (a) reduction in reverse blocking voltage (V_{br}), (b) reduction in current density as the damaged area contributes lesser current, and (c) more importantly, the impact on device lifetime and reliability. Therefore, it is important that a method that allows us to avoid these defects created by ion-implantation or etching be used for GVPD fabrication.

Our group, in the past, developed the PAMBE-based SAG protocol that completely circumvents the requirement for ion-implantation and ICP-RIE etching and causes almost no damage to the lattice [4-8]. It enables the formation of trenches (and, therefore, buried *p-n* structures or islet-like *p*- or *n*-structures) with a smooth surface, non-alloyed ohmic contacts with low resistance, and controlled regrowth of stable *n*- and *p*-doping, all of which are essential to processing of GVPDs. A very recent demonstration of our PAMBE-based SAG capability is illustrated in **Fig. 1**.

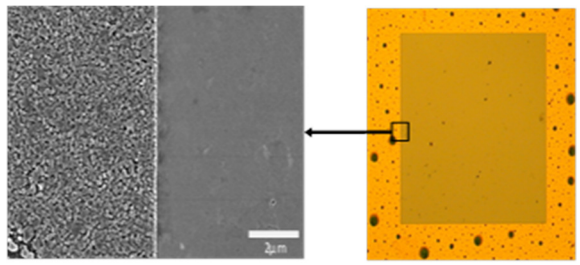

Fig. 1. A demonstration of clear distinction between regrown crystalline region using PAMBE-based SAG and masked region.

Our sister paper will discuss further on the very fine surface morphology of the PAMBE-based SAG growth already achieved en route to PI-MPS diode, corroborated by experimental results. A key device, successfully demonstrating GVPD fabrication using our PAMBE-SAG protocol is the PI-MPS diode, which is a marriage between the SBD and the *p-i-n* diode. It has the advantage of boosting the surge current capability because of lower on-resistance [9], higher switching speed and lower switching losses due to lower reverse recovery (RR) transients than the SBD, and a turn-on voltage lower than that of the *p-i-n* diode but similar to that of the SBD. The most recently reported GaN PI-MPS diode [9] used *p*-layer growth followed by ICP-RIE and regrowth and explicitly mentions the etching damage associated with it resulting in lower current density than expected due to the reason alluded to earlier. A combination of thick drift layer

(t_{dr} = 18μm), low-doped drift (N_{dr} = 8×10^{15}cm^{-3}), and ICP-RIE mesa isolation were used to achieve V_{br} ≈ 2kV. For comparison, a leakage current > 10A/cm^2 was observed at V_{br}, in contrast to a recently reported SiC MPS diode with a leakage current 2mA/cm^2 at V_{br} > 10kV [10]. This underscores the space for improvement of GaN PI-MPS as a nascent power device compared to its more mature counterpart, the SiC MPS diode.

DESIGN OF THE PAMBE-SAG ENABLED PI-MPS DIODE

To ensure a high-current capacity, in our fabricated device, we limit t_{dr} to only 10μm with an UID structure (UID: N_{dr} ≈ 2×10^{16}cm^{-3}). Unless carefully designed, snapback is very common in MPS diodes and this phenomenon is a serious issue for paralleling [10]. In our masks, the SBD section length, L_N = 2μm. The simulated forward I-V plots using a commercial simulation tool for various values of *p-i-n* section (*p*-base) length, L_P in an MPS unit cell are shown in Fig. 2.

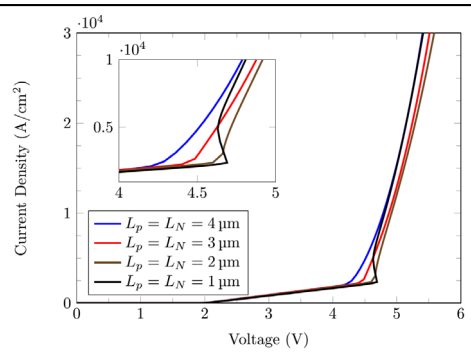

Fig. 2. The simulated PI-MPS unit cell forward I-V characteristics (snapback in inset).

Clearly, L_P ≥ 4μm results in no snapback. Thus, for the PI-MPS *p-n* grid, L_P ≥ 4μm is desirable. The vertical PI-MPS diode half-structure schematic appears in Fig. 3.

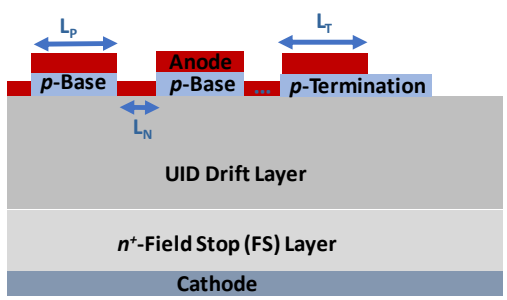

Fig. 3. The MPS diode half-structure for simulation.

The diode core length is given by L_{Core} = 2·L_T+m_P·L_P+(m_P+1) ·L_N. Here, m_P is the number of *p*-bases. The *p*-ExT length, L_T = 4~14μm results in L_{Core} = 250~260μm. We use L_{Core} = 250μm. This is done for the sake of uniformity across various devices with different L_P values.

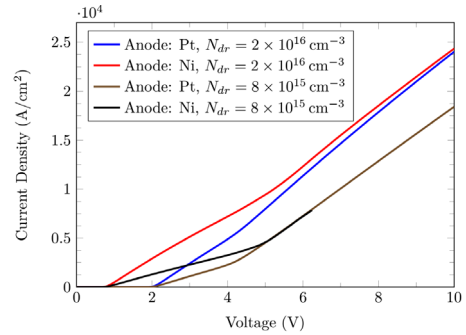

Fig. 4. The PI-MPS diode forward I-V characteristics. L_{Core} = 250μm.

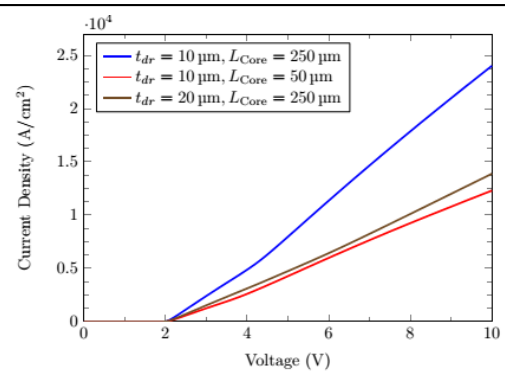

Fig. 5. The impact of L_{Core} and t_{dr} on PI-MPS diode forward I-V characteristics simulated for L_P = 8μm, L_N = 2μm, and L_T = 4μm.

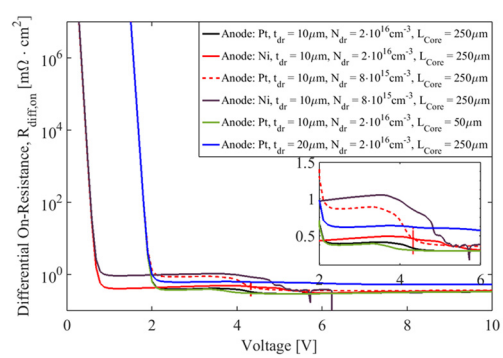

Fig. 6. The simulated differential on-resistance of the PI-MPS diode as a function of anode metal, N_{dr}, L_{Core}, and t_{dr}.

The forward I-V results for L_P = 8μm (N_{dr} = 8×10^{15}cm^{-3}, 2×10^{16}cm^{-3}, anode: Pt, Ni) are plotted in Fig. 4. The impact of L_{Core} and t_{dr} on current capacity is illustrated in Fig. 5. Clearly, L_{Core} = 250μm (wide area) and t_{dr} = 10μm (thin drift layer) are preferable for the high-current operation of the MPS diode.

The differential on-resistance ($R_{diff,on}$) as a function of various parameters is shown in Fig. 6. Clearly, the SBD section of the PI-MPS diode turns on at ~ 0.8V (Ni) and ~ 2.0V (Pt) and the *p-i-n* section turns on around ~ 3.0V signifying transition from unipolar to bipolar conduction. An ultra-low N_{dr} results in a stronger transition, which translates to a lower leakage due to the suppression of Schottky action, but the current density is lower due to higher $R_{diff,on}$. However, it requires a compensation doping which can adversely impact mobility, especially because of low Mg activation apart from the requirement of precise control of compensation. The reverse I-V characteristics for $L_P = 8\mu m$ ($N_{dr} = 8\times10^{15}cm^{-3}$, $2\times10^{16}cm^{-3}$) are considered here. While FP with passivation was used, for simplicity of fabrication, mesa isolation (using PAMBE-based SAG, mesa isolation can be formed without etching) was not used.

The reverse I-V characteristics appear in Fig. 7. For comparison, an MPS diode with $N_{dr} = 8\times10^{15}cm^{-3}$ ($t_{dr} = 18\mu m$) but with a structure similar to ours (no mesa isolation and $L_T = 4\mu m$, compared to reported $L_T = 10\mu m$ with mesa isolation and a much smaller $L_P = 2\mu m$ in [9]) was simulated. This resulted in $V_{br} \approx 1.76kV$ with a conservative critical electric field estimation and in the absence of many of the features used in enhancing V_{br} [9]. Using more advanced ET structures enabled by PAMBE-SAG, V_{br} can be considerably increased. These structures will be reported elsewhere.

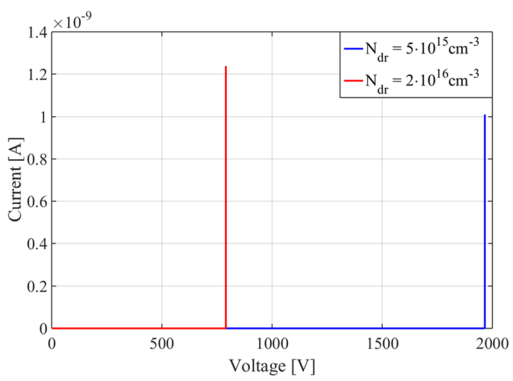

Fig. 7. The simulated PI-MPS diode reverse I-V characteristics.

EXPERIMENTAL RESULTS

To find the total Mg dopant concentration, SIMS analysis was performed. For the SIMS profile, the Mg effusion cell was opened and shuttered at regular intervals with Mg temperature (T_{Mg}) increased for each cycle. Also, the C-V measurement was performed to find the hole concentration. The Results are recorded in Table I. From these results, apparently optimal growth conditions achieve mid-$10^{18}cm^{-3}$ *p*-doping levels. Too high Mg-content results in defect compensation effectively reducing *p*-dopant concentration. The Ga effusion cell temperature (T_{Ga}) was 900°C while substrate temperature was 750°C with 0.75sccm nitrogen plasma at 350W power. There are no C-V data below 325°C because we are not concerned with this low doping.

TABLE I
ACTIVATION OF DOPANTS IN THE P-BASE LAYER

Mg Effusion Cell Temp. T_{Mg} (°C)	Mg Conc. From SIMS (cm^{-3})	Hole Conc. From C-V (cm^{-3})	Mg Activation Rate (%)
325	2.4×10^{19}	6.85×10^{17}	2.86
350	1.07×10^{20}	3.11×10^{18}	2.91
375	4.09×10^{20}	3.5×10^{18}	0.86

The SEM image of the PI-MPS diode islet structure using ICP-RIE etching is shown in Fig. 8. Here the dark wide slats represent the unetched section (*p-i-n* portion: *p*-islet) while the relatively medium-toned narrow slats represent the etched (SBD portion: trench).

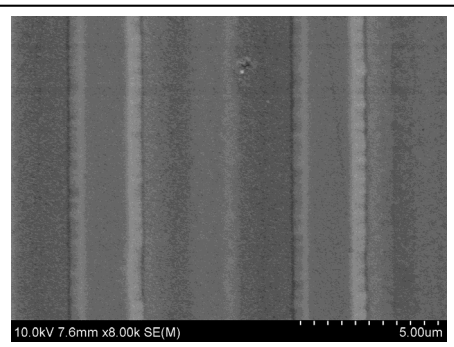

Fig. 8. The SEM image of the PI-MPS diode islet structure formed by ICP-RIE etching.

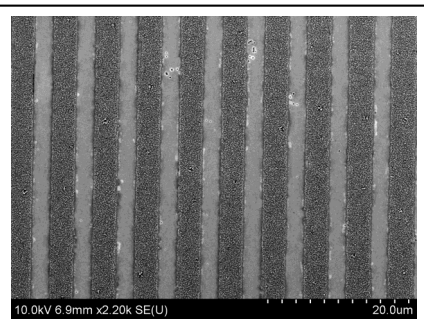

Fig. 9. The SEM image of the PI-MPS diode islet structure formed by the PAMBE-SAG protocol before stripping the SAG mask.

The SEM image of the PI-MPS diode islet structure using our PAMBE-SAG protocol before stripping the SAG mask is shown in Fig. 9. The smooth lighter toned slats represent the PAMBE-SAG regrown *p*-islets with crystalline GaN and the intermittent darker slats represent the polycrystalline GaN

that grows on top of the mask. This polycrystalline GaN layer is subsequently stripped easily along with the mask without the need for etching GaN surface. In Fig. 9, we notice that unlike the case when we resorted to etching, there is no plasma damaged region (the palest shade in Fig. 8) when we use PAMBE-SAG technique. The SEM images of the PI-MPS diode islet structure using our PAMBE-SAG protocol after stripping the SAG mask is shown in Figs. 10-11. Our work on PI-MPS diode is still in progress and we expect to get the electrical testing results for our samples soon.

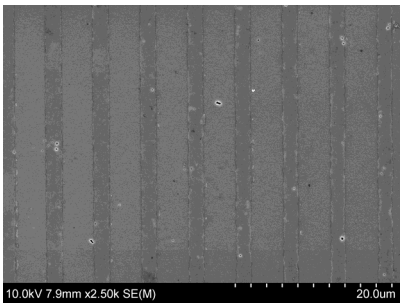

Fig. 10. The SEM image of the PI-MPS diode islet structure formed by the PAMBE-SAG protocol after stripping the SAG mask.

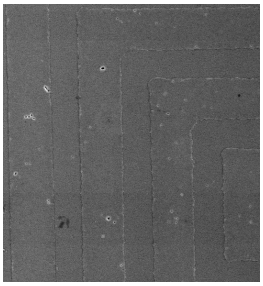

Fig. 11. The close-up SEM image of the PI-MPS diode islet structure formed by the PAMBE-SAG protocol after stripping the SAG mask. The bend is clearly visible.

Conclusions

Traditional ion-implantation and ICP-RIE etching followed by regrowth is problematic in fabricating GaN *p-n* devices as they unavoidably result in damage in the lattice sites. In contrast, our signature PAMBE-SAG methodology avoids the lattice damage and, thereby, eliminates the major leakage contribution and reduction in device current. We employed this methodology to fabricate the GaN PI-MPS diode that showcases the capability of the PAMBE-SAG in achieving high-performance *p-n* devices paving the way for more sophisticated GaN devices with more intricate geometries with reduced leakage yet higher current density.

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Acronyms

CTE: Coefficient of Thermal Expansion
C-V: Capacitance-Voltage
ET: Edge Termination
ExT: Extension Termination
FP: Field Plate
GVPD: GaN vertical Power Devices
HEMT: High Electron Mobility Transistor
ICP-RIE: Inductively-Coupled Plasma Reactive-Ion Etching
PAMBE: Plasma-Assisted Molecular-Beam Epitaxy
PI-MPS: *p*-Islet Merged *p-i-n* Schottky
SAG: Selective Area Growth
SEM: Scanning Electron Microscope
SBD: Schottky Barrier Diode
SIMS: Secondary Ion Mass Spectroscopy
SMRTA: Symmetric Multicycle Rapid Thermal Annealing
UID: UnIntentionally Doped