SiC Power MOSFET Manufacturing, Performance and Reliability for the Electric Vehicle Market

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Keywords: SiC MOSFET, Power MOSFET, UIS Ruggedness, FIT

Since the commercial introduction of SiC MOSFETs in the early 2010s, generational advances in device design and improvements in processing have driven the costs down to open many markets that currently rely on Si-based power switch technology. The growing electric vehicle (EV) market provides an enormous opportunity for the implementation of SiC power devices into a variety of EV systems, including on-board and off-board chargers, DC-DC converters, and drive train inverters. The challenge for SiC MOSFET manufacturers is to demonstrate the strict levels of reliability and ruggedness demanded for EV applications. In this paper, we present breakdown performance, ruggedness to unclamped inductive switching events and single event burnout failure in time (FIT) statistics of 1200V-rated SiC MOSFETs

INTRODUCTION

The electric vehicle (EV) market presents a huge opportunity to expand the total available market for SiC power devices. The performance advantages that SiC MOSFETs provide over Si switches that are currently employed in such EV systems as on-board and off-board chargers, DC-DC converters and drive train inverters will allow for faster and more efficient vehicle charging, significantly increased drive range and/or reduced cost of batteries and electric cooling systems. However, the reliability requirements demanded by the automotive markets are far more stringent than those needed from the industrial and energy markets that have fueled the market growth of SiC power MOSFETs. Since the first commercially available MOSFETs were released in the early 2010s, which were fabricated on 100mm SiC substrates, continual improvements in manufacturing methods, chip designs, substrate quality and substrate diameter have led to third generation devices now being manufactured on 150mm substrates.

DESIGN – ON-RESISTANCE AND BREAKDOWN VOLTAGE

Figure 1 shows the specific on-resistance ($R_{on,sp}$) vs. breakdown voltage (V_{BR}) Figure of Merit trade-off curves for unipolar devices, comparing the theoretical limits for both Si (long dashes on the left of the plot) and SiC (short dashes on the right of the plot) unipolar devices, derived from

$$R_{on,sp} = \frac{4V_{BR}^2}{\mu\varepsilon E_C^3},$$

where E_C is the critical breakdown field of the semiconductor, μ is the electron mobility and ε is the semiconductor dielectric constant. For any given V_{BR}, a SiC power device can be designed with more than two orders of magnitude lower $R_{on,sp}$, leading to far smaller chip sizes than comparably-rated Si devices. This is, of course, a simplified comparison between Si and SiC unipolar devices. In reality, the use of a bipolar structure, such as the insulated gate bipolar transistor (IGBT), allows one to design a part that is better (below or to the right of the limit lines) than the theoretical unipolar limits shown in the plot. Thus, the true comparison in the voltage classes of 600V to 1700V is between SiC unipolar devices and Si bipolar IGBTs. Nevertheless, SiC unipolar MOSFETs have better conduction performance at a given V_{BR} than Si IGBTs, especially at light loads, considering the knee voltage inherent to the Si IGBTs. These on-state benefits, combined with the superior switching performance of SiC MOSFETs, lead to a

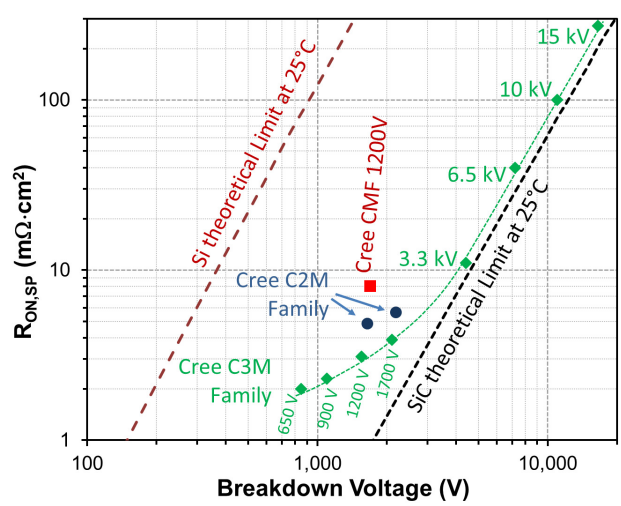

Fig. 1 – Specific on-resistance as a function of breakdown voltage at 25°C for various voltage-rated classes of Wolfspeed SiC MOSFETs.

substantial performance benefit of SiC MOSFETs and are what is driving the EV market excitement.

Also shown in Fig. 1 are data points for a variety of SiC MOSFETs manufactured by or in development at Wolfspeed, a Cree Company, including generational improvements shown for the 1200V- and 1700V-rated MOSFETs. In evolving from the first generation to the second and third generations, we have reduced specific on-resistance significantly while minimally impacting V_{BR}. For example, in the evolution of the 1200V SiC MOSFET from the first generation to the third, $R_{on,sp}$ has been reduced from 8.0 mΩ·cm^2 to 3.1 mΩ·cm^2, while the V_{BR} was reduced by only 175V, from 1700V down to 1525V. These large reductions in $R_{on,sp}$ have been achieved through optimal design of the MOSFET cell structure and the doping and thickness of the device's epitaxial structure. Through the large reduction in $R_{on,sp}$ with successive generations, chips that are designed for a certain resistance or power-handling capability can be designed much smaller, which leads to a reduction in the manufacturing price and price to the consumer.

Figure 1 shows that as design voltage decreases, starting at about 2.5 to 3kV, the achievable $R_{on,sp}$ begins to diverge from the theoretical limit. Figure 2 shows the schematic cross-section of a SiC MOSFET, highlighting the various resistive components through the device's conduction path. The substrate resistance, JFET resistance, channel resistance and source resistance are more or the less the same for all MOSFETs, regardless of V_{BR} design. The theoretical limit shown in Fig. 1 is calculated solely from the drift resistance, which is set by the design needs for blocking – which then defines the doping and epitaxy thickness required to achieve a given V_{BR}. Thus, for MOSFETs designed for high V_{BR}, above about 3 kV, $R_{on,sp}$ for real devices converges towards the theoretical limit, as shown in Fig. 1, because the resistance of the epitaxy dominates the design. Below about 3 kV, however, the other resistances in the MOSFETs become equitable to the drift resistance, resulting in the divergence of $R_{on,sp}$ from the theoretical limit line.

The design space for the SiC MOSFETs to be used in the EV industry extends from 600V to 1700V, depending on the specific application, and this is the design space at which the resistive components of a device become significant compared to the drift resistance. We must therefore take great care in designing the die and manufacturing to the limits and capabilities of today's manufacturing toolsets. This includes shrinking cell pitches as much as is feasible, considering the p-well and source implant depths required (and the associated lateral straggle) and the channel length required to ensure normally off performance. Because we are pushing the limits of the manufacturing toolsets and feature sizes, we must take great care to ensure the intrinsic ruggedness of the final design, considering process variability across all process steps in the manufacture of the devices. Various reliability and ruggedness tests have recently been performed on various MOSFET designs, and the remainder of this manuscript details some of these tests.

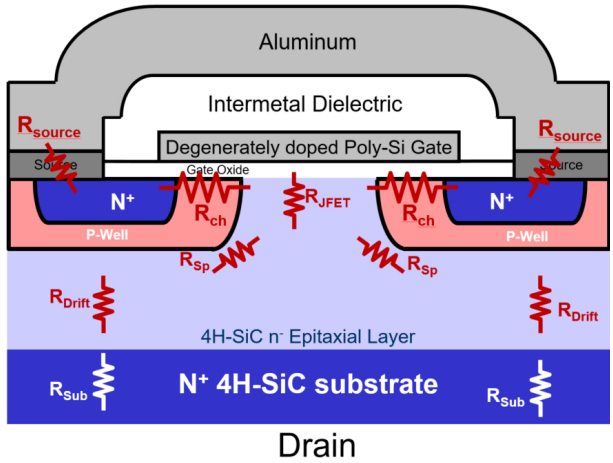

Fig. 2 – Schematic cross-section of a SiC MOSFET, showing various resistive elements through the conduction path.

Breakdown Voltage and Avalanche Ruggedness

Figure 3 shows V_{BR} as a function of temperature for a Gen 3 75 mΩ 1200V SiC MOSFET, comparing to a commercially available 1200V-rated Si IGBT. The SiC MOSFET has a far lower temperature coefficient than the Si IGBT, providing much more overhead for blocking to the full rating at over all temperatures of use. The difference in temperature coefficients derive from the fundamental material properties of SiC and Si.

Unclamped Inductive Switching (UIS) is a common operational mode that semiconductor switches must survive. We have subjected many Gen 3 1200V SiC MOSFETs to various UIS events in order fully characterize the single pulse UIS ruggedness capability. The circuit diagram for UIS testing is described in [1], and for these 1200V MOSFETs, the test was performed with V_{DD} = 50V and V_{GS} = 15V, and

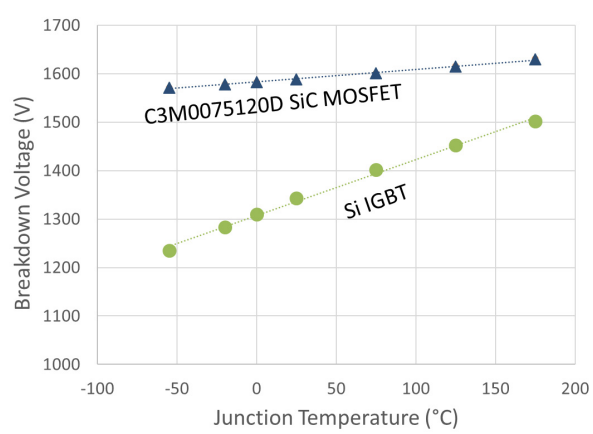

Fig. 3 – Breakdown voltage as a function of temperature for the C3M0075120D 1200V, 75mΩ Gen 3 SiC MOSFET and comparably rated 1200V Si IGBT.

with current in avalanche (I_{AV}) ranging from 5A to 120A. The MOSFETs are turned on with a series inductance that can be varied for each test to set the avalanche time (t_{AV}) and energy (E_{AS}). As the MOSFET turns on, the current ramps over time to the preset I_{AV} due to the series inductance. When the MOSFET reaches the set I_{AV}, the gate is turned off, the inductor current freewheels through the diode, and the MOSFET is forced into avalanche to maintain the inductor current. The MOSFET remains in avalanche until all energy stored in the inductor ($E = 0.5LI^2$) is fully dissipated in the MOSFET as E_{AS}. By stepping the inductance up with each successive test on a given device, we systematically step up the E_{AS} and can determine the E_{AS} at which the part fails.

Figure 4 shows a typical UIS waveform of current and drain bias for a Gen 3 75mΩ 1200V (C3M0075120D) MOSFET. The current level at trigger was 20A for this example and the MOSFET voltage at this condition reached 1600V. The part survived this condition, so the inductor was stepped up in successive tests until failure was observed. Figure 5 shows a plot of the typical **last surviving t_{AV}** for parts subjected to I_{AV} of 5A to 120A. Also plotted in Fig. 5 is the last surviving t_{AV} for the Gen 2 80mΩ 1200V (C2M0080120D) MOSFETs [2]. The two envelopes for the typical last surviving t_{AV} for both generations of MOSFETs are almost completely coincident. Because of the nature of the failure mechanism of power dissipation in a given unit area, avalanche ruggedness scales directly with active area of the device for a given device design. For Wolfspeed MOSFETs, the Gen 3 75mΩ device is 75% of the active area of the Gen 2 80mΩ device, yet the failure envelopes are identical. The energy of avalanche in a UIS test is proportional to avalanche voltage (V_{AV}), and since V_{AV} is lower for the Gen 3 device, the dissipated energy is lower. When normalized to active area, the energy density dissipated in the two differently-sized devices is approximately the same, and the same failure envelope is observed. Thus, there is no UIS ruggedness detriment by replacing a larger Gen 2 MOSFET with a smaller Gen 3 MOSFET of similar resistance rating.

Because of the empirical nature of the determination of the typical last surviving t_{AV} for UIS ruggedness, we apply an appropriate statistical margin of safety to get the UIS Safe Operating Area for the C3M0075120D shown by the dashed line in Fig. 4. We have demonstrated that this methodology of establishing the appropriate margin of safety allows us to fully demonstrate a qualification of C3M-family MOSFETs that have been subjected to UIS stresses that sit on the envelope of the SOA curve [1].

FIT Determination under High Blocking Bias

Failure in Time (FIT – Failures per Billion Device Hours) statistics for Gen 2 and Gen 3 MOSFETs were collected by examining the failure rate under high DC biases while subjecting the MOSFETs to a high flux density of high energy neutrons at the Los Alamos Neutron Science Center

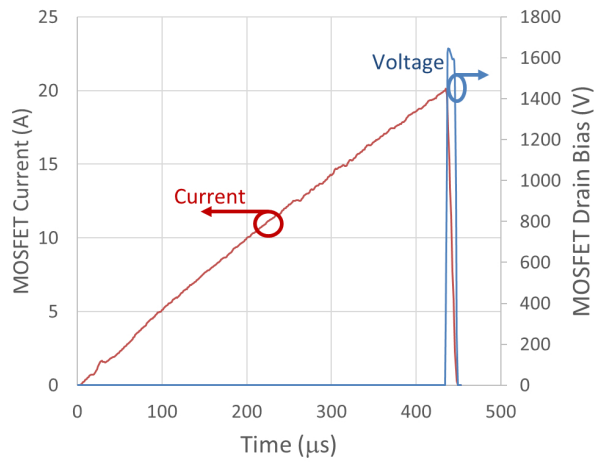

Fig. 4 – Waveforms from a UIS test with I_{AV} = 20A, L = 1.0mH, t_{AV} = 14µs, V_{AV} ~ 1600V and E_{AS} = 190mJ.

(LANSCE) [3]. Power devices have shown to be susceptible to single event burnout (SEB) that results from high energy neutrons that constantly bombard the Earth's surface [4-7]. The high energy neutron beam at LANSCE mimics the spectrum of terrestrial neutrons at a flux level of up to a billion times that at the Earth's surface. Therefore, by conducting investigations at the LANSCE beamline, failure rates of power devices under SEB conditions can be accelerated by up to a billion times and proper FIT statistics can be obtained.

Figure 6 shows the FIT rate as a function of applied drain bias for various voltage classes of Wolfspeed MOSFETs. The points represent the mean values of FIT normalized to the unit area of the chips obtained for each group of devices tested at the given drain bias, so that the FIT/cm^2 values line up for various device sizes in a given voltage family. The lines represent a model fit following the approach of [7]. As expected, devices with a higher voltage rating have a lower failure rate at a given drain bias. To better compare devices

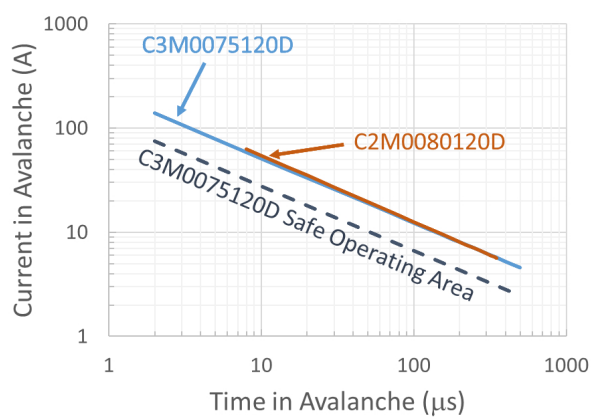

Fig. 5 – Current in avalanche (I_{AV}) as a function of the time in avalanche (t_{AV}), showing the typical failure envelope of Gen 2 (C2M) and Gen 3 (C3M) devices (solid curves) along with the statistically determined UIS Safe Operating Curve for C3M0075120D.

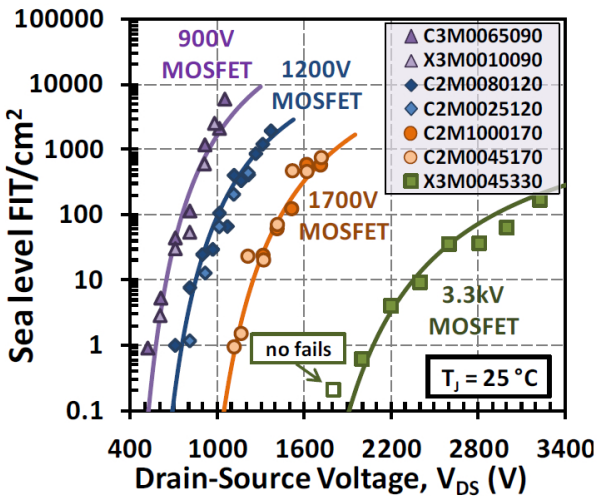

Fig. 6 – MOSFET SEB failures in time (FIT), scaled by active area [3].

with different blocking ratings, we have normalized the data by the avalanche voltage (V_{DS}/V_{AVAL}) and replotted the data in Fig. 7. For all devices tested, within the bounds of the noise of the statistical processes occurring, there is roughly a universal scaling of the devices.

Figure 8 compares the FIT rate of 25 mΩ 1200V Gen 2 MOSFETs, rated to 60A continuous at a case temperature of 100°C, to a 60A-rated 1200V Si IGBT. To provide the most direct comparison in a real application, we have normalized the FIT by the current rating, since the Si IGBT has a much larger area than the 25 mΩ SiC MOSFET. As applied drain (or collector) bias increases much above about 850V, the FIT/Amp of the SiC MOSFET becomes much better than that of the Si IGBT, having an order of magnitude lower failure rate as the applied bias approaches the device rating. Thus,

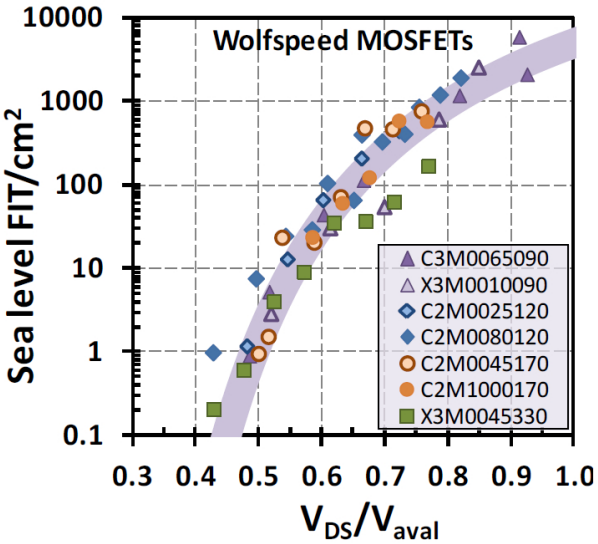

Fig. 7 – MOSFET SEB failures in time (FIT), scaled by active area and normalized by the avalanche voltage of each voltage class of device [3].

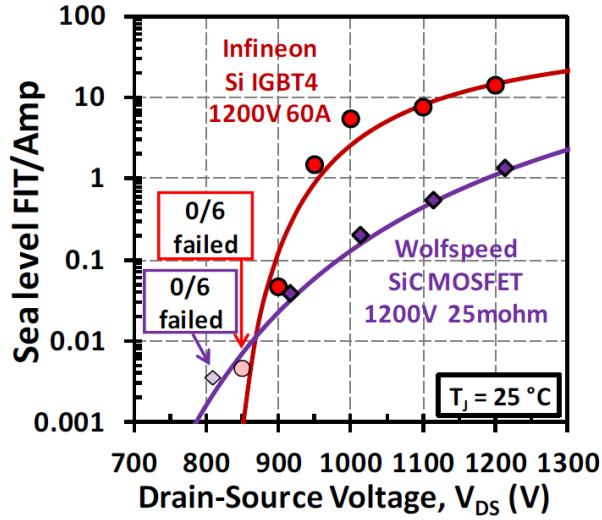

Fig. 8 – Comparison of FIT rates for comparably rated 60A Si IGBTs and SiC MOSFETs [3].

the SiC MOSFET is much less susceptible to SEB failures in systems where high voltage overshoots from the nominal bus voltage occur.

Conclusions

SiC MOSFETs are rapidly becoming cost beneficial for EV applications due to continuous improvements in design and manufacturing. In order to be adopted into EV applications, SiC MOSFET manufacturers must demonstrate the reliability and ruggedness required by the automotive industry. We have demonstrated aspects of reliability, including blocking capability, ruggedness to UIS events and the superior FIT performance of SiC MOSFETs compared to Si IGBTs.

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