CMP Process Development on III-V Substrates for 3D Heterogeneous Integration

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Abstract

Integrating compound semiconductors with silicon CMOS has been critical for the success of the commercial wireless communications industry, especially at macroscopic integration nodes (board-level, MCM, etc). With continued scaling of system bandwidth and power requirements, RF and mixed-signal microsystems can benefit from 2.5D and 3D heterogeneous integration techniques with finer size and pitch interconnects. Chemical-mechanical-polishing (CMP) becomes a critical tool for these interconnects. We outline our findings during development of CMP processes on compound semiconductor substrates (InP and SiC) substrates, and present measurement results from integrated parts. Developments include: CMP polishing of SiO and metals (Cu and W); and controlled wafer thinning of bonded InP and Si wafers to <10 µm final thickness.

INTRODUCTION

II-V integration with Si CMOS technologies has been a key enabler of analog and mixed-signal circuit technologies [1]. As the Si CMOS industry drives toward 2.5D and 3D integration solutions, compound semiconductor technologies will require solutions for fine-pitch heterogeneous integration. Our work to utilize Direct Bond Interconnect ® [2] for 3D wafer stacking required chemical-mechanical-polishing (CMP) development on compound semiconductor wafers [3]. We will outline our process development on indium phosphide (InP), and silicon carbide (SiC) substrates and show finished device integration results from the process.

PROCESS DEVELOPMENT AND RESULTS

Chemical-mechanical-polishing (CMP) is used extensively in semiconductor substrate manufacturing and CMOS device fabrication [4]. Back-end-of-line (BEOL) wiring environment processing of integrated circuits leaves wafers with non-planarities, affecting photolithography and maintaining consistent controlled impedance transmission lines. The Si CMOS industry embraced CMP to tackle this problem, whereas III-V foundries have typically implemented spin-on-dielectrics with planarizing properties, such as polyimide and benzocyclobutene (BCB).

Fig. 1 shows a schematic cross-section of the 4-level BCB-based interconnect process used for Teledyne's InP HBT process. Thin-film transmission lines in the technology can be accurately modeled and have been demonstrated in the technology for circuit demonstrations at frequencies up to 700 GHz. Compared to silicon back-end-of-line processes that utilize extensive CMP processes, the BCB-based process offers a relatively simple process flow with a low cost of ownership.

3D heterogeneous integration using wafer stacking and the DBI process requires highly planar substrates, ultra-smooth oxide surfaces, and the ability to CMP interconnect metals. To maintain benefits of our existing BCB based BEOL process, a copper (Cu) damascene process was developed on-top of the interconnect stack. Major challenges in this development included: inter-level dielectric peeling, wiring interconnect peeling, wafer edge dielectric delamination, and InP scratching, which can lead to wafer breakage. Fig. 2 shows an example of interconnect delamination near the edge of an InP wafer after SiO2 CMP.

Solutions to these challenges included lowering the CMP

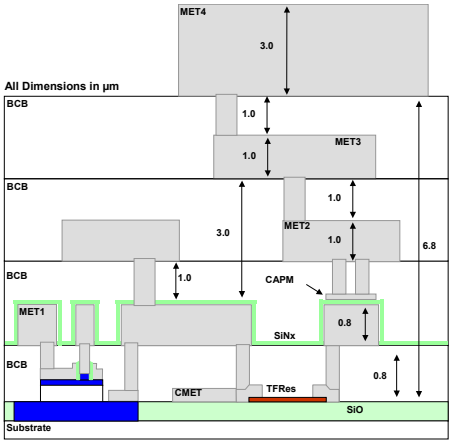

Fig. 1 Schematic cross-section of Teledyne's 4-level BCB-based interconnect stack.

downforce during oxide polishing, changing wiring

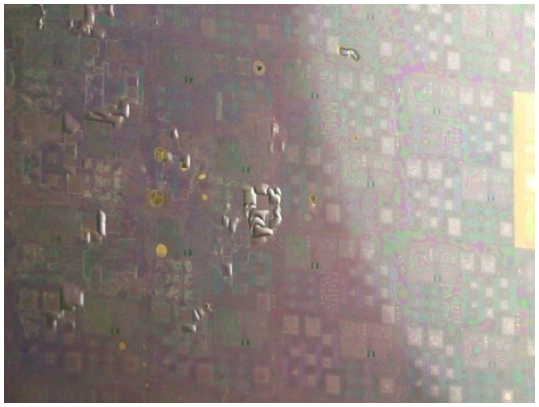

Fig. 2 Image showing local interconnect delamination on InP substrate with poorly optimized SiO_2 CMP process.

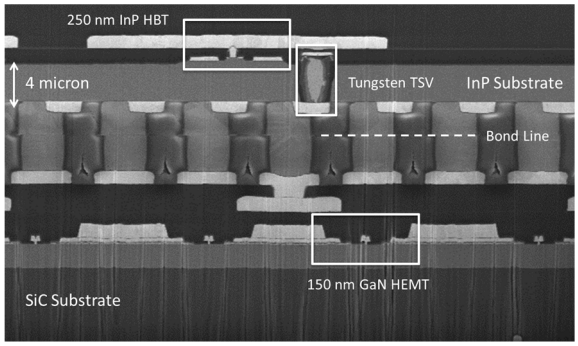

Fig. 4 Cross-section of 3D integration of InP HBT and GaN HEMT using DBI process with tungsten TSVs in InP layers.

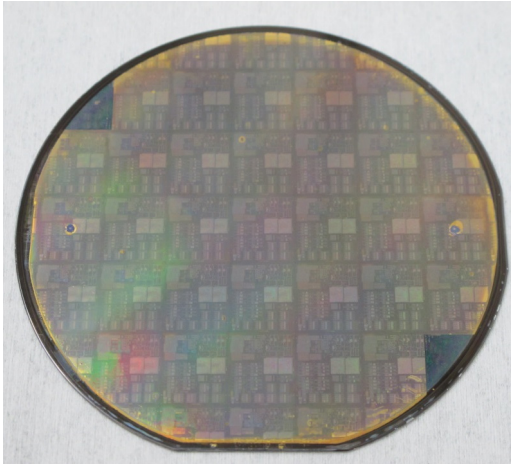

Fig. 3 InP HBT wafers after SiO CMP polish on-top of BCB-based interconnect stack using optimized process.

interconnect density rules, improving the BEOL wiring stack adhesion to the substrate, managing BEOL wiring stack material accumulated stresses, and keeping the wafer edge as uniform as possible. In order to planarize SiO2 for wafer bonding, given the lack of planarity in the lower Au/BCB levels, multiple sequences of SiO2 depositions and polishes may be required. Fig. 3 shows an example of an InP wafer after SiO2 CMP using the optimized processes. With these processes 3D DBI integration of InP to Si CMOS was successfully demonstrated with good heterogeneous interconnect yield and no degradation in the performance of native substrate devices [3].

In addition to InP-to-CMOS integration, InP HBTs have been integrated with GaN HEMT devices on SiC substrates through 3D integration. To maintain a thermal path from the HBTs to the SiC substrate, a two-transfer process was implemented that keeps the HBTs face-up and allows heat transfer through a thinned InP substrate. This process required a via-first process prior to InP HBT fabrication. Tungsten (W) metal was used for the through-substrate via (TSV) and W CMP on InP substrates for TSVs utilized many of the same development heuristics from InP/SiO2. Given the relative fragility of the InP substrates, scratching during CMP becomes problematic. Alleviating scratching included minimizing large-area TSV features, and controlling wafer bow during CMP by optimizing tungsten metal deposition processing and thickness. Fig. 4 shows a cross-section of a completed InP wafer back-to-front bonded to GaN. The InP was thinned using grinding and CMP.

CONCLUSIONS

Development of CMP processes on compound semiconductor substrates may require modifications to the interconnect wiring BEOL. Applying these changes without sacrificing intrinsic device performance will not only enable fine-pitch heterogeneous integration, but also can enhance the baseline BEOL properties.

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