Modelling of Backside-induced ESD Defects in GaAs Front End Manufacturing

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Abstract

The semi-insulating characteristics of GaAs substrates makes GaAs front end manufacturing sensitive to ESD events occurring during wafer processing. Charges induced to the wafer by these ESD events can harm or even destroy insulating structures like MIM capacitors because these charges cannot dissipate. This paper deals with the modelling and control of backside-induced ESD defects on MIM capacitors. It will highlight how charges can be induced to the wafer from its backside by wet chemical processes and consequently destroy MIM capacitors at the wafer front side.

INTRODUCTION

In contrast to Silicon technologies, GaAs technologies utilize semi-insulating substrates to grow their epitaxial layers on. These semi-insulating substrates are used to avoid undesirable substrate leakage current and RF losses for passive devices and transmission lines.

According to ESD standard [1], resistances >1e11 Ω are considered to be insulating regarding their efficiency for charge dissipation. This means that, strictly speaking, semi-insulating substrates are not ESD compliant and bare the risk of charge accumulation because practically the limit for ESD risk is already at a resistance of 1e9 Ω.

ESD RISK OF WET CHEMICAL PROCESSES

Solvents and etchants are solutions, which contain a significant amount of ions. These ions guarantee a sufficiently low resistivity of the liquid to prevent charge accumulation and, thus, ESD events in the process.

De-ionized water (DI-water), however, is treated to yield a typical resistivity in the range of 20 MΩcm. During processes in which the wafer is exposed to DI water while spinning, DI water moves laterally from the wafer center to the edge. This movement together with the high resistivity of the liquid causes charge separation, as schematically depicted in fig. 1. This mechanism can result in electric fields up to 20kV/cm.

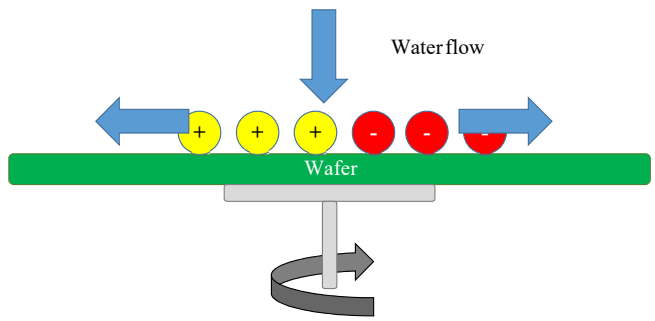

Fig. 1. Charge separation while DI water is applied to wafer under spinning.

IMPACT OF ESD EVENTS ON MIM CAPACITORS

Electrostatic discharge can cause sudden breakdown of MIM capacitors [2]. Defective MIM capacitors have been observed in this case by the final AOI inspection at the end of the wafer manufacturing. An optical image and the associated top-view SEM and FIB cross section of the observed defect is depicted in fig. 2

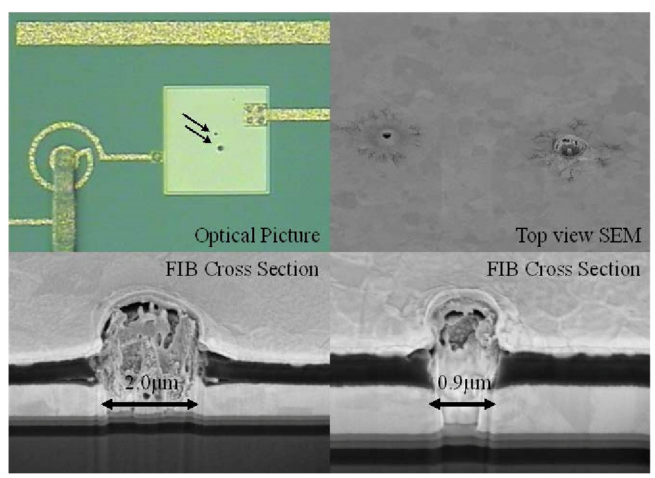

Fig. 2. Defect analysis of ESD defects observed on MIM capacitors

ESD Defect Generation

During backside processing of the wafer, there is a cleaning step exposing DI water to the wafer, which is then spun off to dry the wafer. As explained in the section before, this process induces charges to the wafers backside. The semi-insulating wafer acts as a capacitance, which leads to the generation of mirror charges at the opposite frontside of the wafer, where the MIM capacitors are located. According to following equation

$$C_{wafer} = \varepsilon \cdot \varepsilon_0 \cdot \frac{A_{wafer}}{d_{wafer}} = q_{process} \cdot V_{wafer}$$

the voltage drop across the wafer for a given induced charge is proportional to the capacitance of the wafer, whereas the capacitance of the wafer is determined by its thickness. A schematic of the described process is depicted in fig. 3.

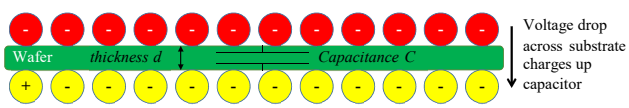

Fig. 3. Voltage drop induced by charges on the backside of the wafer

Because the wafer is thinned down to a thickness of 100 µm or thinner during the backside processing, the ESD sensitivity of the wafer increases significantly compared to the frontside processing.

To prove this model, three wafers have been grinded down to different thickness and the cleaning process has been applied to the wafers. After the process, the wafers have been inspected by AOI and pictures have been taken from each defect on each wafer with the result given in table I.

TABLE I
ESD Defect Rate of Each Wafer With Different Substrate Thickness

Thickness	ESD defects (total number of taken picture)	Defect Rate
100µm	9 (92)	9.8%
300µm	8 (100)	8.0%
625µm (not thinned)	2 (52)	3.8%

The defect maps for the 100µm and 625µm wafers are depicted in fig. 4 and 5 as an extreme case comparison. All the defects are randomly distributed without showing a specific center of defect accumulation, which is expected by such an effect since the complete wafer surface is equally exposed to the DI water.

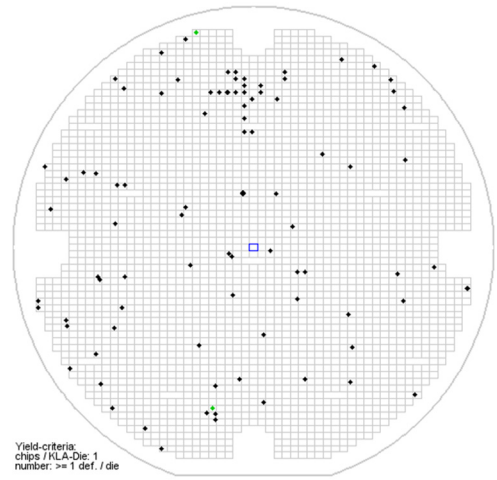

Fig. 4. Defect map of a 100µm thick wafer presenting all defects of the wafers surface incl. ESD defects.

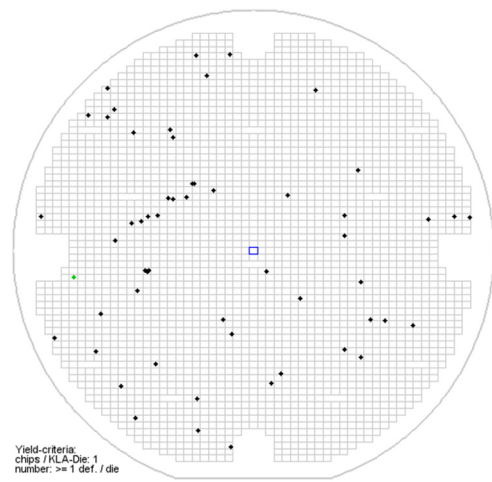

Fig. 5. Defect map of a 625µm thick wafer presenting all defects of the wafers surface incl. ESD defects.

The AOI maps present for the wafer with a thickness of 625µm presents in total less defects than for the wafer with 100µm thickness. This is because the thicker wafer suffers from less ESD defect than the thinner one whereas the density of the other defects induced by the normal processing remains nearly the same. This investigation proves the proposed model since the ESD sensitivity is reduced with higher wafer thickness.

Control of DI Water Resistivity to Avoid ESD Defects

In order to efficiently prevent the generation of ESD defects, it is necessary to guarantee sufficiently low resistivity of the DI water. The resistivity of the DI water defines the level of charge separation during spinning and therefore the risk for ESD events.

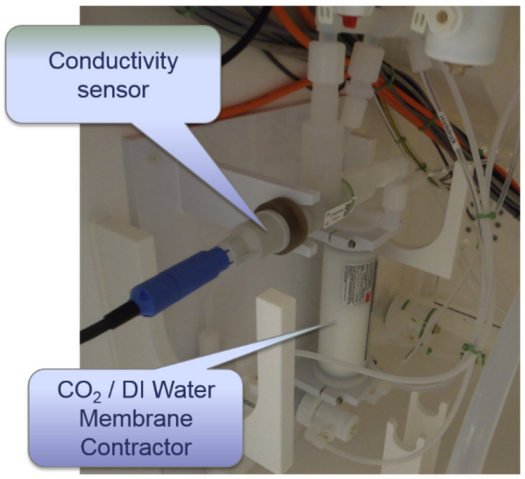

Fig. 6. Control of DI water conductivity by adding CO_2 and measuring the resulting conductivity.

Fig. 7. Automatic process stop due to violation of DI water conductivity limit of 1MΩcm.

The cleaning tool in our backside process has been equipped with a CO_2 membrane contractor in the DI water supply line. This solution has been purchased directly from the toll supplier as an of the shelf solution for ESD control. The CO_2 dissolves in the DI water and decreases the resistivity from the typical level for DI water of 18 MΩcm down to <1 MΩcm which is a typical value that can be achieved with this approach. A sensor measures the resistivity of the DI water with dissolved CO_2 before it enters the process chamber. The system is depicted in fig. 6.

The sensor measuring the conductivity of the DI water is directly linked to the PLC control of the tool. The sensor is controlled by the tool software (see fig. 7) and allows to continuously monitor the resistivity of the used DI water and to stop the tool automatically, when the resistivity rises above the limit. This measure solved the issue of ESD defect generation and since then more than 5000 wafers with in total more than 10 millions of chips have been processed and no defects have been detected anymore after the installation of the DI water resistivity control. Assuming an average amount of 20 MIM capacitors per chips, this means, that more than 200 millions of capacitors have been inspected without presenting ESD defects. An example is depicted in fig. 8.

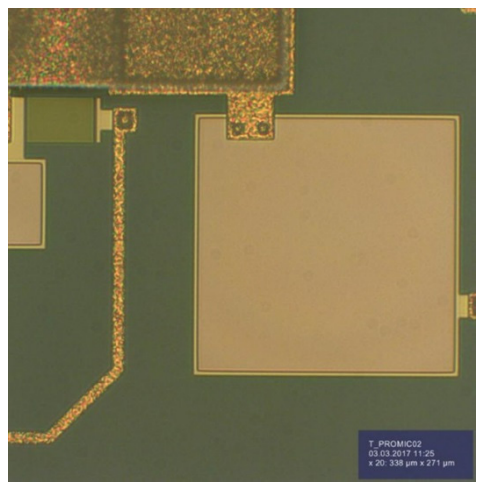

Fig. 8. Optical picture of an defect free MIM capacitor.

Conclusions

In this paper, we have shown how charge separation is caused by DI water treatment of wafers. Furthermore, we explained, how these induced charges cause ESD defects on MIM capacitors even on the opposite side of the wafer. It has become clear that the control of the resistivity of the DI water exposed to the wafer is a critical parameter to avoid high electric fields and, therefore, ESD defects to sensitive devices like MIM capacitors.

ACKNOWLEDGEMENTS

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REFERENCES

[1] ESD Standard, *Electrostatics - Part 5-1: Protection of electronic devices from electrostatic phenomena - General requirements*, IEC 61340-5-1:2016, May 2016.

[2] L. Luu-Henderson et al., *Mechanism and Resolution of Implant Induced ESD Damage in GaAs IC Processing,* 2018 CS MANTECH Technical Digest, pp. 57-60, May 2018.

ACRONYMS

GaAs: Gallium Arsenide
ESD: Electrostatic Discharge
MIM: Metal-Insulator-Metal
DI-water: De-Ionized Water
AOI: Automatic Optical Inspection
PLC: Programmable Logic Controller