AlGaN/GaN Power Devices in a Si World: From R&D to Manufacturing and Reliability

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Abstract

Converting a research project into a product and running AlGaN/GaN power device technology into a CMOS line poses several challenges. The hetero-epitaxy is an important part of the device and product, and as such requires tight process control. For e-mode device operation, the use of a p-GaN gate structure has a back-to-back diode in the gate, which poses reliability concerns. Future AlGaN/GaN wafer and process technology will transfer to 200mm, and first results are disclosed.

INTRODUCTION

The AlGaN/GaN materials system, with its unique combination of a high 2DEG density (high mobility, low on-resistance) and a wide band gap (high breakdown) is appealing for both rf and power applications [1]. Over the past years, the first power products entered the market. To be cost-competitive with Si Trench MOSFETs (<200V node) and super-junctions (650V node), manufacturability is focused on hetero-epitaxy (GaN-on-Si) and on the challenges of processing a III-V material system in CMOS Si process fabs.

For the GaN-on-Si hetero-epitaxy, reduction of the crystalline defects caused by the lattice mismatch and compensation of the stress is important. The newest generation of MOCVD reactors allow better process stability, within wafer uniformity and reproducibility.

As for the processing aspect, integration issues like cross-contamination, non-standard wafer thickness, wafer breakage and the use of a non-Au based metalisation are important.

From the device perspective, e-mode operation is desired for fail-safe operation. From the different e-mode device concepts (p-(Al)GaN gate [2], MISHEMT [3], Trigate [4], Tunnel FET [5] etc), only the p-GaN gate structure made it into commercial products. The back-to-back diode stack however imposes reliability challenges [6,7,8,9].

An outlook to the prospects and challenges for GaN-on-Si on 200mm will be given.

OPEN INNOVATION AND RESEARCH NETWORK

AlGaN/GaN HEMT power devices are a disruptive technology, and often the seeds are planted and incubated at research centers world-wide. Throughout the years, ON Semiconductor has established a long-lasting collaboration with selected Centers of Excellence on GaN power device development. Specifically, since 2012, ON Semiconductor is part of imec's affiliation program on 200mm GaN-on-Si, which allows us to perform early technology development (high risk), at a reasonable cost (either through funding, or through cost sharing). In 2013, the d-mode process technology was transferred in-house, to a 150mm production line. In 2017, the p-GaN technology was transferred.

PROCESSING III-V WAFERS IN A CMOS PROCESS LINE.

There are several challenges for processing an III-V material system in an automotive qualified CMOS process line.

- Cross-contamination: Ga and Al are life-time killers for Si devices. ON Semiconductor has developed a contamination control protocol, such that only a very limited number of tools are dedicated to GaN, and the majority of the tools are shared with the Si production line, resulting in very fast fab cycle times. Dedicated cleans and wafer boxes guarantee that no cross contamination occurs.
- Wafer breakage: special care has to be taken for all wafer handling, clamping and (de)-chucking of the wafers. Wafer breakage rate is <1%.
- Non-Au based metalisation: III-V process lines use Au and/or Ni as metals for Ohmic and gate contact. In a CMOS fab, these materials are not available and hence a good Ohmic contact is developed using a Ti/Al based metal stack. A low Rc of 0.2 Ω.mm with good reproducibility can be achieved, see Fig. 1.

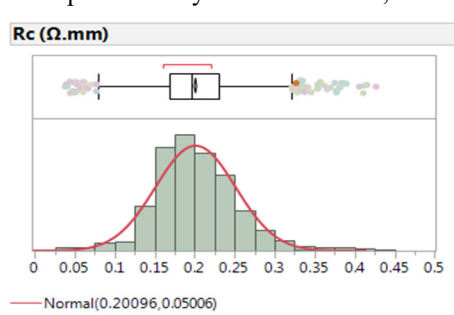

Fig. 1: Statistical data (histogram) on Ohmic contact resistance Rc, using a Ti/Al metal stack.

GAN-ON-SI HETERO-EPITAXY.

Hetero-epitaxy of III-nitrides by MOCVD is currently the most suitable method for industry-scale AlGaN/GaN HEMTs. Silicon has become most utilized substrate because of its excellent quality, low price and availability up to 300 mm. Utilization of a silicon substrate, however, requires growth of carefully optimized buffer structures in order to reduce problems caused by the mismatch between the crystal lattice constants and the thermal expansion coefficients of the substrate and the epitaxial layer. High crystalline quality, no structural defects and smooth interfaces are essential to obtain good device properties. The buffer structure is generally formed by an AlN nucleation layer, a system of stress-relief layers, the active hetero-structure and a passivation layer. The stress-relief layers are either formed by a series of step-graded AlGaN layers, or by a superlattice structure.

Selection of the best silicon substrate is needed to reduce the effects of the hetero-epitaxial growth. A heavily boron doped material has higher Young modulus compared to the lightly doped material and is less prone to formation of crystallographic and surface defects [10], see Fig. 2a.

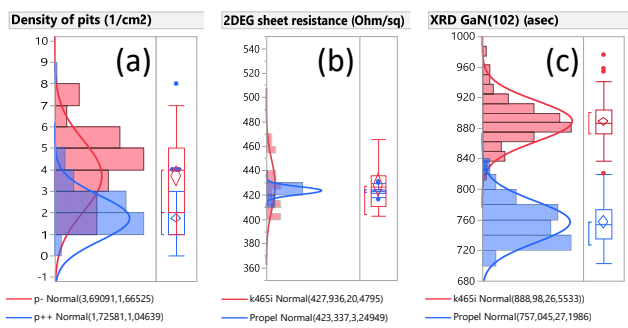

Fig. 2 : (a) Pit densities measured on GaN-on-Si wafers with p- (red) and p++ substrates (blue) ; (b) Rhosheet (Ω/sq) and (c) XRD, obtained on k465i (red) and Propel (blue).

GaN-on-Si growth for power devices is still relatively new to our industry and therefore there is still a lot of development on novel types of MOCVD reactors. ON Semiconductor has initiated its development on a Veeco TurboDisc k465i reactor, which is capable of processing five 150 mm wafer in one batch. The wafers are placed eccentrically on the carrier with rotation speed up to 1200 rpm. This causes formation of deep crystallographic defects due to the high centripetal forces. Moreover, the design with single heating element below the wafer area leads to non-uniform temperature field with negative effect on the thickness and composition uniformity of the AlGaN barrier layer. The newest generation of MOCVD reactors that were optimized for the GaN-on-Si growth, such as single wafer reactor Veeco Propel HVM, can mitigate the majority of the problems, as can be seen from Figs 2b and 2c. The single wafer construction ensures that there are no centripetal forces on the wafer and reduce the possibility of compromising the substrate quality. The construction with optimized gas injection system and heating assembly improves the thickness and composition uniformity of the grown layers.

An integral part of the GaN-on-Si MOCVD growth process are the in-situ and ex-situ metrology systems. The in-situ systems provide on-line information on the status of the growth. Besides the direct temperature control of the system, they are routinely utilized to evaluate the growth rate of the epitaxial layers, evolution of the stress, and also qualitative analysis of the thickness uniformity and surface roughness. The ex-situ systems such as measurement of the wafer shape, high resolution X-ray diffractometry, photoluminescence and optical surface analysis are used to assess the physical properties of the hetero-epitaxial layers.

E-MODE USING PGAN GATE ARCHITECTURE.

To achieve e-mode operation, the pGaN gated device architecture is implemented. Fig. 3 shows a schematic cross-section of the gate structure. Important is that the gate consists of a back-to-back diode stack, in which the top diode is a Schottky diode (TiN/Al gate metal to p–GaN), and the bottom diode is a p-i-n diode (pGaN to i-AlGaN to 2DEG). Some device trade-offs have to be considered.

- Vth versus Ron: a high hole concentration in the pGaN (high [Mg]) is desirable, since this will determine Vth. However, since the pGaN is grown over the complete wafer, the diffusion tail of the [Mg] in the AlGaN barrier will also increase, leading to high on-state resistance Ron. An AlGaN/pGaN regrowth is a solution, but adds cost and is hence not desired [9].
- Gate leakage versus gate control (Ohmic gate versus Schottky gate): the control of the transistor gate (p-GaN) is determined by the ratio of the leakage currents of both diodes in the gate stack. An Ohmic gate provides a good control, but at the expense of a high gate leakage current. A Schottky gate has several decades lower gate leakage, but imposes more constraints on the leakage of the p-i-n diode.

Besides the above, many other process and device parameters need to be considered and optimized: pGaN etch-back, surface passivation, surface cleaning, field plate design, metal routing etc.

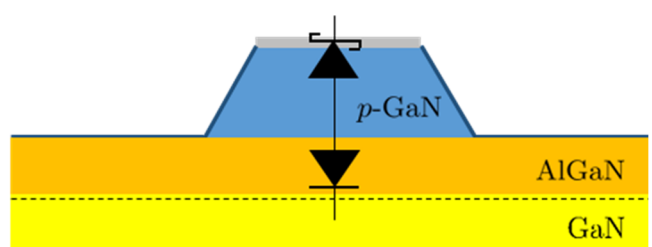

Fig. 3 : pGaN gate device cross-section with the back-to-back diode in the gate stack.

Device development is focused on a 650V rated e-mode product, targeted for 100mΩ. All data is from the k465i MOCVD reactor. Fig. 4 show a statistical data collection of the most important prime device parameters V_{th} (at 10µA/mm), Ig_on (at V_{gs}=5V), Ron (at V_{gs}=5 and 6V) and Dynamic Ron (tested after 300µs in on-state at V_{gs}=5V, after a 10ms off-state stress at V_{ds}=400V, 400V being the on-wafer tester limitation). Data set consists of several 1000's of devices, different lots and wafers. The device parameters except the leakage current exhibit a normal distribution. There is only a small difference of less than 3mΩ in Ron at V_{gs}=5V and V_{gs}=6V (see Fig. 4c), indicating that the device is fully on at V_{gs}=5V. The Ig_on at V_{gs}=5V has a typical value of 15µA, with a tail in the distribution towards a maximum of 100µA.

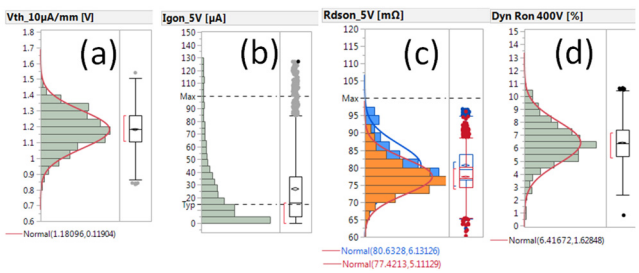

Fig. 4: Statistical data collection for a 100mΩ, 650V eGaN product die: (a) V_{th} at 10µA/mm; (b) Ig_on at V_{gs}=5V; (c) Ron at V_{gs}=5V (blue data) and 6V (red data); (d) Dyn Ron at V_{ds}=400V.

Typical device figures-of-merit Ron*Qoss, Ron*Eoss and Ron*Qg are reported in Fig. 5.

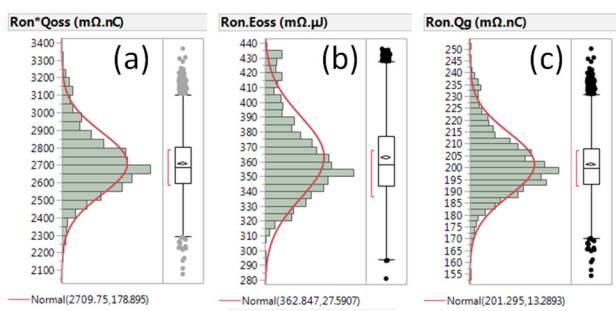

Fig. 5: Device figures-of-merit (a) Ron.Qoss ; (b) Ron.Eoss ; (c) Ron.Qg.

Table 1 compares the results to Si superjunction, SiC MOSFET and two eGaN industrial parts, with a focus on 650V rated devices. For SiC MOSFETs, little offering below 1.2kV exist, only a 900V rated part is available for comparison. For voltages below 1.2 kV, the Ron is mainly determined by the channel resistance, hence not much improvement is expected at 600V. From Table I it is clear that Ron.Qoss is substantially lower for eGaN transistors (~10-15x and ~2x compared to Si SJ and SiC MOSFETs, respectively). Ron.Eoss is somewhat lower than Si SJ, and about ~2x lower than a SiC MOSFET. Ron.Qg is much lower (~15-20x compared to Si SJ, and ~5-10x lower compared to SiC MOSFET). Also the reverse recovery charge Qrr is much lower for GaN compared to SiC (due to the absence of a blocking p-n junction). Since the ON Semiconductor part is driven at 5V instead of 6V gate drive, a low Ron.Qg is obtained.

TABLE I: BENCHMARKING OVERVIEW, COMPARING SI SUPER JUNCTION (SJ), SIC MOSFET, AND EGAN.

		eGaN			SiSJ	SiC
	Unit	This work	Comp1	Comp2		
Ron	mΩ	80	55	100	84	62
Vrating	V	650	600	650	650	900
Vth	V	1.2	1.2	1.3	3.5	2.1
Ciss	pF	124	380	130	2140	660
Qoss*	nC	34	41	28.2	380	85
Eoss*	µJ	4.5	6.5	3.5	5.5	12
Qg	nC	2.5	5.8	3	45	30
Qrr	µC	0	0	0	9	0.25
Ron.Qoss	mΩ.nC	2710	2255	2820	31920	5270
Ron.Eoss	mΩ.µJ	362	358	350	462	744
Ron.Qg	mΩ.nC	201	319	300	3780	1860

*Qoss and Eoss at 400V.

RELIABILITY CONSIDERATIONS FOR E-MODE PGAN.

Since the gate structure consists of two back-to-back diodes (see Fig. 3), the current conduction and the field distribution across the two diodes is not straightforward. Under sufficient forward gate bias, the p-i-n diode is forward biased, and the Schottky is reverse biased. Hence the latter will determine the gate reliability. Fig. 6 shows the I_g-V_g characteristics of the pGaN gate structure, for different temperatures [11]. For 4<V_{gs}<7V, the current conduction is determined by trap assisted tunneling. Above V_{gs}=7V, Poole Frenkel emission is the dominant mechanism.

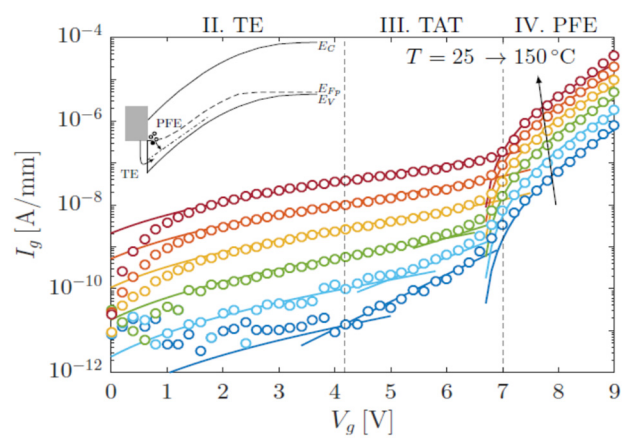

Fig. 6: Current conduction through the pGaN gate stack. Symbols: measured data. Full lines: model. The different conduction models in the Schottky diode are indicated [11].

The information about the current conduction in the Schottky diode is used to extrapolated the TDDB time-to-fail to V_{gs}=7.25V, T=150°C, see Fig 7 [11]. All time-to-fail data (obtained from stress tests 7.75V<V_{gs}<9.25V, and temperatures between 25C and 150°C), fall on one single distribution, which is LogNormal distributed (rather than Weibull). At V_{gs}=7.25V, T=150°C, for a 100mΩ device size, the expected lifetime at 100ppm is ~10^5s. Since the device has a V_{gs_max}=5V, this is well within specification.

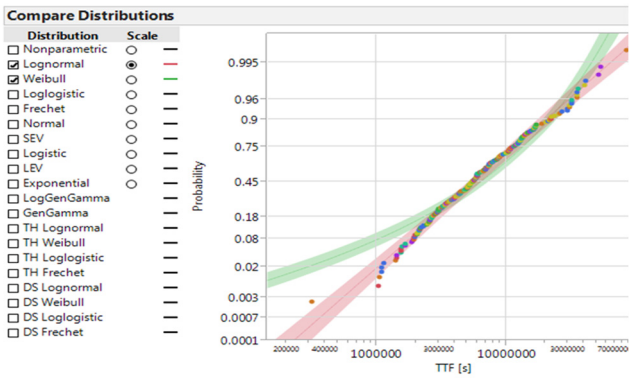

Fig. 7: TDDB time-to-fail data from stress experiments at different temperatures and gate voltages, extrapolated to V_{gs}=7.25V, T=150°C, and fitted with a LogNormal (red) and Weibull (green) distribution function [11].

OUTLOOK FOR 200MM GAN-ON-SI.

200mm GaN-on-Si is pioneered by research groups like imec. The main driving factor to move from 150mm to 200mm is die cost reduction. The issue is to control wafer bow and warp, due to the increased strain by the hetero-epitaxy. With the new generation of MOCVD reactors, this problem is now under control. Device performance for 650V rated eGaN devices, with Ron=450mΩ is shown in Fig 8. The devices exhibit negligible dyn Ron both at RT and T=150°C, and are stable under HTRB at both 520V and 650V, which are 80% and 100% of the rated voltage, respectively [12].

CONCLUSIONS

GaN-on-Si AlGaN/GaN HEMT power devices are entering the market. With the newest generation of MOCVD tools, better layer uniformity and quality can be achieved. p-GaN gated HEMTs are the devices of choice for normally-off operation. However, the control of the p-GaN gate is based on the leakage currents of the back-to-back gate metal/pGaN (p-n) and p-GaN/i-AlGaN/2DEG (p-i-n) diodes. The top diode (gate metal to p-GaN) can be either Schottky type (low leakage current) or Ohmic type (high gate leakage current). This tradeoff has an impact on the on-state reliability. Focussing on the 650V rated eGaN transistors, they largely outperform Si SJ and SiC MOSFET devices.

First data of 650V rated e-GaN power HEMTs on 200mm GaN-on-Si show promising results, both parametrically as well as for reliability. These data indicate that 200mm GaN-on-Si is ready when volume would pick up.

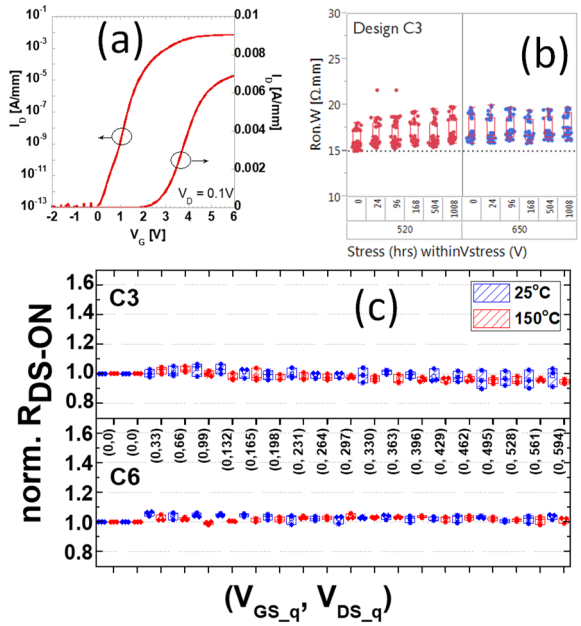

Fig. 8: Power device data for 200mm GaN-on-Si. Data on 450mΩ power devices. (a) transfer characteristics ; (b) HTRB data at V_{ds}=520V and 650V (up to 1008 hrs); (c) dynamic Ron for two different field plate designs [12].

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ACRONYMS

HEMT : High Electron Mobility Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
TDDB : Time Dependent Dielectric Breakdown
HTRB : High Temperature Reverse Bias
SJ : super junction