Channel temperature determination for GaN HEMT lifetime testing – Impact of package and device layout.

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Abstract

Reliability testing of GaN High Electron Mobility Transistors critically relies on the determination of device channel temperature. If inaccurate, this has severe impact on the prediction of device lifetime. Here we use Raman thermography for accurate device temperature measurement, and show that the measured thermal resistance can differ significantly dependent on device layout, package, and test fixture used.

INTRODUCTION

GaN High Electron Mobility Transistor (HEMT) RF amplifiers have enabled a new generation of long range, high speed terrestrial and space communication systems, as well as defense systems. All of these applications require reliability verification. Standard reliability testing tools developed for Si devices such as High Temperature Reverse Bias (HTRB), High Temperature Operating Lifetime (HTOL), Highly Accelerated Stress Test (HAST), or Accelerated Life Testing (ALT) are usually used in adjusted form also for GaN HEMTs. Purpose of this testing is to observe the device response to stress factors such as elevated temperature, voltage bias (HTRB, HTOL, ALT), even humidity (HAST) over certain set time intervals. HTOL tests are used to extract the activation energy of the dominant degradation mechanism and predict mean time to failure (MTTF). HTOL testing requires accurate channel temperature determination at the operating condition used. The high thermal conductivity materials in the GaN epitaxial stack, GaN (~160W/mK) and SiC (~450W/mK), allow for efficient thermal dissipation and therefore higher power dissipation densities (P_{diss}) compared to previous technologies, e.g., GaAs pHEMTs. In GaN devices, an effective thermal boundary resistance (TBR_{eff}) exists between the epitaxial GaN layer and the SiC substrate, which is associated with the nucleation layer[1]. Other than epitaxy and device layout[2], die attach and package materials, and thermal resistance between the package and test fixture contribute to the device on-state temperature rise. Thermal simulation is used to determine the peak channel temperature, but these results must be experimentally verified because of uncertainties in model input parameters, particularly the TBR_{eff} and die attach interfaces. In this paper, we present the Raman thermography temperature rise measured on 2-10 finger GaN-on-SiC devices from a selection of commercial manufacturers. Our data show how device layout, different packaging, and test fixtures have a significant impact on thermal resistance.

MATERIALS, MEASUREMENT TECHNIQUE, AND SIMULATION

All studied devices were AlGaN/GaN HEMTs on SiC substrates with various degrees of packaging (on-wafer, diced and brazed to carrier, in RF package) and mounted (with or without using of specialised test fixture e.g. such as used in Accel RF systems). A thermoelectric chuck was used to fix the backplate temperature to different ambient temperatures (T_a). An InVia confocal Raman spectrometer using laser excitation at wavelengths of 488 and 532 nm was used to acquire Raman spectra 0.5 µm away from the drain edge of the gate or field plate, near the location where the maximum temperature rise occurs. A 50x 0.5NA objective lens was used to focus the light to a lateral spot size of 0.5 µm. T_{ch} was determined from the temperature shift of the E_2 and A_1(LO) GaN phonon modes. Further details about the Raman thermography technique can be found in Refs[2–7]. Thermal resistance (R_{th}) of the devices (including packaging, where applicable) was extracted from T_{ch} vs P_{diss} plots. We note Raman thermography probes an average temperature of a finite material volume and peak channel temperature (often located underneath the gate contact, optically inaccessible) can be extracted from the measured data with the aid of simulation[3]. 3D finite element steady-state thermal simulation of a 10 finger GaN on SiC HEMT was used to extract the influence of some of the device dimensions and material parameters (chip size, TBR_{eff}, GaN channel thickness, SiC substrate thickness, die attach and chip carrier thermal conductivity) to peak channel temperature rise. Device dimensions (W_g=125µm, GG=30µm) were selected to match measured 10 finger HEMTs to provide a comparison with experimental data. Typical reported values of epitaxy layer structure and material parameters were used.[3]

RESULTS AND DISCUSSION

Fig. 1 shows T_{ch} vs P_{diss} for 2-4 finger devices and documents an influence of device layout. Devices from Manufacturer A show a more than about two-fold increase in

T_{ch} compared to the other on-wafer devices, as a result of decreased gate to gate finger spacing (GG), as expected and consistent with our earlier results[2]. Clearly, mounting the devices in a package results in significantly increased channel temperature rise as illustrated for the devices measured from manufacturers C and D. However, larger gate width of these devices need to be considered as it has strong influence on the T_{ch} too. We typically find the extent of the increased channel temperature depends on the detailed package and the brazing used. Here it is likely due to that most of the R_{th} originates from limitations in heat transport in the brazing or package, although differences in TBR_{eff} between both device samples and T_a may also contribute. Interestingly, the thermal resistance of the narrowest GG device from manufacturer D (packaged) is similar to the on-wafer device with similar GG from manufacturer A (~15% difference) indicating differences in TBR_{eff}. However, packaging influence needs to be considered. Also important factors are thickness of the GaN layer and the length of the field plate (if present); Both affects measured temperature, although not necessarily the peak temperature.

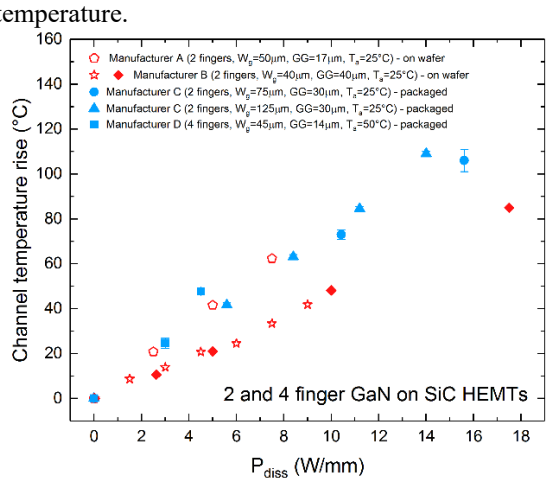

Fig. 1. Measured channel temperature rise vs dissipated power density for 2- and 4-finger GaN on SiC HEMTs, at different ambient temperatures T_a. The devices had different Gate-to-Gate (GG) spacings, some were measured on wafer.

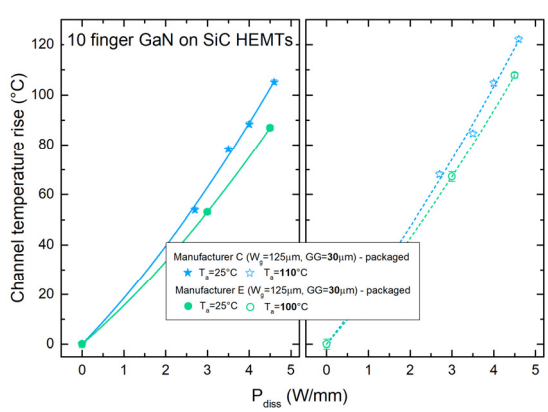

Fig. 2. Comparison of measured channel temperature rise vs dissipated power density for 10-finger packaged GaN on SiC HEMTs at different ambient temperatures; 25 and 100-110 °C.

The influence of temperature-dependent thermal conductivity (κ) is indicated by Fig. 2 showing data for 10 finger devices with W_g=125µm operated at different backplate temperatures. Thermal resistance (the slope of the T_{ch} vs P_{diss}) is clearly increased when operating the devices at a higher backplate temperature, also summarised in Fig. 3. Device from manufacturer C was brazed onto proprietary test fixture, whereas device from manufacturer E was brazed to the RF package and then mounted onto the test fixture. The latter shows a 15% smaller R_{th} than for devices mounted in another test fixture at T_a=25°C. At an increased T_a this difference was reduced to 7.5%.

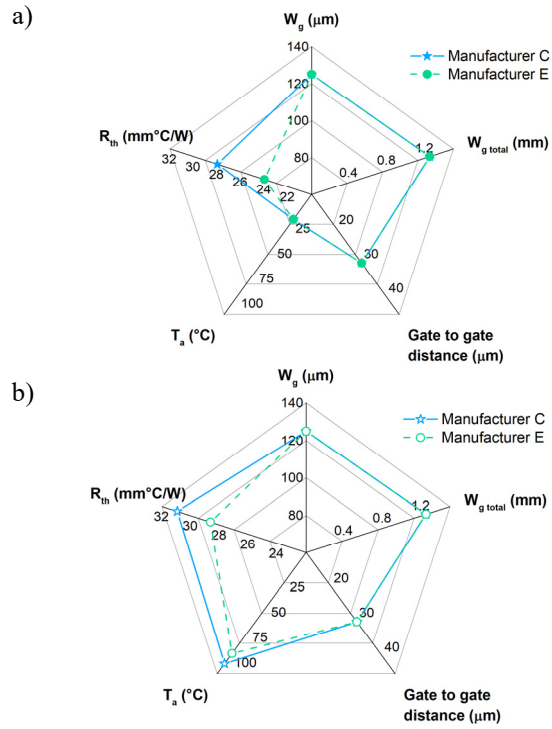

Fig. 3. Plots of 10-finger devices showing some of their key parameters (including their R_{th}) at different backplate temperatures a) at T_a=25 °C, b) at T_a=100-110 °C.

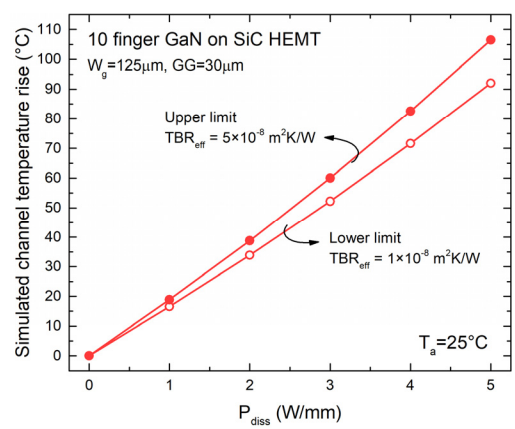

Fig. 4. Simulated channel temperature rise vs dissipated power density for 10-finger GaN on SiC HEMT at ambient temperature T_a=25°C showing an influence of varied TBR_{eff}.

This may be caused by differences in temperature-dependent thermal conductivity of used brazing and packaging materials, however TBR_{eff}[1] can have similar effect. This is documented by Fig. 4 showing simulated values of channel temperature rise as a function of dissipated power density in a finite volume of GaN channel, 0.5 µm away from the drain edge of the gate metal to match the experimental measurement conditions. By varying of the TBR_{eff} value between $1 – 5\times10^{-8}$ m^2K/W, an additional R_{th} increase of ~12-15% can be observed.

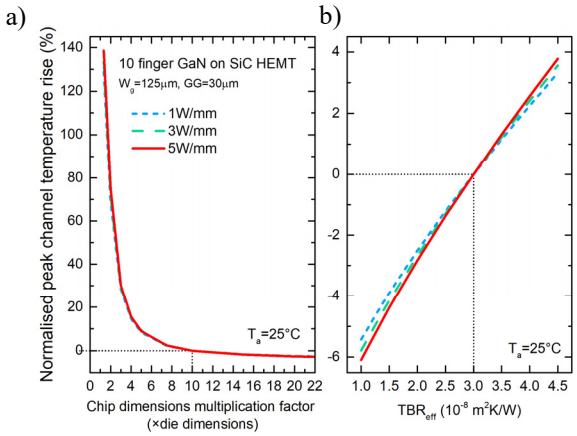

Fig. 5. Simulated normalised peak channel temperature rise at T_a=25 °C as a function of varied a) lateral chip dimensions b) values of TBR_{eff}.

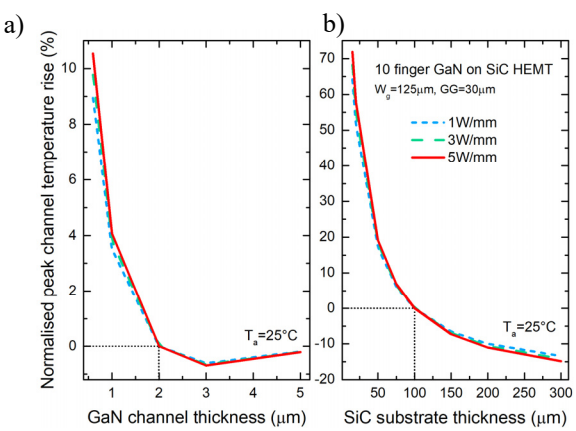

Fig. 6. Simulated normalised peak channel temperature rise at T_a=25 °C as a function of varied a) GaN channel thickness b) SiC substrate thickness.

The influence of chip dimensions and TBR_{eff}, GaN and SiC thicknesses, and die attach and chip carrier thermal conductivities to peak channel temperature as extracted from the thermal simulation of 10 finger device (W_g=125µm, GG=30µm) is documented in Fig. 5 – 7, respectively. Expectedly, reducing the chip area causes decreased heat spreading into the GaN and SiC and can lead to ~1.5 times increase in the peak channel temperature (Fig. 5a). This should be considered when dicing the chips.

If TBR_{eff} is decreased or increased within values reported previously[1], this can have ~10% influence on the peak channel temperature (Fig. 5b).

Thicknesses of GaN channel and SiC substrate affect lateral heatspreading, however the possible device self-heating-lowering effect is rather insignificant. Thickness of GaN, however, affects the measured temperature as it relates to the volume probed by Raman thermography. Typical device design uses ~2µm thick GaN channel layer and 100µm thick SiC substrate. Substrate thickness is dictated by the operating device frequency and cannot be arbitrarily changed, so thicker SiC layer is not an easy to implement option.

Devices brazed to the carrier can benefit from high thermal conductivity die attach and carrier/flange materials. Currently, the industrial standard for die attach is AuSn solder (κ ~ 57 W/mK), but AuSi or Ag sintered epoxies can decrease the channel temperature rise up to ~4%.

Fig 7b depicts the influence of common alloys (coefficient of thermal expansion, CTE, matched to GaN and SiC) when used as a material for chip carrier. CuW and CuMo are typically used materials. As compared to these, up to ~20% increase or ~12% decrease in device channel temperature rise can be achieved if materials such as alumina (κ ~35 W/mK) or advanced Ag-diamond composite, respectively, are used.

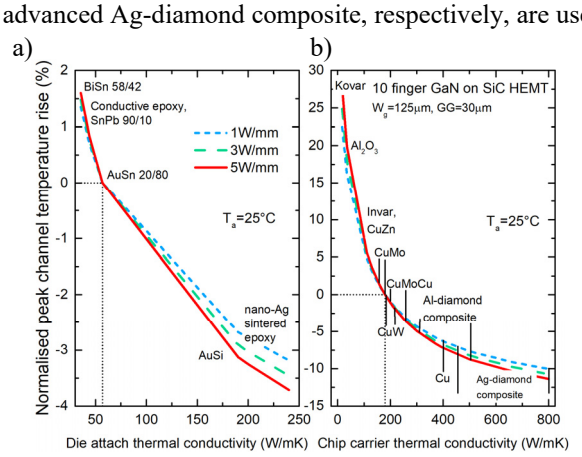

Fig. 7. Simulated normalised peak channel temperature rise at T_a=25 °C as a function of varied a) die attach thermal conductivity b) chip carrier thermal conductivity.

An importance of the material of the text fixture increases for high power devices. In that case, the temperature difference (ΔT) across the fixture increases and so does it's R_{th}. However, if common alloys are considered, there is only negligible advantage of using materials with high thermal conductivity for the considered 10 finger device at typical dissipated power densities (1 – 5 W/mm).

Similarly, significance of used materials and manufacture processes of die attach and chip carrier increases dramatically for large/high power devices.

Clearly, it is critically important to determine not only the channel temperature of the device on wafer or on-chip, but also in the test fixture used for the accelerated lifetime testing. However, to provide a better insight into the contributions

of individual parameters and to produce a fair comparison, apart from providing only a T_{ch}, a standard edge-of-the-chip temperature (substrate temperature not affected by the heating of the device) and temperature of the packaging and test fixture need to be known.

CONCLUSIONS

Device reliability lifetime testing relies on accurate (peak) channel temperature determination. Here we demonstrated some of the key factors affecting channel temperature which need to be considered when carrying out the reliability testing.

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