Addressing 0.25 um T-Gate Lithography Defects through Data Fit Model Analysis

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Distribution Statement A: Approved for Public Release; Distribution is Unlimited; #19-0099; Dated 02/07/19

Keywords: III-V semiconductor; electron beam lithography; 0.25 micron; T-gate; lithography defect; PMMA resist

Abstract

The Gallium Arsenide (GaAs) psuedomorphic high electron mobility transistor (pHEMT) fabricated at the Advanced Technology Laboratories (ATL) uses a T-Gate structure to improve transistor performance for microwave- and millimeter-wave frequency integrated circuits (MMIC's). An unresolved lithography template produces defective T-Gates which negatively impacts device electrical performance. This work stems from a recovery team's efforts to address a defect observed within the main gate stripe of a 0.25 um T-Gate lithography process. Resist thickness and develop process parameters were optimized to mitigate an intermittent clearing defect, increasing overall quality of the resulting lithography-defined structures.

INTRODUCTION

The T-Gate lithography module used at the Advanced Technology Laboratories consists of a tri-layer resist coat, Electron Beam (Ebeam) expose, and a two-step develop procedure. During production of a 0.25 um T-Gate using standard process of record (POR) conditions in the T-Gate lithography module, an intermittent resist clearing defect was observed. The defect is associated with darker regions of non-uniform widths along the gate stem, while optimal gate structures display brighter and more uniform dimensions. In the scanning electron microscopy (SEM) images, the underlying conductive substrate is bright, while the resist covered sections are dark. Specifically, due to conductivity differences between the underlying layer and resist the effective clearing of the exposed resist can be directly correlated with the percent brightness of the image. Additionally, the standard deviation of the brightness distribution can be used to quantify the extent to which the gate resist is cleared.

To effectively discuss the impact of the intermittent clearing defect on gate quality, quantitative gate quality parameters were extracted from the critical dimension scanning electron microscopy (CDSEM) images. Data analysis via an original MATLAB® algorithm produced four low noise standard metrics to evaluate the quality of the main gate stripe. Parameters consisted of average brightness percent (AB), brightness standard deviation percent (BStdev), width accuracy (ΔW), defined as delta from target line width in nm, and width standard deviation in nm (WStdev). These parameters were chosen due to their strong correlation with the qualitative characteristics of interest encompassing both defective and ideal T-Gate structures.

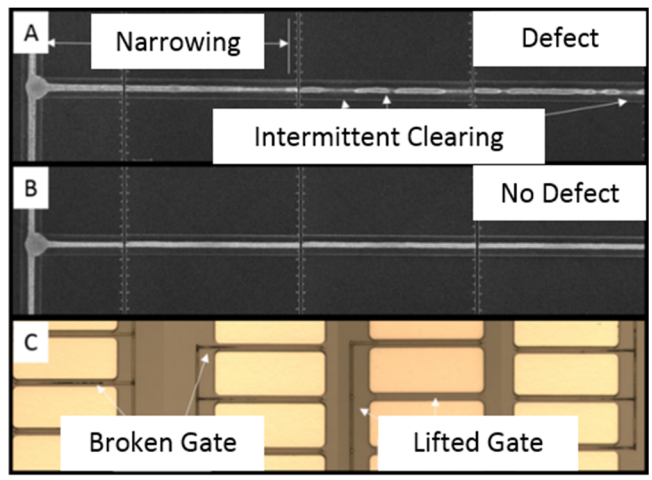

Figure 1: Sample lithography CDSEM images (top down) of a T-Gate resist profile A) Intermittent Clearing Defect. B) Ideal Gate. C) Impact of defect on metal T-Gate formation, showcasing broken and lifted gates.

Sample images of a defective T-Gate reflecting a typical wafer affected by the intermittent clearing phenomena are shown in Figure 1A). For reference, a well-defined main lobe stem along the entire gate length, characteristic of an ideal gate, is displayed in Figure 1B). The intermittent clearing observed within the lithography module induces defects within downstream processing flows and can be correlated with broken or lifted gates after metallization and lift off as shown in Figure 1C). Issues during metallization are likely due to poor gate adhesion induced by the intermittent clearing defect.

With the goal of mitigating the clearing defect, sample trials were executed using a combination of standard

experimentation and full factorial experiments. Statistical analysis of processing factor effects on the gate quality metrics indicate resist thickness, followed by descum ash recipe and develop time have the largest standardized effect on the defect of interest. A new procedure with a larger processing window was created utilizing an increased resist thickness coupled with a decrease in the duration of the first develop step. Prior to optimization efforts, gate structures displaying the clearing defect typically showed average brightness values at or below 60% and a width standard deviation greater than 20 nm. Ideal gate structures defined by the newer more robust process display average brightness values greater than 70% and width standard deviation values less than 10 nm. This work seeks to serve as a reference for potential routes of gate quality optimization and T-gate process development. Results related to process optimization considerations and resist/topography interactions are also discussed.

METHODS

Device-quality experimental wafers were fabricated using the lithography T-Gate module which consisted of a coat, expose, and develop step. A spin coating method was employed to create the tri-layer resist profile. The bottom and top resist layers were spun using a 495k MW polymethyl methacrylate (PMMA) resist, with a 4% polymer resin suspended in chlorobenzene. The intermediate El-10 layer was composed of a copolymer containing a 10% solid resin of 8.5% PMMA and + 1.5% methacrylic acid (MAA) suspended in ethyl lactate applied via spin coating.

Next, the CAD patterns used for the Ebeam exposure were all fractured using the same resolution and beam step size. The wafers were then exposed with an accelerating voltage of 20 keV, with negligible variation in the spot size, current, beam mode settings, dose, and quality.

Finally, after pattern exposure, the wafers were developed in a three-step process. The first develop consisted of a xylene and toluene developer (X:T), and subsequent xylene rinses. This was followed by a descum option to clean the wafer surface before the second and final developer treatment. The second developer was a methyl isobutyl ketone and isopropanol developer mix (MIBK:IPA) followed by two IPA rinses. This step resolved the remaining resist layers to produce a lithography T-Gate template.

RESULTS

Figure 1 serves as a visual baseline in which the gate quality of an ideal vs. defective gate result can be compared. The two example structures with (Figure 1A) and without (Figure 1B) the intermittent clearing defect strongly correlate with the four relevant output metric values. The ideal gate outperforms the defective gate in all four metrics. The ideal gate is brighter than the defective gate, indicating greater resist clearing. In addition, the defective gate's ΔW is larger than the ideal gate metric, denoting a less controlled process. Similarly, both the standard deviation in brightness and width are higher for the defective gate, indicating low uniformity and gate quality. Overall, the ideal gate shows an increase in brightness indicating a clearer gate stem, a smaller ΔW, and lower standard deviation values for both brightness and width.

Twenty-two unique processing conditions were investigated to evaluate the impact of EL-10 resist thickness and the X:T develop time on gate quality. Figure 2 summarizes experimental splits consisting of two El-10 Thicknesses (POR−20% nm, POR +20% nm) and six X:T develop times ranging from POR−30% minutes to POR+20% minutes. Results indicate a thinner EL-10 resist layer correlates with lower brightness values, higher standard deviations in both width and brightness, and a greater delta between average stem width and target (Figure 2 A,C, E, G).

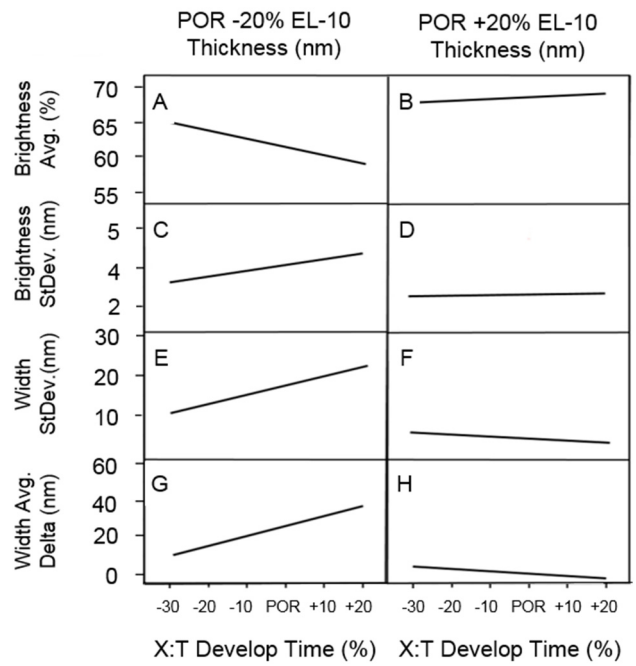

Figure 2: Displays the fit-model predicted impact of X:T Develop time at POR -20% nm EL-10 thickness (A, C, E, G) and POR +20% nm EL-10 thickness (B,D,F,H) on the four gate quality metric outputs. Outputs consist of average brightness percent (AB), brightness standard deviation percent (BStdev), width accuracy defined as delta from target line width in nm (ΔW), and width standard deviation in nm (WStdev).

Conversely, as the EL-10 thickness increases from POR−20% nm to POR +20% nm, we observe the opposite trend. Spin coating a thicker resist layer correlates with higher brightness values, lower standard deviations in both width and brightness, and a smaller delta between average stem width and target (Figure 2 B, D, F, H). These results suggest that a

thicker EL-10 resist layer produces higher quality gates. When the POR EL-10 thickness was used, the original process produced gates with varying results. Based on Figure 2 results, a new method with an increased resist thickness of POR +20% nm was applied to improve the process by mitigating the intermittent clearing defect.

Figures 2 (A, C, E, G) show an increased dependency of the gate quality metrics on X:T develop time for samples with a POR−20% nm EL-10 layer compared to a POR +20% nm EL-10 thickness. Figure 2 (B, D, F, H) shows a smaller dependence on X:T develop time for POR +20% nm samples, as evinced by the more horizontal modelled curve for X:T develop time. At thinner EL-10 thicknesses, results suggest increasing the X:T develop time from POR−30% minutes to POR+20% minutes has a negative impact on gate quality. Results also indicate a shorter develop time increases the gate quality for thinner resists. With thinner resist trials, longer develop times correlate with lower brightness values, higher standard deviations in both brightness and width, and a greater delta between average stem width and target.

As discussed above, the output metric dependence on X:T develop time is highly pronounced for samples with thinner EL-10 resist layers. However, as the EL-10 thickness increases, the impact of varying the X:T develop time decreases significantly as seen in Figure 2 (B, D, F, H). For instance, the dependency of AB on X:T develop time, indicated by the slopes of Figure 2A and 2B, is 4.55 times greater for POR−20% nm samples than POR +20% nm samples. Additionally, the greater slopes for standard deviation in brightness and width of samples at POR−20% nm vs. POR +20% nm confirm a larger dependence on the X:T develop time for thinner EL-10. The samples coated at POR−20% nm display X:T dependence values greater by factors of 9.89 and 2.57 for standard deviation in brightness and width, respectively. This trend is also mirrored in the average width from target delta, in which the slope dependence of the 350 nm trials is greater by a factor of 8.32 than the POR +20% nm trials.

Independent of EL-10 Thickness, reducing the develop time correlates with improvement in three out of 4 output parameters. For samples coated with POR +20% nm of EL-10, a change of sign is observed in the average ΔW fit models. As the X:T develop time is increased from POR-30% minutes to POR-10% minutes, the ΔW approaches zero from a positive delta. Continuing to increase the X:T develop time over 5 minutes results in modeled ΔW values which continue to trend lower than zero. In this context, because ΔW values are reported as absolute values, negative regions in the fit model reflect a region of minimized delta from target width where optimal line width accuracy is achieved. With respect to WStdev, POR +20% nm EL-10 trials show a negative relationship with X:T develop. The total range in WStdev spanned only 4 nm – 5 nm which is within tolerance.

Additionally, POR +20% nm thick EL10 trial results indicate that a longer develop time increases the AB and BStdev negligibly by 0.004% and 0.001% respectively. These results indicate a more robust process window is achieved when the POR +20% nm thick EL-10 layers are used. For these samples, large changes in the X:T develop time had minimal impact on gate quality indicating a larger process window.

RESIST PROFILE

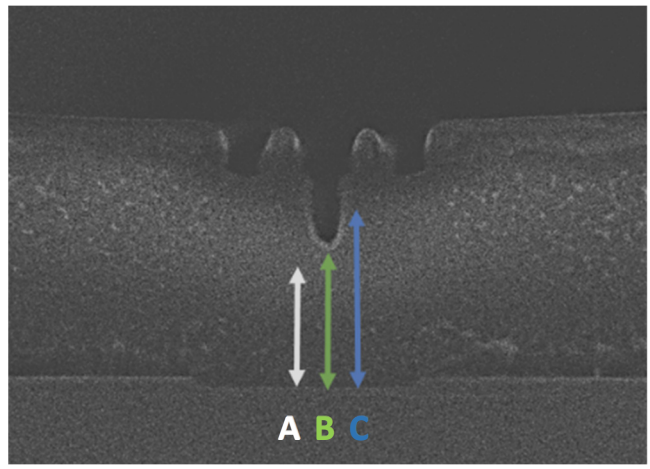

Figure 3: Resist profile of a tri-layer resist stack after the initial xylene:toluene develop A) POR-20% (nm) thick resist, 1st develop penetrates 14% closer to substrate surface compared to POR, B) POR (nm) thick resist C) POR+20% (nm) thick resist, 1st develop stops 31% farther away from substrate surface than POR

This wider process window may be attributed to an overall decrease in the penetration of the first develop relative to the wafer surface (Figure 3). As the thickness of the EL-10 resist layer increases, there is a corresponding increase in the thickness of undeveloped co-poly resist regions above the wafer surface (Figure 3B). This correlates with results shown in Figure 2 (B, D, F, H,), which indicate a higher quality gate is achieved with POR+20% nm. This tuning of the penetration of the 1st develop likely impacts the wafer clearing during the 2nd develop.

Figure 4 displays positive-tone tri-layer resist stack profiles throughout the T-gate lithography process. To better understand the defect, cross sectional SEM images were obtained throughout the coat and develop processes, shown in Figure 4 (C and F). Based on these images a more realistic schematic of the T-gate resist profile after develop was compiled in Figure 4 (B, E, H). Notably, the images highlight significant differences between conventionally represented and actual resist profiles between the S/D pads. The conventional representation does not capture the pooling of

resist that induces a significantly thicker co-poly layer (Figure 4B). In addition, the top PMMA layer is often depicted with a highly selective removal of the exposed area after the top X:T develop step, leaving the underlying co-poly layer intact. However, systematic in-line characterization indicates removal of material in the main and side lobe exposure areas penetrating the middle co-poly layer in a three-pronged pattern.

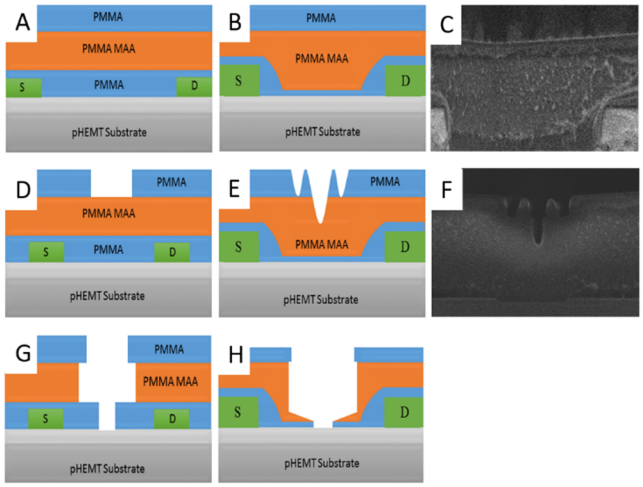

Figure 4: Schematic and scanning electron microscopy images of resist profiles during various stages of an Ebeam lithography T-Gate process. A, B and C) Resist coat. D, E, and F) Resist profile after top develop. G and H) Resist profile after bottom develop. Conventional T-Gate resist profile representation: A, D, and G. Cross Section Informed T-Gate profile representation: B, E and H.

To evaluate T-Gate Metallization Focused Ion Beam (FIB) destructive analysis was performed on select samples to evaluate the impact of the processing changes on downstream metallization and liftoff steps. Figure 5 shows comparative FIB images of gate structures after metal deposition and liftoff. Figure 5 (A, and B) show FIB results from a wafer coated with POR nm of EL-10 resist, during gate lithography. Figures 5 (C, and D) show results from a sample coated with POR+20% nm of EL-10 resist. The POR nm sample gates show inconsistent contact with the underlying metal layer. The POR nm gate samples also correlate with a lower measured brightness as compared to the POR+20% nm samples. Conversely, the POR+20% nm gate shows ideal contact with the underlying metal stack correlating with the higher measured brightness values. It should be noted that metal wings, protrusions of metal along the feature edges, are observed on the POR+20% nm sample. Future work may center on reducing the relative frequency of the post-metal artifacts. Currently, to mitigate any impact on electrical performance, gates are immediately passivate after liftoff to prevent metal wings from detaching and short-circuiting the device.

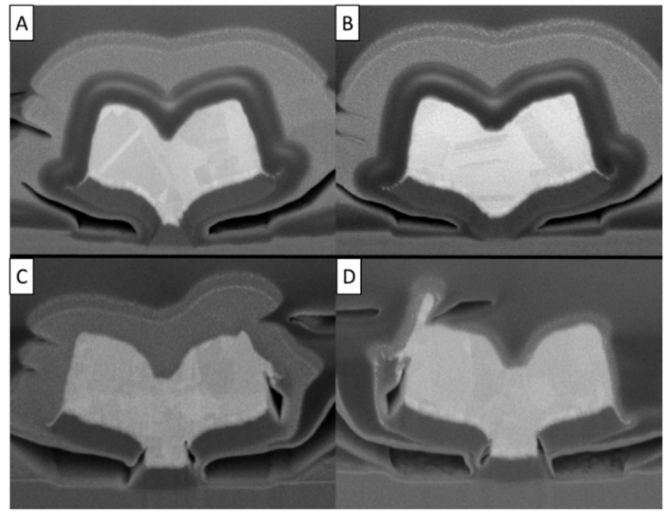

Figure 5: Focused Ion Beam cross sections of the metalized T-Gate. Original Process A) POR nm EL-10 thickness. B) POR nm EL-10 thickness. Optimized Process C) POR+20% nm EL-10 thickness. D) POR+20% nm EL-10 thickness.

CONCLUSION

This work describes the impact of several processing factors on the quality of a 0.25 um pseudomorphic high electron mobility transistor (pHEMT) T-gate process and the resolution of an intermittent clearing defect issue. Gate quality evaluation was based on critical dimension scanning electron microscopy images. Image analysis produced four metrics to evaluate the quality of the main gate stripe. We showed that resist thickness followed by descum recipe and develop time have the largest standardized effects on the metrics of interest. An increased co-poly thickness coupled with a decrease in the X:T develop time showed improvements in all four output metrics, producing gates with greater brightness as well as improved accuracy and precision. This could serve as a reference for potential routes of gate quality optimization, and T-gate process development.

ACRONYMS

Ebeam: Electron Beam
POR: Process of Record
CDSEM: Critical Dimension SEM
AB: Average Brightness
ΔW: Delta from Target Width
WStdev: Standard Deviation in Width
BStdev: Standard Deviation in Brightness
FIB: Focused Ion Beam