Development of InP DHBTs with High Breakdown Voltage for Ka-Band PA Applications

Yuefei Yang[1], Dheeraj Mohata[1], David Rasbot[1], R. Soligo[1], David Wang[1], Robert Bayruns[2], John Bayruns[2], David Osika[2] and Joseph Brand[2]

[1]Global Communication Semiconductors, LLC. 23155 Kashiwa Court, Torrance, CA. 90505
[2]Duet Micro Electronics, Inc. 575 Rt 28 Suite 100n Raritan, NJ 08869
Email: yfyang@gcsincorp.com, Tel: 310-530-7274 Fax: 310-530-7279

Keywords: InP DHBTs, Breakdown voltage, PA applications, 5G PA

Abstract

InP DHBT breakdown behaviors and device performance have been studied with different collector structure design. An abrupt breakdown characteristic, BVceo of 11V and low knee voltage are obtained with a proper collector transition layer design. The devices show good RF and power performance with f_T of 115GHz and *fmax* of 150GHz. Good power performance of a 28GHz PA has been demonstrated with PAE of 54% and Psat of 26dBm. The InP DHBTs developed are good candidate for Ka-band PA applications.

INTRODUCTION

HBTs are known for their high linearity, high efficiency, and high frequency response for RF power amplifiers. GaAs HBTs are widely used in current wireless communication systems below 6GHz. In the later phase of 5G deployments, Ka-band frequencies (26.5 to 40GHz) will most likely be used. GaAs HBTs obviously cannot meet this frequency requirement. Currently available technologies include 0.15µm GaAs pHEMT, 0.15µm GaN HEMT and SiGe BiCMOS and advanced SOI CMOS, which all have their own drawbacks in different aspects. For example, the use of 0.15µm gate lengths in HEMT technology may require e-beam lithography which tends to be a high-cost solution. A significant drawback to HEMT technologies is that they require negative supplies for the gate bias which adds cost and complexity. InP/InGaAs HBT provides high frequency response, does not require a sub-micron process and negative supplies, and is a good candidate for Ka band PA applications [1-3]. However, InP HBT process is not as straightforward as GaAs HBT process. Some issues still need to be resolved before it becomes manufacturable. The main challenge is the high leakage current at base-collector junction, which is sensitive to epi design [4] in addition to process and passivation. In this work, we will present how the epi design affects leakage current and report an InP DHBT with high $f_T/fmax$, an 11V breakdown voltage and good power performance suitable for Ka-band PA applications.

EPI DESIGN AND DEVICE FABLICATION

The InP DHBT epi wafers were grown by MBE and its structure consists of a n^+-InGaAs cap layer, n-InP emitter, a carbon-doped InGaAs base layer, an n^--InP collector structure with an n^--InGaAs/AlInGaAs grading transition layer between InGaAs base and InP collector to eliminate electron blocking and an n^+-InP sub-collector layer. Different collector structures are designed to study base-collector junction leakage and collector-emitter breakdown voltage. To have good PA performance, high device breakdown voltage is desirable, but its tradeoff is speed, on-resistance and knee voltage. To obtain high breakdown voltage of an InP DHBT device is a challenge because the base-collector junction is prone to high leakage due to the narrow band gap of InGaAs used in the collector transition layer. We have found that collector-emitter breakdown voltage (BVceo) is highly affected by the collector design. Table I shows 3 different collector structures. Dev. A and Dev. B have the same n^--InP collector thickness but different n^--InGaAs/AlInGaAs collector grading transition layer thickness. Dev. C. has thinner InP collector thickness with optimal n^--InGaAs/AlInGaAs collector grading transition layer. Emitter and base designs are the same for all structures.

TABLE I
COLLECTOR EPI LAYER STRUCTURES FOR 3 DIFFERENT COLLECTOR DESIGNS

HBT Epi Layers	Dev. A	Dev. B	Dev. C
p^+- InGaAs Base sheet resistance (Ω/sq.)	650	650	650
n^--InGaAs/AlInGaAs collector grading transition layer thickness 500-1000A	T1	T2	T3
n^--InGaAs/AlInGaAs collector grading transition layer doping.	D1	D1	D3
n^--InP Collector thickness with same doping (Å)	4000	4000	3500

The key process steps include self-aligned emitter metal/emitter mesa, non-self-aligned base metal, base mesa, collector metal, and collector mesa. BCB is used for device passivation, planarization, and also as low-loss interlayer dielectric between first and second level metals. BCB via etch process is employed to expose emitter, base, and collector metals for the first-level metal to access those three contacts, and for M1-M2 connection as well. TaN thin film resistor and Si_3N_4 MIM capacitor are used for monolithic integration of passive components. Backside through-substrate via with low-inductance grounding is used for ground connection. Devices with different emitter widths from 1.0 to 1.6 μm are fabricated.

DEVICE PEFORMANCE

DC IVs were tested for different collector designs. Fig.1 shows Iceo versus Vce curves with log and linear scales. For the same InP collector thickness, BVceo of Dev. A is much lower than that of Dev. B, which indicates that the collector transition plays an important role in the breakdown voltage. The breakdown behavior is soft for both Dev. A and Dev. B. This is because the high leakage current masks out the intrinsic avalanche breakdown. With an optimal transition design as in Dev. C, even with a thinner InP collector its breakdown behavior is very abrupt, which indicates that the leakage current is low, and it reaches intrinsic avalanche breakdown. BVceo of 11V is achieved for Dev. C, which is higher than that of Dev. A and Dev. B. Fig.2 shows a 4-inch wafer map of BVceo tested at Iceo of 20μA for an DHBT with 4 1.6x10 μm^2 emitter fingers in parallel. The average value is 11V. BVceo uniformity is good across a 4-inch wafer except for one defective device.

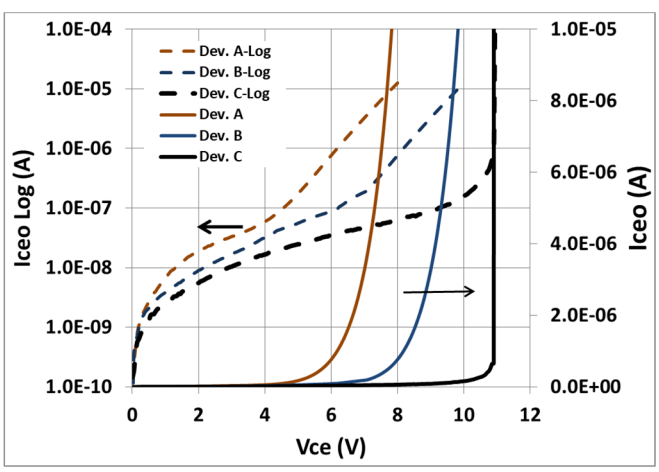

Fig. 1. Iceo vs Vce curves for Dev. A, B and C. Solid lines are linear scale and dash lines are log scale for a device with emitter size of 1.6x10 μm^2.

Low knee voltage and low on-resistance are desired to have high maximum RF output power and efficiency for PA applications. InP collector thickness/doping and collector grading transition layer will affect knee voltage and on-resistance. Fig. 3 shows IV curves of a 1.6x10 μm^2 device using designs of Dev. A, B and C at two different collector current densities. Dev. C shows the lowest knee voltage and on-resistance due to its thinner collector thickness. Collector electron blocking effect is well eliminated. Fig. 4 shows the IV curves of Dev. C with emitter size of 1.6x10 μm^2. Its current gain is ~50 across a wide collector current range. The knee voltage measures 0.8V at *Jc* of 150kA/cm^2.

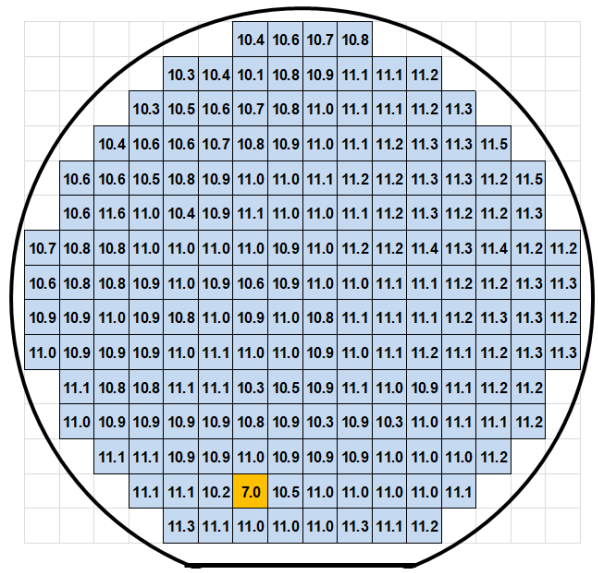

Fig. 2. BVceo wafer map for a 4-finger 1.6x10 μm^2 device.

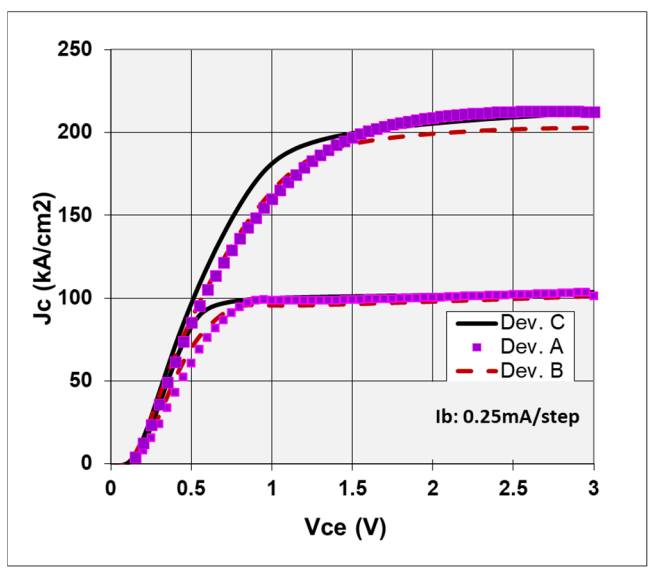

Fig. 3. IV curves to show knee voltages at high collector current densities for a 1.6x10 μm^2 HBTs using designs of Dev. A, B and C.

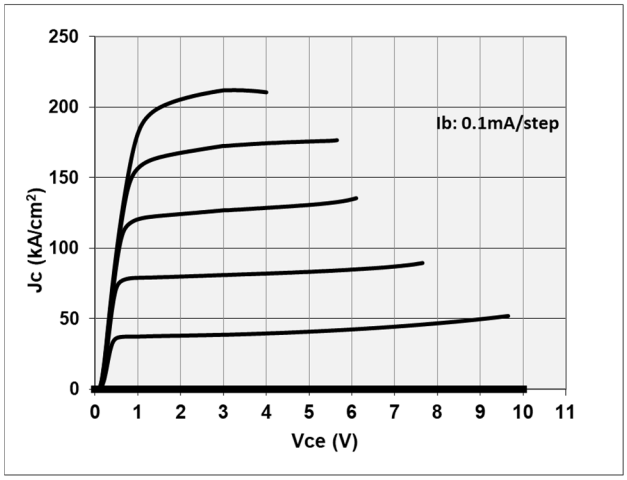

Fig. 4. IV curves for Dev. C with emitter size of 1.6x10 μm².

On-wafer small-signal RF performance was measured with a vector network analyzer in the frequency range of 0.5 to 40GHz. Fig. 5 shows f_T and *fmax* versus *Jc* at Vce = 3.5V. Peak f_T and *fmax* are 115GHz and 150GHz, respectively, which are sufficient for Ka-band PA applications. Table II summarizes some device parameters for 3 different designs. Dev. C shows both high breakdown and low knee voltage, which is ideal for PA applications.

Fig. 6 shows load pull data of a 1.6x20 μm² Dev. C at 18GHz and Vce=5V. Linear gain of 14dB, and PAE>45% are obtained. Psat power density is about 2mW/μm² (or 3.2W/mm of emitter length) which is much higher than that of typical GaAs HBTs and pHEMTs. Due to test equipment limitation, load pull test was done only at 18GHz.

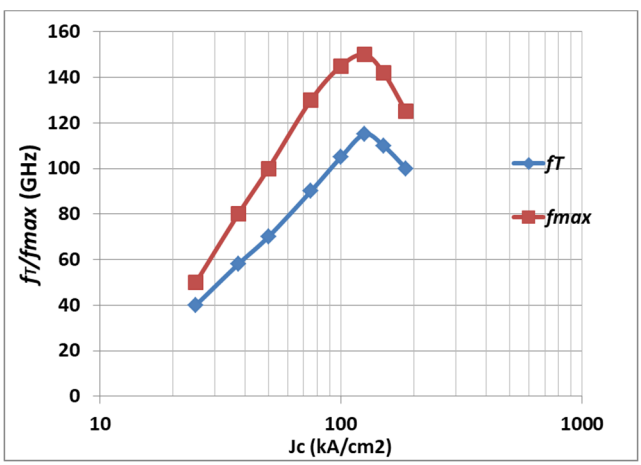

Fig. 5. f_T and *fmax* vs collector current density for Dev. C with emitter size of 1.6x10 μm².

TABLE II
SUMMARY OF DEVICE FOR A 1.6X10 μm² DEVICE WITH 3 DIFFERENT COLLECTOR DESIGNS

HBT Parameters	Unit	Dev. A	Dev. B	Dev. C
BVceo at Iceo 1E-5A	V	8.7	9.7	11
BVceo breakdown behavior		Soft	Soft	Hard
Knee voltage at *Jc* 100kA/cm²	V	0.8	0.8	0.6
Peak f_T	GHz	-	-	115
Peak *fmax*	GHz	-	-	150

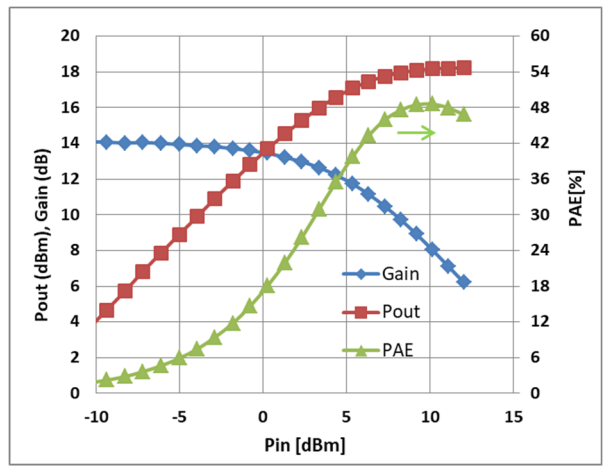

Fig. 6. Load pull data of a 1.6x20 μm² DHBT device with Dev. C design at 18GHz and Vce=5V

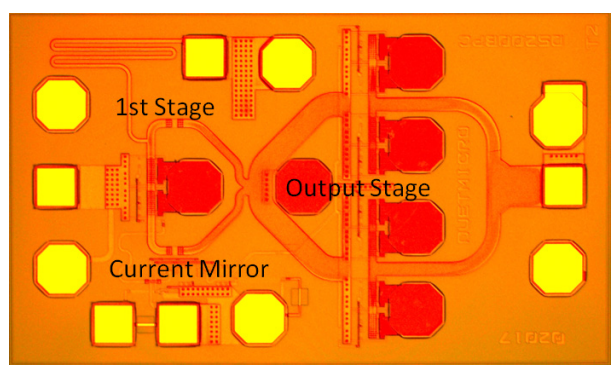

Fig. 7. A picture of a 28GHz PA MMIC.

To evaluate PA performance, a two-stage PA was designed and fabricated as shown in Fig. 7. The first stage input has a bandpass match topology; the inter-stage match is low-pass as well as the final output match. Output stage uses a device with 16 1.0x10 μm² emitter fingers. Fig. 8

shows the measured S21 at Vcc=3V. The gain from 27.5-28.35GHz is about 18dB. Max PAE of >50% is obtained at 28GHz which is much better than 45nm CMOS technology [5] and 0.15µm pHEMT technology [6]. Table III lists some key power parameters. The performance could be improved further with 5V Vcc.

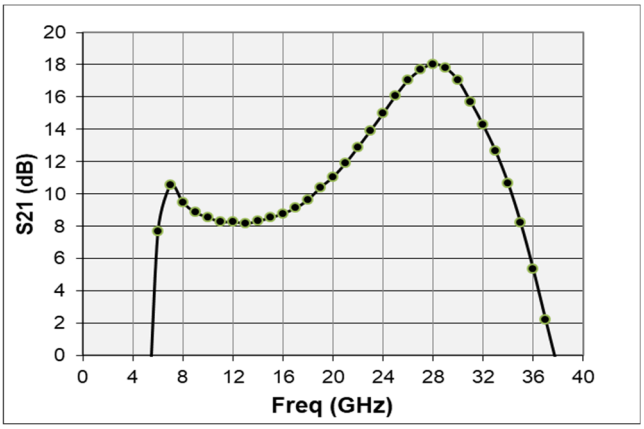

Fig. 8. S21 vs frequency of a two stage PA.

TABLE III
SUMMARY OF 28GHZ PA PERFORMANCE

Measured Parameters	Unit	Value
Operating Power Supply Range	V	2.9-3.5
Supply Current at Psat	mA	245
Freq Range	GHz	27.5-28.35
Gain S21	dB	18
P1dB	dBm	24
Psat	dBm	26
PAE at Psat	%	54

From the above DC, RF, and power performances, we have demonstrated that InP DHBTs with emitter dimensions greater than one micron is sufficient for Ka-band PA applications. The process is not only much easier than 0.15µm pHEMT technology but its PA performance is better than that of pHEMTs as well.

CONCLUSIONS

In summary, we have demonstrated that the collector transition layer design plays an important role in InP DHBT breakdown behavior. An abrupt breakdown characteristic, BVceo of 11V, and low knee voltage are obtained with a proper collector transition layer design. The DHBTs with emitter dimensions greater than 1 µm can yield *fmax* of 150GHz which is much easy to manufacture than 0.15µm pHEMT processes. We have demonstrated good power performance of MMIC PA at 28GHz.

ACKNOWLEDGEMENTS

The Authors wish to thank GCS manufacture group for supporting the device fabrication and testing, and the CAD group for the chip layout.

REFERENCES

[1]. V. Midili, et al, "InP DHBT technology for power amplifiers at mm-wave frequencies," Microelectronics Journal Volume 67, September 2017, p.111-119

[2]. T. Quach, et al, "Ultra-Efficient X-Band and linear-efficient Ka-band power amplifiers using InP DHBTs." 2001 International Conference on InP and Related Materials, Nara, Japan, May 14-18, 2001.

[3]. K. Kurishima, et al., "Fabrication and Characterization of High-Performance InP/InGaAs Double-Heterojunction Bipolar Transistors," IEEE Transactions on Electron Devices, Volume: 41 , Issue: 8 , Aug 1994, p.1319-1325

[4]. D. Caffin, et al, "Base-collector leakage current in InP/GaAs double heterojunction bipolar transistors." IEEE Transactions on Electron Devices, Volume: 44 , Issue: 6 , 1997, p.930-936

[5] N. Rostomyan et el., "28 GHz Doherty Power Amplifier in CMOS SOI With 28% Back-Off PAE." IEEE Microwave and Wireless Components Letters, Volume: 28 , Issue: 5 , May 2018, p.446-448

[6] K. Wang et el, "A K-band power amplifier in a 0.15-um GaAs pHEMT process", 2018 IEEE MTT-S International Wireless Symposium (IWS), 6-10 May 2018

ACRONYMS

DHBT: Double Heterojunction Bipolar Transistor
PA: Power Amplifier
f_T : Cut off frequency
fmax: Maximum oscillation frequency
P1dB: Output at 1dB compression
Psat: Saturation output power
PAE: Power Added Efficiency
HEMT: High Electron Mobility Transistor
Jc: Collector current density
MIM: Metal-Insulator-Metal
MMIC: Monolithic Microwave Integrated Circuit