Technology and future perspectives of III-V devices

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Abstract

Compound semiconductors are slowly but steadily penetrating the existing Si discrete device markets with predominant performance. SiC MOSFETs rather than Si IGBTs are adopted in EV inverters, and GaN switches become one of the best choices for low power charger applications. Similar trends are observed in other areas such as RF, displays, and sensors. We believe compound semiconductors would play one of the most important roles in the future of ESG. In this paper, we would like to introduce our optical and electrical III-V device projects and to present future prospective to be adopted in major markets.

III-V RESEARCH AT SAIT

In the past, compound semiconductors took a negligible portion of semiconductor market that is dominated by Si devices. Recently, due to the significant improvement in the performance and reliability, it becomes one of the key components for the future electrical systems. Our research topics are mainly related to the future technologies that can contribute to the next generation electrical systems with efficient and cost-effective approaches. Compound semiconductor projects correspond to our purposes to develop devices/processes to save energy consumption and conserve environment. The following sessions introduce the activities related to compound semiconductors at SAIT, R&D hub of Samsung Electronics.

GAN POWER DEVICES

Travel adaptors utilizing GaN's efficient power conversion can be easily found in the market, and more adoptions in data center and automotive applications are on the way. Every application with power conversion could take advantage of GaN's superior performance, though they have to pass stringent reliability standard. Samsung Electronics has also released a 65W fast charger and plans to adopt more compound semiconductors to commercial products such as large TVs, air conditioners, refrigerators, washer/dryer, etc.

We have been developing several GaN processes for more than a decade and preparing for foundry services to the customers. 650V pGaN gate e-mode process [1] became one of our main products, and other processes such as MIS HEMT, low voltage, RF, sensor processes are also in interest. We have been going through many obstacles such as wafer crack/bowing, dynamic on-resistance (D-Ron), and reliability of the gate and buffer, etc. Now, we are very close to release a commercial process, though there are still a few more hurdles to overcome. Our recent progress showed a significantly improvement in the robustness of our devices. The Ron shift after HTRB becomes negligible, and the package devices endure multiple short circuit stresses, which is the best among the reported devices. [2,3] Application tests were also performed to verify the performance and reliability of our GaN processes.

These days, making a working GaN HEMT device is not difficult due to the cumulative experience on CMOS compatible GaN HEMT processes. However, to be adopted in the commercial market, the process/device should be reliable and economically reasonable enough to satisfy customers, which are final goals of our GaN projects.

To improve the reliability of a new device from the materials with unexpected properties such as GaN epi layers on a Si substrate, it is important to design evaluation methods carefully. Especially when the material includes unacceptable defect density, more attention should be given to exclude noise. We have been developing proper methods to evaluate the real performance of GaN HEMT devices and figured out how to prepare for the reliability assessment. As GaN's bandgap is much wider than that of Si, the lifetime of GaN devices should be longer than Si devices. The standard reliability evaluation procedures developed for Si devices could not directly apply to GaN devices. This is because GaN on Si HEMT system is a lot more complicated, and there is no HEMT structure in Si power devices. There are several reports mentioned abnormal reliability behaviors. For example, the low temperature degradation is faster than high temperature, which is different from Si's lifetime expectation calculation. [4,5] Our method makes the feedback from the reliability assessment to revise the epi structure and process conditions valid and keeps our development on track.

Fig. 1 shows one of our HTRB test results. The D-Ron shift versus drain stress voltage up to 1.2kV is presented. Even if the device was developed for 650V rating, we could check the D-Ron up to 1.2kV. The measured D-Ron across 200mm wafer was up to 5% and 15% at 650V and 1.2kV

respectively. After 900V HTRB for 60hrs which is an accelerated condition for 650V rated devices, the Ron shift was less than 20%. When a high voltage was applied after HTRB, less than 8% of Ron shift was observed, and the D-Ron becomes lower than the static Ron. This is one of the advanced features of our process, and it makes our devices performance more reliable during switching. The drain leakage up to 1.2kV is also presented. Further improvements are ongoing to lower the Ron shift.

To reduce the cost of the devices, we have been using 200mm wafers and trying to reduce the die area as small as possible without sacrificing the performance, reliability, and yield. The first and most important piece to shrink the die size is the distance between gate and drain (Lgd). Shorter Lgd means lower Ron and smaller die area. However, as shown in Fig. 1, the Ron degradation and the reliability of the device becomes worse for shorter Lgd, which is a trade-off of shrinking dimensions. As actual Ron of shorter Lgd devices is still lower, if they pass other reliability assessment, it can be applied to a released process. We are investigating how much we can shrink the Lgd and other regions. Reducing dimensions looks a simple work. However, there are a lot of trade-offs, and enormous effort to optimize epi layers, processes, and device designs are required.

HEMT structures are known to be vulnerable to short circuit condition compared to commercial Si Power MOSFET. Even a 10us of high voltage/current pulse could easily destroy the device. To overcome this deficiency, epi layers, processes, and device designs were optimized through multiple cycle of learning. Finally, our devices could withstand 100 times of 10us short circuit pulses. (Fig. 2) As a typical short circuit test is performed with a packaged device, it takes long time to evaluate a new device. We could manage to shorten the learning cycle time significantly by measuring the spatiotemporal change of the potential inside of GaN HEMT devices on wafer. The correlation between the wafer level measured results and the short circuit capability let us estimate the robustness of the packaged devices. [6]

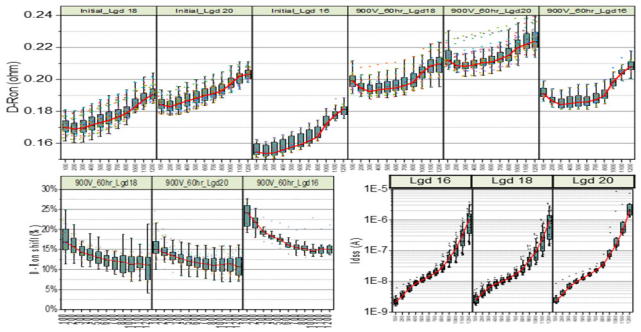

Fig. 1 D-Ron before and after 900V/60hr HTRB. The gate to drain distances (Lgd) are 16um, 18um, and 20um. Lgd 20um devices showed slightly lower shift compare with Lgd 18um devices. The Ron shift of Lgd 16um device was highest. The drain leakage currents (Idss) of both are similar, as most drain leakages flow to the buffer.

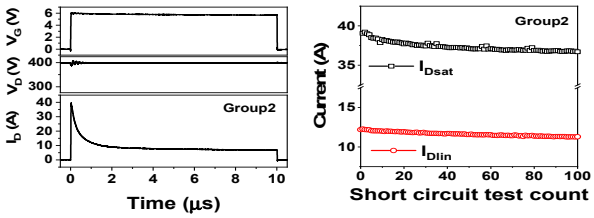

Fig. 2 Single and repeated short circuit capability test of the packaged devices. No failure was observed during the short circuit test for up to 10 µs and the device could withstand 100 consecutive short circuit tests. After completing tests, 6 % of I_{Dsat} and 7 % of I_{Dlin} degradation observed.

We have also evaluated our devices under actual application setup. After checking the switching behavior of the devices under repeated switching using a modified double pulse setup, the packaged devices were installed in passive and active clamp circuits shown in Fig 4. The repeated double pulse test at an elevated temperature showed no degradation on the D-Ron under a hard switching environment. (Fig. 3) The measured efficiencies of the flyback converters were competitive to commercial devices with similar Ron. (Fig. 4)

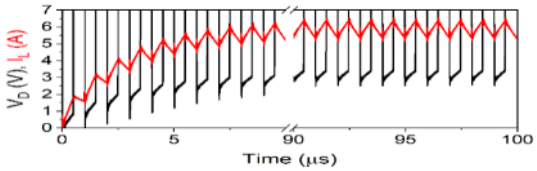

Fig. 3 Multi pulse D-Ron test result at 150°C. Approximately 10% of D-Ron increase was observed after switching 100 times at 1 MHz with a 50% duty cycle.

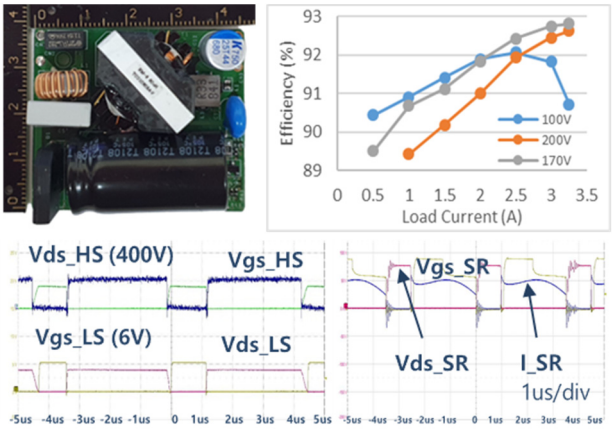

Fig. 4 65W Active Clamp flyback converter evaluation board using GaN device and efficiency versus load current. Waveforms of the clamp and main FETs and secondary synchronous rectifier. 92% of the maximum efficiency for 220Vac input achieved. 100Vac input showed a degradation at high power due to non-optimized package.

We believe that GaN adoption would be extended to higher power and more profitable applications such as data center, renewable energy, and EV applications. To win the

battle with Si and SiC Power MOSFETs, new generation GaN devices should maximize their advantages such as low loss switching and resolve drawbacks. Monolithic integration could be one of the best approaches to maintain switching speed. Low input/output capacitance and robust gate design/processes are also helpful to reduce the switching losses. One of the main downsides of GaN HEMT device is its poor thermal performance. To compete with SiC, there should be a way to improve the thermal conductance and lower Ron increase over elevated temperatures. A special package such as embedded package or flip chip package could improve some of the thermal performances. As a foundry service provider, we are investigating various candidates to enhance the performance and reliability of GaN HEMT processes. These efforts include new device structures, material engineering, and process development.

HIGH PPI U-LEDs FOR AR GLASS

Due to the inherent high efficiency, brightness, and stability, inorganic Group III–V microLEDs (μLEDs) are being evaluated as next-generation displays for a wide variety of applications [7]. The 'pixelation' here refers to forming an array of light emitters (pixels) distinctively controlled without a crosstalk between neighbors. Mesa etching, which physically removes p-GaN and multiple quantum wells (MQWs) to make electrical contacts to the n-GaN surface, has long been used for single LED devices and is regarded as a common pixelation technique for next-generation μLEDs. However, non-optimized mesa etch process damages the surface of the active region and leads to too much non-radiative surface recombination with decreasing pixel size (< 10 μm), thus significantly reducing the efficiency. To reduce the surface recombination, surface passivation techniques or core-shell structures must be used. Moreover, an integration into driving pixel thin-film transistors (TFTs) is difficult due to three-dimensional (3D) geometry-related process issues, such as poor step coverage. Therefore, a new pixelation strategy is required to achieve high efficiency of submicron-scale devices and easy integration into pixel-driving circuitry. Herein, we report utilizing tailored ion implantation (TIIP) to fabricate highly-efficient, electrically-driven pixelated InGaN μLEDs at mid-submicron scale (line/space of 0.5/0.5 μm), corresponding to 8500ppi (RGB). Ion implantation (IIP) of a thin pixelation mask at ~100°C using heavy ionic species with tilt angle of 0° and low energy/dose was used to confirm the pixelation mechanism. Monolithic integrations of TIIP pixelation with low-temperature polysilicon (LTPS) pixel circuits applied to 2000-ppi (pentile) display prototypes and 5000-ppi compatible core technologies including quantum dot color converters (QD C/Cs) [8].

We investigated several TIIP conditions and pixel sizes using fluorescence photoluminescence (PL) microscopy TIIP spatially confining the implanted region precisely, with minimal lateral spreading. The thickness of the implantation mask is one of the most critical parameters for optimal TIIP. Using 0° tilt angle and heavier ions, including Ar^+ or Kr^+, is also beneficial. Minimal ion energy and dose should be used because high values degrade the pixelation contrast, and the ion energy is more influential than fluence. The excellence of TIIP pixelation was experimentally verified. A 200-nm-thick Ti mask is formed under the TIIP with Ar^+ implantation at 100°C, tilt angle of 0°, energy of 5 keV, and dose of 2×10^{12} cm^{-2}. PL microscope images of the subpixels with various pixel densities (300-8500 ppi) are presented in Fig 5.

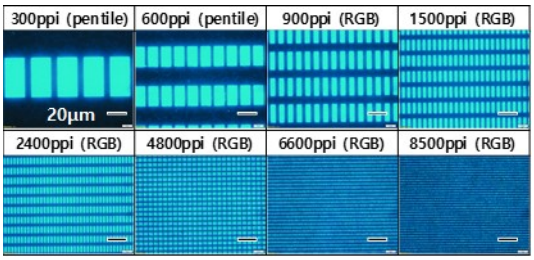

Fig.5 PL microscopy images of eight different InGaN subpixels by ion implantation from 300 to 8,500 ppi (RGB).

Owing to the planar geometry, TIIP pixelation is readily incorporated via monolithic or bonding integration into any high-resolution pixel-driving circuits in high-ppi μLED displays. For example, 2-transistor/1-capacitor (2T1C) pixel circuits based on LTPS are fabricated monolithically on the TIIP/charge-blocking layer (CBL) structure. Fig. 6 (a) and (b) present TIIP/CBL-pixelated LEDs operated by 300/600/2000 ppi LTPS-TFTs. The 2000 ppi (pentile) LTPS-TFTs have width/length (W/L) of 2 μm/2 μm. Furthermore, we verified the transfer characteristics of p-Si TFT even at W/L of 1 μm/1 μm, which corresponds to 4,000 ppi (pentile) pixel circuits. Finally, the TIIP/CBL LEDs are readily assembled with a QD color converter (C/C) pattern. For example, we applied QD C/C for 300-ppi RGB displays (Figs. 6c). Furthermore, we are developing a backside-exposure technique for high-resolution patterning of QD C/C, which is essential for full-color micro displays in AR glasses. The backside-exposed QD layer begins crosslinking from the bottom side, which enables fine patterning with controlled PR thickness.

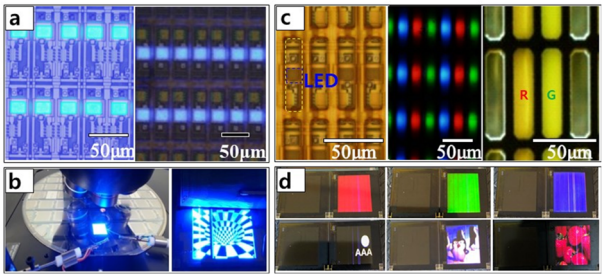

Fig.6 Monolithic integration of TIIP-pixelated LEDs with TFTs and QDs. (a) TFT-driven microscopic EL pixel images and (b) Moving EL pixel images. (c) QD integration of barrier rib onto 300 ppi (RGB) LEDs (top left), QD C/C (top center and right) and corresponding full-color images including R, G, B, BW and moving images (bottom).

MICROLED TRANSFER

One of the most difficult processes of manufacturing uLED displays is transferring millions of μLED chips to a display panel. The chips have to be picked-up and precisely placed on the panel substrate with virtually no error. However, conventional pick-and-place type mass transfer methods have not been able to fulfill the requirements, even though the technologies have been significantly improved in recent years. Moreover, it would be a critical issue whether current transfer methods can be adopted to 8K or 16K resolution TV with smaller μLED chips in the future.

To overcome aforementioned difficulties of μLED transfer methods, several groups have reported newly developed suspension-based transfer methods of μLED chips. [9-13] The proposed methods using randomly suspended μLED chips in fluidic environment achieve high transfer yield and acceptable processing time regardless of the number of μLED chips. Due to random mixing of the μLED chips, an improved color quality of panel can be attained naturally even though epi-grown wafer has the wavelength difference.

Fig. 7 shows a comparison of three groups with different fluidic transfer techniques corresponding to particular chip designs. The transfer methods are strongly related to the unique chip design with different kinds of external force.

Fig.7 (a) is an electric-field assisted transfer method by rearranging nanorod LEDs with 2.5um length and 0.5um diameter. When nanorods are dropped on the sub-pixel position between two metal electrodes, they are horizontally assembled in one direction by the external DC/AC field. A large-area panel can be adopted by using an accurate and fast dotting method such as inkjet printing. In addition, a cost reduction due to the adoption of small size chips can be expected. However, the reduced efficiency due to downsizing chip becomes a crucial factor to overcome. [14]

In the case of eLux in Fig.7 (b), a leading company in FSA transfer technology, they attempted to align the chips by creating asymmetric structures on the backside of the chips. A handle-shaped artificial structure 'post' was attached to the opposite side of the electrode surface, and then the chips are settled down in the bank structures so as to electrode-face of μLED downward on the electrode surface in accordance with the internal flow. They reported that 100% orientation control of chips are possible, and the assembly yields are 99.95%/100% at 15min./30min., respectively. However, as the external force could not bring the chips directly to the individual subpixel location, the assembly yield would be an important issue.

In Fig.7 (c), the micro-LEDs are transported into the hole-patterns provided in the interposer by using a magnetic field. At first, magnetic materials are deposited on μLED electrodes to attract the chips into the holes, and the chip shape is specially designed to make chip to be aligned metal-up face. When the chips approach closely to the patterned mold through the lower chip tray equipment, the magnetic field from the backside of the interposer pulls μLED chips to be aligned metal-up face into the hole patterns. Unlike eLux's method, the external force by magnetic field directly acts on whole patterns of interposer, which has high probability to fill up the holes with chips. The chip align mechanism related to the chip design and the fixing method after chips transferring into the interposer are important. Although no specific details are known about this method, limited results are expected through the published patents.

Recently, we have discovered and demonstrated a fluidic based transfer method differentiated form the methods mentioned above. We hope to introduce our transfer method with good results soon.

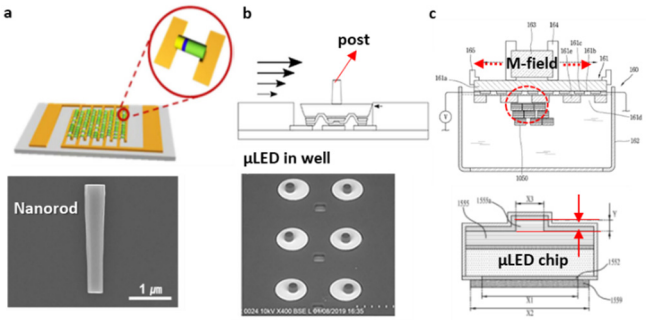

FIG. 7 Comparison of fluidic-based μLED transfer methods. The specifically designed μLED are rearranged by external force: (a) electric field (b) lamina flow (c) magnetic field

CONCLUSIONS

Electrical and optical compound Semiconductor projects at SAIT are introduced. GaN power devices would be adopted to new markets and compete with SiC. If a new generation to overcome a few drawbacks, it can be one of the most important power switching devices. uLEDs using IIP enables shrinking of pixel size and monolithically integrating circuits. Fluidic based uLED transfer method improve yield and lower the manufacturing cost of QLED displays.

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