Optimization of GaN RF Switch Device Performance using AFRL GaN 140 nm MMIC Process

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Abstract

Gallium nitride (GaN) RF switches in this report have been evaluated to achieve a high switch cutoff frequency figure of merit (FOM) $f_c = (2\pi R_{on}C_{off})^{-1}$ exceeding 600 GHz by considering a range of device layouts and topologies to minimize on-resistance R_{on} and off-capacitance C_{off}. These RF switch devices were manufactured within a process flow that is compatible with the production of AlGaN/GaN high electron mobility power amplifiers. This optimization was achieved by varying factors including compound gates, W/SiO_2 low conductivity layer (LCL), source-drain spacing L_{sd}, and contact length L_c. Analysis of DC, RF and power handling data confirm levels of influence for these factors.

Introduction

Active devices in GaN monolithic microwave integrated circuit (MMIC) process development kits (PDK) are high-electron mobility transistor (HEMT) cells that deliver high RF power density at microwave frequencies. GaN HEMTs can also be configured as switches to re-route RF signals with low-loss, high-speed and high-power handling properties with simple voltage control. These RF switches are essential for many wireless communications systems and radar applications [1]. However, monolithically integrating GaN RF switches is generally limited to standard process layers necessary to fabricate the HEMT for the power amplifier and associated passives with little optimization to realize a high-performance RF switch FOM.

This work intends to experimentally determine the highest performing GaN HEMT RF switch device topology through a design of experiments (DOE) using the Air Force Research Laboratory (AFRL) GaN 140 nm gate length MMIC process by reducing the off-state capacitance (C_{off}) while maintaining low on-state resistance (R_{on}). The switches in this DOE have a modified gate length L_g of 340 nm. The RF switch FOM characterizes the suitability of a transistor for routing RF energy by its cutoff frequency $f_c = (2\pi R_{on}C_{off})^{-1}$ where R_{on} is the resistance between input and output terminals in the "on" state, and C_{off} is the capacitance between these terminals in the "off" state. A high f_c is achieved by reducing R_{on} and C_{off} to minimize the product of these two factors.

Independent variables for this optimization include device geometries of contact length (L_c) and source-drain channel length (L_{sd}). The use of a low conductivity layer (LCL) [2] and compound gating [3] (multiple gates in the channel) with devices that have 1, 2, 3 or 4 planar I-gates in the channel are additional strategies that were investigated for reducing C_{off}. A room-temperature co-sputtered W/SiO_2 LCL with sheet resistance R_{sh} ~ 90 MΩ/□ spans the full length of the channel, as shown in Device Types B, D, and E in Figure 1. The low conductivity W/SiO_2 has a high RC time constant, preventing the layer from following an RF signal. The layer properties are fast enough to follow the DC control signal and allow the device to deplete the access regions in the off state. These approaches for minimizing C_{off} are extrinsic to GaN HEMTs and may be applicable to other FET-based MMIC processes.

Fabrication and Test

Coplanar waveguide GaN HEMT devices with 4x100 µm gate width were fabricated on two wafers through silicon nitride (Si_3N_4) passivation and interconnect metal with L_c dimensions ranging from 0.5 µm to 15 µm and L_{sd} dimensions ranging from 1.3 µm to 3 µm. Ohmic contacts were annealed at 850 °C. The effectiveness of the LCL for improving the RF switch FOM is determined by comparing R_{on} and C_{off} across 5 different device

layouts as shown in Figure 1: **A)** baseline metal-semiconductor HEMT (MESHEMT), **B)** MESHEMT with Al_2O_3/LCL on top of the device, **C)** baseline HEMT with Al_2O_3 gate insulator (MISHEMT), **D)** MISHEMT with Al_2O_3/LCL gate insulator, and **E)** MISHEMT with Al_2O_3 gate insulator and LCL on top of the gate.

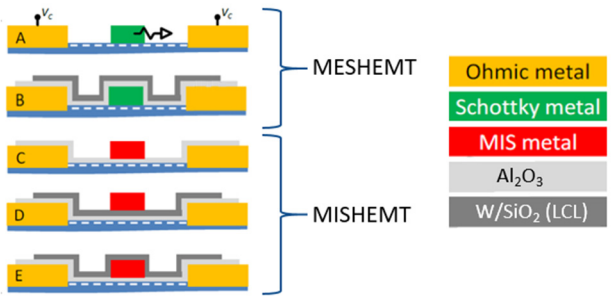

Fig. 1. Five device type topologies were evaluated for optimizing f_c. Devices are passivated with Si_3N_4.

After MMIC fabrication, common-gate S-parameter measurements were captured up to 10 GHz, with gate bias conditions ranging from -20 V for the off state to +2 V for the on state. After recording DC measurements, sites that had the best RF performance were selected for power handling tests. JMP statistical analysis software was used to format and compile the data for all bias conditions, followed by calculations of R_{on}, C_{off}, and f_c from the S-parameters across frequency for each site.

Data Analysis

A series-impedance s-parameter model, $S_{21} = 2Z_0/(2Z_0 + Z)$, was used to curve fit on-state and off-state data. Z is modeled as a resistor for on-state conditions ($V_{gs} \geq 0$ V) and a capacitor for off-state conditions ($V_{gs} \leq -15$ V). R_{on} and C_{off} calculations from the S_{21} data for each site are fit to the model and an R^2 fitting parameter is used to screen data in JMP according to $R^2 > 0.9$ or higher. Filtering data by a higher R^2 only includes data points in the analysis that have a closer match to the series impedance model.

Data analysis identified trends in factors to yield the highest f_c through low R_{on} and C_{off}. Device types A and B MESHEMT switches shown in Figure 2 have a median R_{on} value 42% lower than the MISHEMT switches, with R^2 fit > 0.999. MISHEMT Device types C, D and E do not show a statistically significant improvement in C_{off} over the MESHEMT switches A and B.

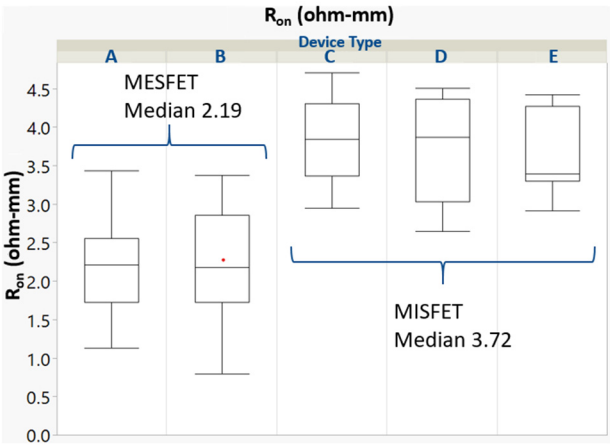

Fig. 2. MESHEMT R_{on} median of 2.19 ohm-mm is 42% lower than MISHEMT R_{on} median of 3.72 ohm-mm for devices with L_c (µm) = 5, 10, 15, L_{sd} (µm) = 1.6, 2, 3, number of gates = 1, 2, 3, 4 at V_{gs} = 1V. R^2 fit > 0.999.

Figure 3 shows the 52% lower median value for C_{off} with W/SiO_2 LCL for single-gate switches compared to the baseline MESHEMT. Compound gating (2, 3 or 4 gates in the channel) did not show statistically significant advantages in R_{on} or C_{off} for MESHEMT devices with LCL.

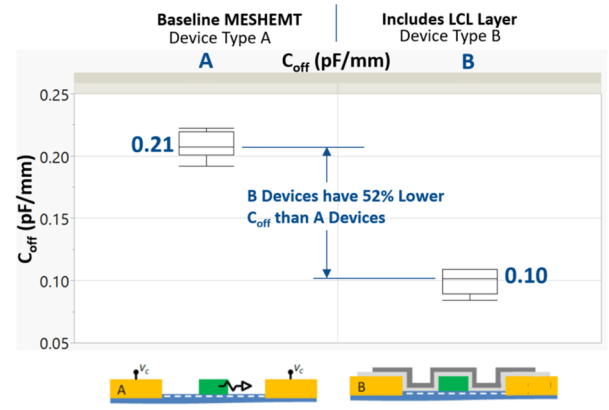

Fig. 3. Median quartile box plot shows that the LCL improves off-state capacitance by 52% for single-gate devices.

Trends for L_c are shown in Figure 4: Shorter L_c has higher R_{on} for $L_c < 5$ µm, although longer L_c has higher C_{off}. Highest f_c is achieved with L_c of 5 µm for the switches in this work.

R_{on} was expected to improve with shorter L_{sd}, and the data confirm this trend. 1.3 µm is the shortest L_{sd} in this DOE, however the yield for this dimension is low and 1.6 µm is considered the best result when accounting for the tradeoff between yield and performance.

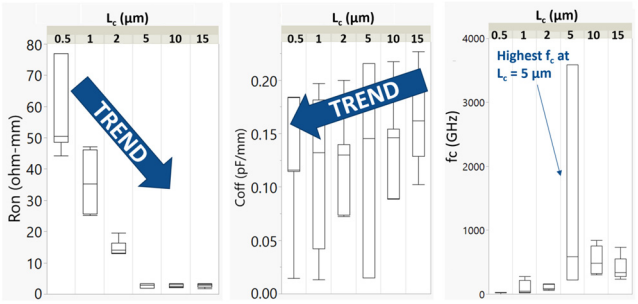

Fig. 4. On-resistance improves with longer contact length L_c (left), whereas off-capacitance improves with shorter L_c (center). The optimized contact length for high cutoff frequency fc is 5 µm (right). Device type B, L_{sd} = 3 µm, number of gates = 1, 2, 3, 4. $R^2 > 0.999$.

I_{ds} vs V_{ds} is shown in Figure 5 for V_{gs} in the on state at +1 V. R_{on} is calculated from the DC data by taking the slope of the I_{ds} vs V_{ds} curve in the linear region at low V_{ds}, and this R_{on} calculation confirms the same trend that the RF data concluded for single-gate MESHEMT devices with LCL, with R_{on} values of approximately 3 ohm-mm.

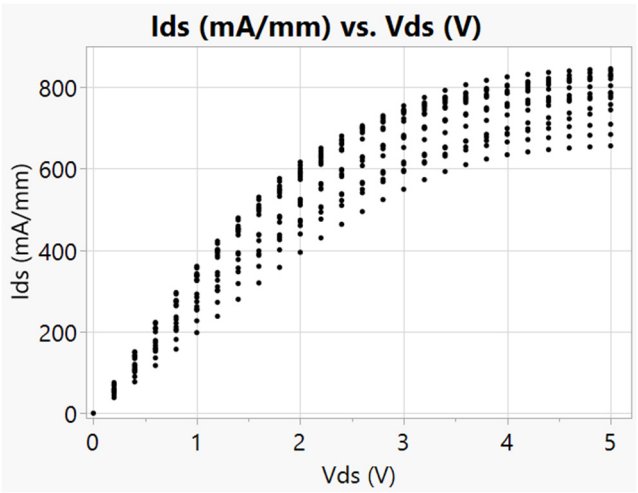

Fig. 5. I_{ds} vs V_{ds} transfer curves from DC data of Device Type B MESHEMTs, 12 sites. V_{gs} = +1 V for sites with L_{sd} = 3 µm, L_c = 5, 10 and 15 µm.

Sites with optimized f_c conditions for 4x100 µm single-gate MESHEMT devices with LCL and L_c = 5 µm and 10 µm were selected for power handling.

Figure 6 shows output power measuring greater than 5W (37 dBm) for power sweeps up to 1 dB compression. Insertion loss (IL) in Figure 7 for 4 sites measured at V_{gs} = 0 V is approximately 0.6 dB, with no significant IL correlations within the range of L_c = 5, 10, 15 µm or L_{sd} = 1.6, 3 µm. Isolation was measured in the off state at V_{gs} = -20 V, ranging from 10.5 to 12.6 dB.

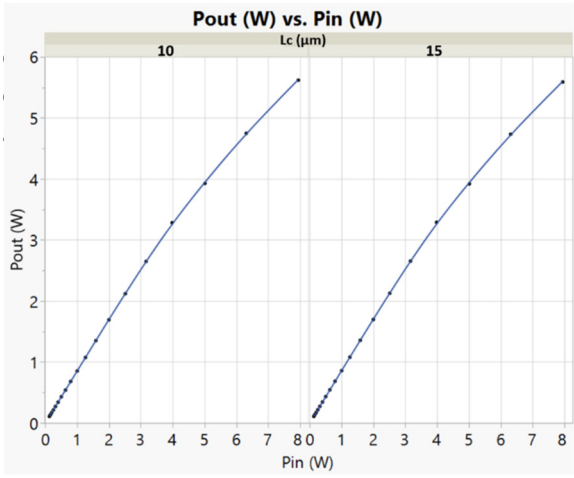

Fig. 6. Output power for two single-gate device type B MESHEMT sites with LCL, sweeping input power up to 1 dB compression.

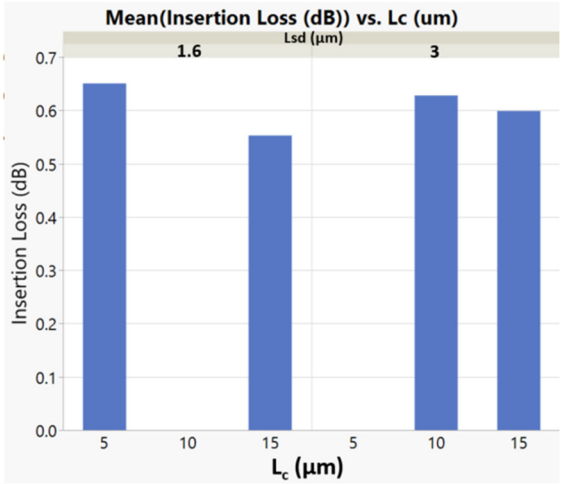

Fig. 7. Switch insertion loss for a variety of L_c contact lengths and source/drain spacing L_{sd}.

Results of the f_c calculation are shown in Figure 8 for optimized topology device type B (MESHEMT with LCL), optimized number of gates (1), and optimized contact pad length (5 µm). R_{on} V_{gs} = 1 V, C_{off} V_{gs} = -15 V, and R^2 data fit > 0.9. Source-drain spacing L_{sd} values of 1.6, 2 and 3 µm are all included to have a meaningful number of data points instead of including only the optimized L_{sd} of 1.6 µm. The median f_c value is 637 GHz, with some sites exceeding 1 THz. Switches made with our standard 140 nm T-gate have an f_c of around 300 GHz or lower. Single-gate switches without LCL in this

work with a gate length of 340 nm have an f_c of around 350 GHz. Switches without LCL from other groups include f_c of around 400 GHz at -20 V for off-state bias [4].

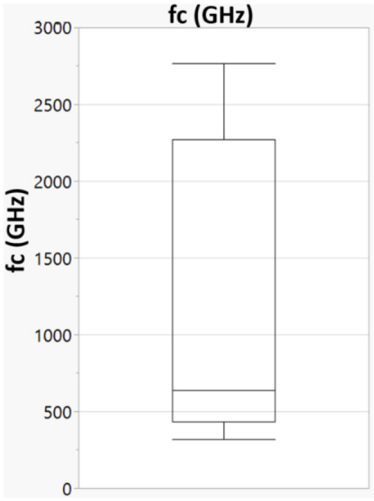

Fig. 8. f_c calculation results for optimized number of gates (1), optimized topology (device type B, MESHEMT with LCL), optimized number of gates (1), and optimized L_c (5 µm). R_{on} at V_{gs} = 1 V, C_{off} at Vgs = -15 V, L_{sd} = 1.6, 2 and 3 µm. $R^2 > 0.9$.

CONCLUSIONS

A variety of factors were considered in order to achieve a high RF switch cutoff frequency f_c, including L_c, L_{sd}, number of gates, and several device types that implemented a low conductivity layer. The data analysis revealed optimization trends to identify the best combination of these factors to optimize an RF switch for high f_c fabricated with a process that is compatible with production of AlGaN/GaN high electron mobility power amplifiers.

Contact length was optimized at L_c = 5 µm due to competing trends of lower R_{on} with higher L_c and lower C_{off} with lower L_c. The optimization of L_{sd} = 1.6 µm was based on lower R_{on} with shorter L_{sd}, and taking into account lower yield for devices with L_{sd} of 1.3 µm. The combination of single-gate MESHEMT devices with LCL have the highest f_c out of all device types that were studied in this work.

REFERENCES

[1] A. Koudymov et al., *Monolithically integrated high-power broad-band RF switch based on III-N insulated gate transistors*, IEEE Microwave and Wireless Components Letters, vol. 14, no. 12, pp. 560-562, Dec. 2004

[2] A. K. Sattu, et al., *Small- and Large-Signal Performance of III-Nitride RF Switches With Hybrid Fast/Slow Gate Design*, IEEE Microwave and Wireless Components Letters, vol. 21, no. 6, pp. 305-307, June 2011

[3] McGrath, F. (Lowell Operations, MA, USA), et al., Novel high performance SPDT power switches using multi-gate FET's, IEEE MTT-S International Microwave Symposium Digest, v 2, p 839-842, 1991

[4] C. F. Campbell and D. C. Dumka, "Wideband high power GaN on SiC SPDT switch MMICs," *2010 IEEE MTT-S International Microwave Symposium*, pp. 145-148, 2010

ACRONYMS

C_{off}: Off-state capacitance
f_c: cutoff frequency $f_c = (2\pi R_{on} C_{off})^{-1}$
HEMT: High electron mobility transistor
L_c: Contact pad length
LCL: Low conductivity layer
L_g: Gate length
L_{sd}: Source – drain spacing
MESHEMT: Metal semiconductor HEMT
MISHEMT: Metal insulator semiconductor HEMT
R_{on}: On-state resistance