Propelling the Power Electronics Revolution: 200 mm Diameter, 100 V to 1800 V and Beyond GaN-on-QST® High Volume Device Manufacturing Platform

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Abstract

The CMOS fab-friendly and SEMI standard thickness 200 mm QST® (QROMIS Substrate Technology) substrates enable fabrication of long awaited commercial high-performance GaN power devices with breakdown voltages ranging from 100 V to 1800 V. This is achieved by utilizing a substrate core with the coefficient of thermal expansion (CTE) matched to GaN over a wide temperature range as well as with its high thermal conductivity and high mechanical strength, breakage-free fully integrated QST® substrates. In this work, results from the production of 200 mm SEMI standard thickness QST®-based 650 V E-mode HEMT devices on a commercial, high volume CMOS foundry manufacturing platform are presented. Also, the development work in 200 mm CMOS fabs for high-quality, high-breakdown voltage (up to 1800 V) and crack-free p-GaN HEMT epitaxial layers, 100 V to 1200 V E-mode HEMTs, wafer-level monolithically integrated circuits (ICs) and semi-vertical / vertical power devices on QST® substrates are presented.

Introduction

In recent years, GaN has become a forefront wide bandgap semiconductor material for next-generation, energy-efficient power electronics. With its higher breakdown strength, faster switching speed and lower on-resistance, GaN power devices can convert power far more efficiently than Si-based devices. While its performance is commercially demonstrated, widespread GaN adoption requires a scalable and high-yielding manufacturable technology platform enabling economies of scale and a full spectrum of low-cost products such as lateral and vertical power switches extending from 100 V to 1800 V and beyond, wafer-level monolithic ICs and rectifiers.

To further scale up both the substrate size and GaN stack thickness and also to achieve wafer-level monolithic ICs of the current 150 mm, 650V GaN-on-Si manufacturing platform, even with non-SEMI standard substrate thickness (1 mm or thicker), is extremely challenging, due to the significant mismatch in thermal expansion coefficient between GaN and Si, and the IC device cross-talk challenges arising from the conducting Si substrates.

A disruptive commercial solution enabling high volume, wafer breakage-free, low cost and scalable GaN device manufacturing is the CMOS fab-friendly and SEMI standard thickness engineered substrate called "QST®" (QROMIS Substrate Technology) with a core material having a thermal expansion that very closely matches the thermal expansion of the GaN/AlGaN epitaxial layers [1-3]. Commercial QST® substrates, available from QROMIS Inc. and Shin-Etsu Chemical Co. Ltd., enable wafer breakage-free high-volume manufacturing of 200 mm GaN device wafers (scalable to 300 mm), covering all GaN applications including 100 V to 1800 V high performance discrete and wafer-level monolithic IC power devices, RF devices, and display microLEDs.

The QST® substrate consists of a polycrystalline ceramic core (poly-AlN), covered by several encapsulation layers, on top of which is a SiO_2 bonding layer and a single crystalline Si layer which serves as the nucleation layer for the epitaxial GaN growth (Fig. 1).

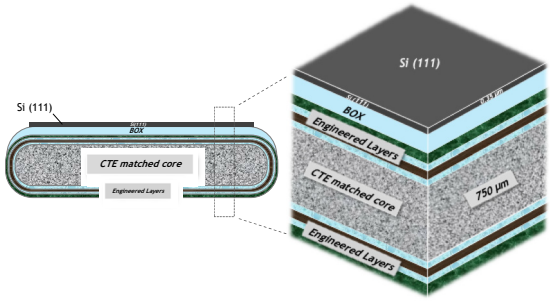

Fig. 1. Cross-section of a commercial QST® substrate.

As the QST® substrates are thermally matched to GaN, thick, high-quality GaN device layers with relatively low defect density, high crystal quality, and low wafer bow can be achieved at SEMI standard thicknesses (Fig. 2) [4]. Moreover, QST® substrates open perspectives for very thick GaN buffers, including realization of

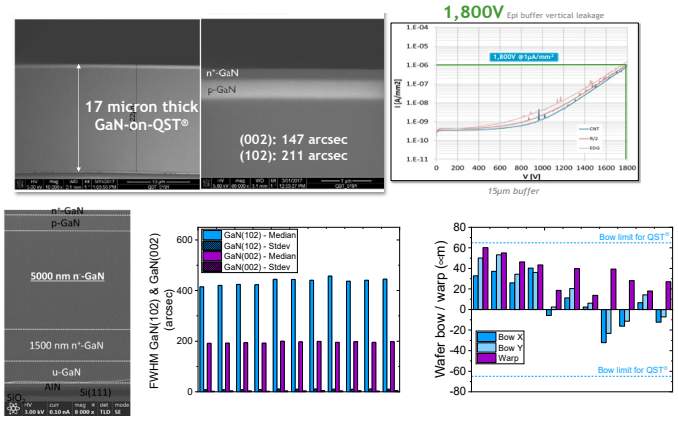

Fig. 2. SEM cross-section of 17 µm GaN epitaxy and I-V characteristics of 15 µm GaN epitaxy buffer layers on 150 mm QST® substrates rated for 1800 V devices. Crystal quality and wafer shape for >8 µm GaN epitaxy stack on 200 mm QST® substrates using a 5 µm thick drift layer for semi-vertical / vertical devices.

free-standing and very low dislocation density GaN substrates by >100 µm thick fast-growth epitaxial layers. These unique features will enable long awaited scalable commercial GaN power switches and rectifiers suitable for high voltage and high current applications presently dominated by Si IGBTs and SiC power FETs and diodes.

In this work, the status updates on the following QST®-based GaN power device solutions will be presented: (1) results from the production of 200 mm SEMI standard thickness QST®-based 650 V E-mode HEMT devices on a commercial, high volume CMOS foundry manufacturing platform, (2) the development work on 1200 V E-Mode HEMT devices, (3) progress in the development of wafer-level monolithically integrated power ICs, and (4) the initial results from the demonstrations of semi-vertical / vertical power devices.

Results and Discussion

Production of 650 V E-mode GaN HEMT commercial devices on a CMOS foundry manufacturing platform

650 V E-mode GaN HEMT devices on 200 mm SEMI standard thickness QST® substrates is entering mass production led by Vanguard International Semiconductor (VIS). Fig. 3 shows the status of GaN-on-QST® manufacturing technology: two- and three-level metal layer devices architectures, typical output and transfer curves, as well as full set of reliability data, 1000 hr HTRB and HTGB, collected on packaged devices. VIS' GaN-on-QST® devices have been already tested for fast chargers and PFC applications and met all specifications. Example of 150 W PFC using GaN-on-QST® 650 V E-mode HEMT is presented in Fig. 4. As shown, power efficiency exceeds 96%. Manufacturing volume of GaN-on-QST® E-mode HEMT devices will ramp for 650V applications as the first step followed by 1200 V and monolithic ICs for improved functionality and new applications.

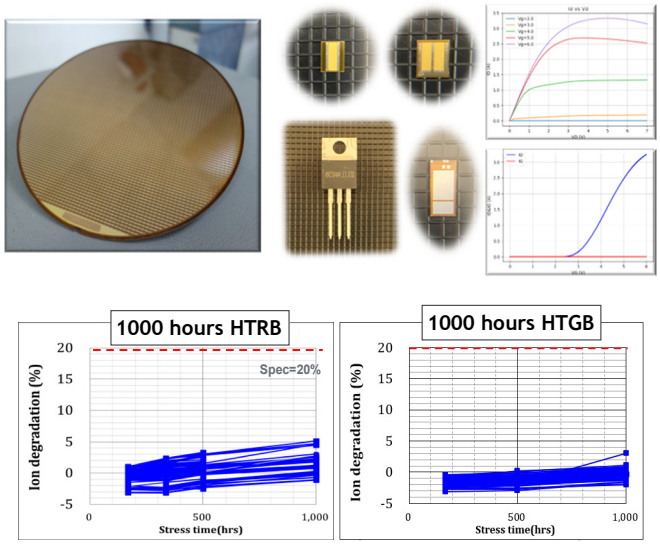

Fig. 3. 200 mm 650 V GaN-on-QST® E-mode HEMT device wafer image manufactured by VIS; 650V devices: bare chip and packaged variations with output and transfer curves of packaged 650 V devices; 1000 hr HTRB and HTGB reliability data for packaged devices.

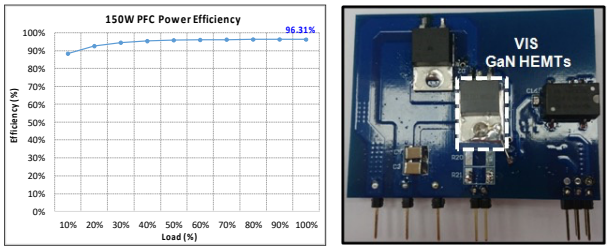

Fig. 4. High efficiency 150W PFC using 650 V E-mode HEMT devices on 200 mm QST® substrates manufactured by VIS.

1200 V E-mode GaN HEMT devices

For important applications beyond 650 V such as electric cars and renewable energy, it has become difficult to further increase the GaN buffer thickness for GaN-on-Si based solutions to the levels required for higher breakdown and low leakage levels, because of the mismatch in CTE between GaN/AlGaN epitaxial layers and silicon substrates. One can envisage to use thicker Si substrates for GaN-on-Si platform for 900V and 1200V applications, but experience has shown that for these higher voltage ranges, the mechanical strength is a major concern in high volume manufacturing which manifests itself as wafer breakage / cracking in GaN epitaxy layers and/or wafer shape issues, as well as compatibility issues in wafer handling in some processing tools. Carefully engineered QST® substrates are now enabling 1200 V buffers and beyond on a SEMI standard thickness 200 mm substrate which is scalable to 300 mm.

In this work, p-GaN gate E-mode HEMT devices with a gate-to-drain spacing of 16 µm were fabricated on 200 mm QST®, with a 7.2 µm-thick (Al)GaN epitaxial buffer stack grown by using the commercial, high volume capable AIXTRON G5+ C Planetary Reactor® [Fig. 5]. The off-state drain and gate leakage of the devices is shown to be well below 0.1 µA/mm and the transistors reach a voltage of 1200 V, as depicted in Fig. 6. The output and transfer characteristics show a low on-resistance of 13.9 Ω·mm for devices with an L_{GD} of 16 µm. A threshold voltage of 2.9 V is extracted at maximum transconductance.

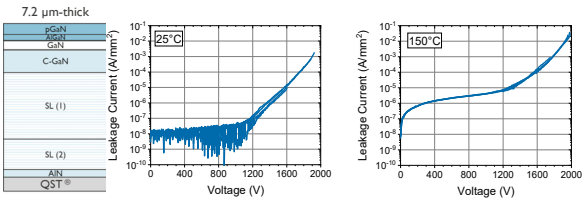

Fig. 5. Demonstration of (Al)GaN buffer epitaxial growth in commercial AIXTRON G5+ Planetary C reactor, qualified for 1200 V applications on 200 mm QST® substrates with a 7.2 µm thick stack.

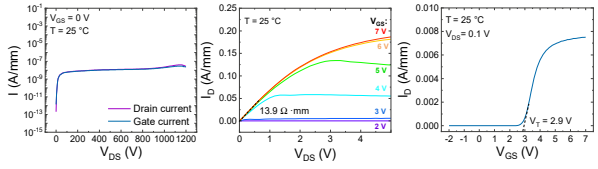

Fig. 6. Typical off-state leakage (V_{GS} = 0 V), output and transfer characteristics of the 1200 V p-GaN gate power HEMTs fabricated on 200 mm GaN-on-QST® substrates.

Additionally, Fig. 7 shows a snapshot of the 1200 V GaN-on-QST® HEMTs development results from a commercial, high volume 200 mm CMOS foundry manufacturing platform at VIS, with hard breakdown exceeding 2400 V.

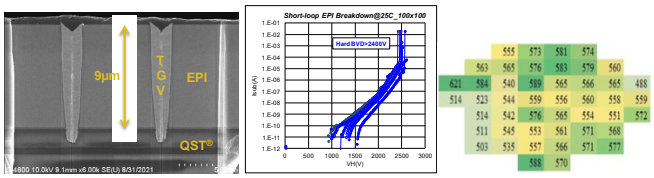

Fig. 7. 1200 V rated E-mode GaN HEMT epitaxy cross-section on 200 mm QST® with "Through GaN Vias" (TGV), and the corresponding leakage curves and the sheet resistance uniformity.

WAFER-LEVEL MONOLITHICALLY INTEGRATED GAN POWER INTEGRATED CIRCUITS

Both in the industry and academia, GaN power ICs have been attracting a lot of interest because of the great advantages of achieving higher switching speed, better power conversion efficiency, and reduced form factor with custom functionalities such as integrated drivers, controllers, and sensors [5]. The holy grail of the GaN power ICs is the realization of a monolithic integration of low-side and high-side transistors, with other custom functionalities, on the same wafer which results in 100 V to 1800 V system on chip GaN ICs enabled by 200 mm QST®-based platform (Fig. 8).

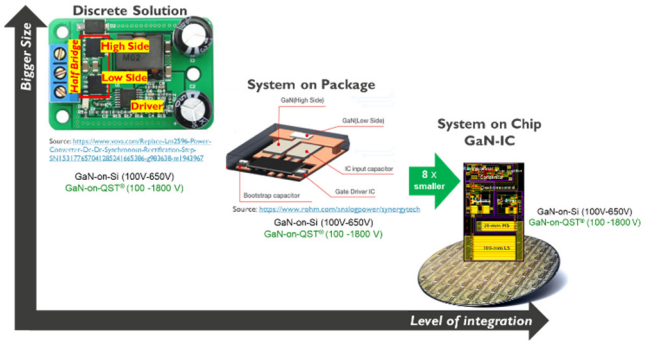

Fig. 8. Evolution from discrete GaN devices to wafer level monolithic 100 V to 1800 V system on chip GaN ICs, enabled by 200 mm QST® platform (scalable to 300 mm).

In this work, 200 V and 650 V GaN buffer and p-GaN gate power HEMTs, trench isolation, and wafer level monolithic GaN power ICs on 200 mm QST® substrates are demonstrated as a showcase to verify the feasibility of this concept [6-8]. Fully functional 200 mm GaN power ICs of a HEMT with integrated driver, half-bridge, and half-bridge with integrated drivers have been processed (Figs. 9-12).

Figure 9 shows 650 V monolithic GaN-on-QST® epitaxy structure and monolithic half-bridge IC device cross section with trench isolation and 650 V rated trench leakage, as reported in [7]. The monolithically integrated half-bridge comprises of a low side HEMT and a high side HEMT in which the source terminals of these two devices are connected to their respective substrate for suppressing the back-gating effect. Fig. 10 depicts the schematic ICs of the power HEMT with integrated driver, which can significantly reduce the parasitic inductance in the gate loop. The driver consists of a push-pull driver and two resistor-transistor logic (RTL) inverters, because of lacking p-MOSFET. The driver and the power HEMT are electrically isolated by oxide filled trenches around the devices, which are connected to the buried oxide (BOX). Fig. 11 shows a schematic and circuit of a GaN-on-QST® monolithically integrated circuit of a half bridge, in which contacts to the Si(111) device layer are formed to avoid back-gating effects and more importantly ~30% parasitic capacitance reduction compared to GaN-on-SOI is achieved. Fig. 12 demonstrates the half-bridge with integrated drivers and a level shifter. These designs are beneficial for suppressing oscillation, reducing device area, and enabling ever higher operating switching frequencies.

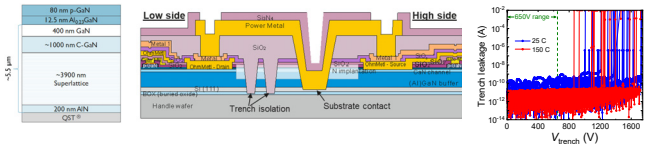

Fig. 9. 650 V monolithic GaN-on-QST® epitaxy structure and monolithic half-bridge IC device cross section with trench isolation and 650 V rated trench leakage.

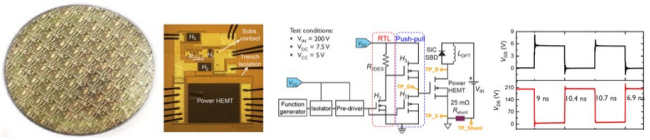

Fig. 10. Wafer level monolithic GaN-on-QST® ICs: power HEMT with integrated driver and its switching performance.

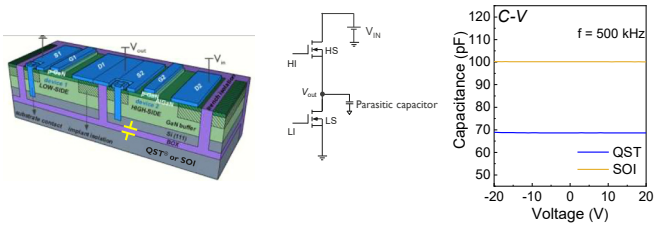

Fig. 11. Wafer level monolithic GaN-on-QST® ICs: eliminating back-gating effect and ~30% parasitic capacitance reduction with GaN-on-QST® compared to GaN-on-SOI.

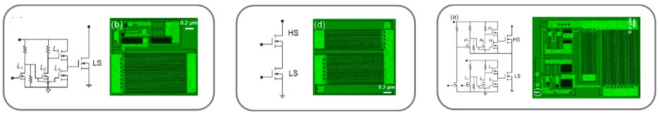

Fig. 12. Examples of 650 V GaN-on-QST® monolithic ICs: power HEMT with integrated driver, monolithic half-bridge, and monolithic half-bridge with integrated drivers and level shifter.

SEMI-VERTICAL / VERTICAL GAN POWER DEVICES

Vertical device architectures have several advantages compared to lateral devices, when scaling to high voltage operation [8-9] First, the fields are vertical over the bulk of the device, rather than peaking at the surface, improving reliability and stability (dispersion) of the devices. There is a potential for avalanche robustness, which has not been demonstrated for lateral devices. And lastly, the area of lateral devices becomes prohibitively large when scaling to large voltage due to the increased gate-drain distance, whereas for vertical devices the thickness of the epilayer (drift region) determines the breakdown voltage. However, most devices to date are either grown on bulk GaN substrates or on silicon. GaN substrates allow the growth of thick GaN layers but are small in substrate size and expensive. Si wafers are available in large substrate sizes, but the total GaN stack

thickness that can be grown is limited [10]. To fabricate vertical GaN devices a thick GaN layer is required.

The CTE matched QST® substrates offer a breakthrough in the growth of very thick GaN layers. As demonstrated in an earlier work, GaN Schottky barrier diodes on QST® exhibited a forward *I-V* characteristics comparable to that on GaN-on-GaN native substrates [11].

In this work, under a collaboration program between imec and AIXTRON and a continuation of the work in [12], epitaxial growth by MOCVD in a commercial AIXTRON G5+ C Planetary Reactor® with >8 µm GaN stack on 200 mm QST® substrates using a 5 µm thick drift layer for fabrication of semi-vertical / vertical devices is demonstrated. High crystal quality with very good run-to-run stability has been achieved combined with good control of wafer shape (Fig. 2).

PN-diodes fabricated on 200 mm QST® substrates reaching 550 V in reverse bias for stacks with 5 µm thick drift layer and 2E16 Si/cm^3 doping are shown in Fig. 13.

As shown in Fig. 14, multi-finger semi-vertical trench gate MOSFET devices ($W_{G,eff}$ = 60 mm) were also fabricated, as a test vehicle to demonstrate the device performance in on-state (2.5 nm Al_2O_3 / 100 nm SiO_2 is used as gate dielectric). A low on-resistance of 11 mΩ·cm^2 with 2.9 V threshold voltage was achieved.

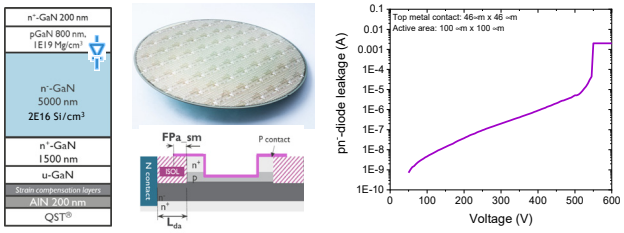

Fig. 13. PN-diodes fabricated on 200 mm QST® substrates reaching 550 V in reverse bias for stacks with 5 µm thick drift layer and 2E16 Si/cm^3 doping.

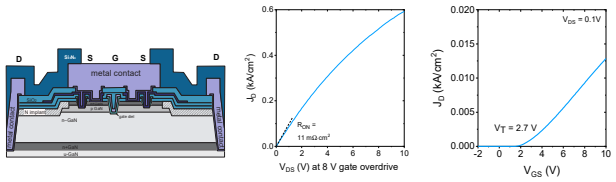

Fig. 14. Multi-finger semi-vertical trench gate MOSFET devices ($W_{G,eff}$ = 60 mm) (2.5 nm Al_2O_3 and 100 nm SiO_2 as gate dielectric) showing a low on-resistance of 11 mΩ·cm^2 with 2.9V threshold voltage.

Conclusions

In summary, commercial production of 650 V high-performance E-mode p-GaN gate HEMT devices on 200 mm, SEMI standard thickness QST® substrates have successfully commenced in a high-volume CMOS foundry manufacturing platform for industry players, and QST® substrates and GaN-on-QST® are now commercially available from QROMIS Inc. and Shin-Etsu Chemical Co. Ltd. The effective trench isolation in combination with the matched coefficient of thermal expansion provided by QST®-based technology platform pave the way to realization of next-generation GaN ICs and 1200 V and beyond power devices in lateral and vertical architectures.

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Acronyms

QST®: QROMIS Substrate Technology
CTE: Coefficient of Thermal Expansion
SEMI: Semiconductor Equipment and Materials International
CMOS: complementary metal-oxide-semiconductor
MOCVD: Metal-organic chemical vapor deposition
HEMT: High Electron Mobility Transistor
E-mode: Enhancement Mode