GaN-on-diamond design for manufacturing

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Abstract: Various processes of making GaN-on-diamond have been demonstrated. Few, if any, are manufacturable at wafer scale or in volume. In this paper we discuss a few aspects that make the GaN-on-diamond by direct diamond formation manufacturable and report on the consistency of results over more than 100 wafers.

INTRODUCTION

Gallium nitride (GaN) high electron mobility transistor (HEMT) devices have been driving the radio frequency (RF) and power industry for years[1]. This is because of the high break down voltages achievable in this material system. However, in high power applications, HEMT devices are still thermally limited. The natural solution is to pair GaN with diamond. because diamond has the highest thermal conductivity of any bulk material.

We have made and demonstrated GaN-on-diamond material that allows devices to operate at 50W/mm [2]. In this paper we will discuss how to manufacture the structuPre with high yields despite the inherent material defects, manufacturing inconsistencies and diamond variability. We then show the repeatability of the results within wafers and across wafer batches.

There are a few different methods for making GaN-on-diamond: growth of GaN on single crystal diamond; bonding of fully formed GaN to fully formed diamond; and direct diamond formation (DDF) where diamond is grown onto flipped GaN. In this paper, we focus on the DDF approach, which we believe is currently the most promising for mass manufacturing.

GAN-ON-DIAMOND BY DIRECT DIAMOND FORMATION

The process for making GaN-on-diamond was first demonstrated in 2006.[3] This process, which we continue to use, consists of taking fully formed GaN grown on <111> silicon, bonding it to a carrier silicon wafer and removing the <111> silicon substrate and transition layers, then growing in their place a diamond wafer. The process is completed by removing the carrier wafer.

Our goal is to make this process as reliably manufacturable as possible. A few points of difficulty in achieving this goal include: achieving a uniform carrier bond between the GaN grown on silicon wafer to a carrier wafer; achieving a uniformly low thermal resistance interface between the GaN and the diamond; limiting electrically active traps between the GaN and the diamond; and avoiding changes to the sheet resistance of the 2DEG after removal of the carrier wafer. A description of how each difficulty is overcome is discussed below.

Practical problems not be addressed here include the GaN strain control, diamond wafer uniformity and bow. These are too closely linked to the specific equipment to address in detail.

CARRIER BONDING

The first hurdle to reliable manufacturing is selecting the appropriate carrier bonding method. Carrier bonding typically depends either on a low temperature organic bond or on diffusion bonding. However, since the carrier bond of the GaN wafer needs to survive diamond growth temperatures which approach 800ºC; all organic bonds are not viable. Diffusion bonds typically rely on smooth surfaces with roughness of less than 0.1nm, and are therefore not desirable. To satisfy both the exposure to high temperatures and avoid the need for extreme cleanliness, we chose to develop a glass

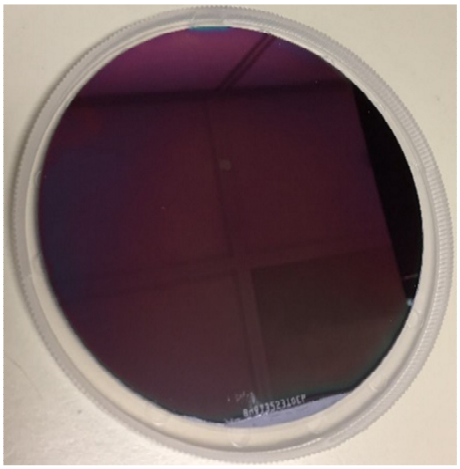

Fig. 1. Shows a 4” flipped GaN wafer onto a carrier silicon wafer. The bond is complete and the wafer laser ID can be seen near the epi flat.

bond. In this process, a custom spin on glass forms a layer of glass approximately 5um thick and has a melting point above 850ºC. This thick bond line allows the bonded wafer to survive the growth temperatures as well as being insensitive to roughness or particles up to about 5 µm in size. Figure 1 shows a wafer where the GaN epi has been flipped and the growth substrate removed.

Using this method, the bonded GaN and carrier wafer pair is flat. The bow of this bonded pair is typically lower than the spec of the epi wafer because the expansion coefficient between the growth substrate matches exactly the expansion of the carrier wafer. This flatness allows the growth substrate to be removed by a combination of grinding and etching. Grinding is important because it is faster and because wet etching is difficult since both the GaN growth and the carrier substrates both are silicon.

THERMAL INTERFACE

Another hurdle to reliable manufacturing is achieving a uniform repeatable and low thermal resistance thermal interface. Achieving this depends on removal of the transition layers and using the appropriate adhesion layer.

The first component of a uniform thermal interface is to remove the AlGaN transition layers. Once the epi is flipped and the substrate removed, the transition layers are exposed. The transition layers are part of the GaN grown on silicon structure they are an AlGaN mixture they are thick and highly defective because of the defects and the ternary composition they have a thermal conductivity of 10W/mK which makes them the largest thermal barrier in GaN epi [4]. These allow the GaN to be grown on silicon but have no function in the final device operation. Now that the epi has been flipped, the transition layers are exposed, they can be removed which significantly reduces the thermal interface resistance between the GaN and the diamond. We use a wet etch process selective to AlGaN over GaN.

The second component of a uniform low resistivity thermal interface is the adhesion layer. Ideally there would be no adhesion layer, unfortunately, GaN exposed to diamond growth conditions is etched along defect lines and leaves an electrically-active high thermal resistance interface. We use a SiN layer as an adhesion layer. This SiN layer is critical for the electrical and thermal properties of the final GaN-on-diamond substrate. The SiN both passivates the exposed GaN N-face and protects it from the diamond growth which includes atomic hydrogen. Unfortunately, the SiN has a thermal conductivity of approximately 3W/mK while the GaN has thermal conductivity of 160W/mK and the diamond 1600W/mK, the SiN has thermal conductivity of 3W/mK. It must thus be minimized to reduce the interfacial thermal boundary resistance. The competing manufacturing priority is that the interface needs to be thick enough that the thermal properties are consistent across the wafer and that the electrical properties are maintained. To balance these competing requirements, we chose a thickness around 300 Å. We measure the interfacial thermal boundary resistance by a technique pioneered by the University of Bristol[5]. Figure 2 shows the measurement of the TBR (thermal boundary resistance) over the center three inches of a 4-inch wafer. TBR is measured in m^2K/GW. The theoretical minimum TBR is 7 m^2K/GW the best demonstrated is around 10 m^2K/GW. A typical GaN on silicon wafer has a TBR above 100 here the bulk of this wafer has TBR around 23 m^2K/GW.

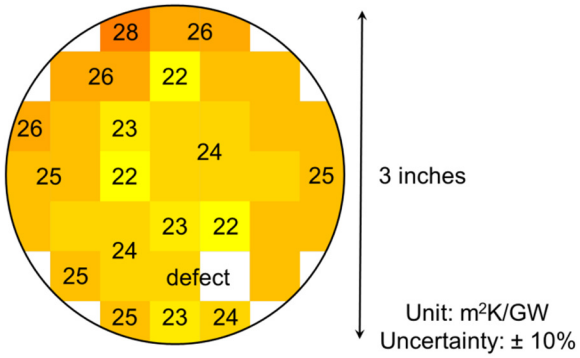

Fig. 2. Shows thermal boundary resistance measurements from a GaN-on-diamond wafer.

LIMITING ELECTRICALLY ACTIVE TRAPS

Once the adhesion layer is deposited, the diamond is grown. It is important to verify that the interface between the GaN

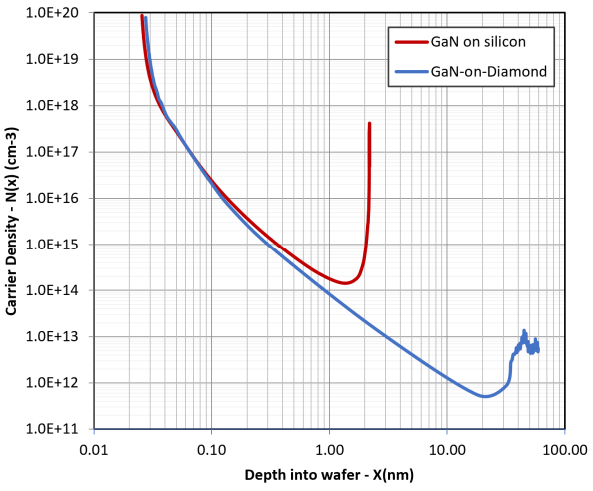

Fig. 3. Carrier density vs depth of GaN on silicon (red) and diamond(blue). From CV measurements with a 760um Hg probe.

and the diamond is not electrically active. Defects or traps at the interface between GaN and diamond would form a secondary channel which would affect the high speed or high voltage performance of devices. For GaN-on-diamond to be useful, it is not only important that the interface be thermally conductive, it is also important that it be electrically neutral.

To evaluate the electrical characteristics of our interface, we take a CV measurement of the substrate. By varying the voltage of the CV measurement, we can extract the charge density as a function of depth into the semiconductor. For comparison, we plot the charge density vs depth characteristics of the original GaN grown on silicon epi and compare to the same epi after transfer to diamond. This comparison is shown in figure 3.

The GaN on a silicon substrate in the CV measurements cannot deplete the carriers past the transition layers which are highly defective. However, measuring the same GaN after it was transferred to diamond and transition layers have been removed, the measurement can deplete the carriers deep into the diamond itself, showing no electrical traps at the GaN to diamond interface.

SURFACE DAMAGE AND 2DEG SHEET RESISTANCE

The finally we wish to show the consistent electrical characteristics over a number wafers. The metric we chose is the sheet resistance. The sheet resistance is a good indicator of the electrical performance of the wafer and can be mapped on the GaN before and after the epi transfer to diamond. Our goal is to reproduce the electrical performance of the GaN on silicon in the GaN-on-diamond. In figure 4, we map about 100 4" wafers and plot the average wafer sheet resistance of the GaN before and after the transfer to diamond. Showing that the GaN sheet resistance has not significantly change during the epi transfer process is a good indicator that the GaN can be reliably transferred to diamond without affecting its electrical properties.

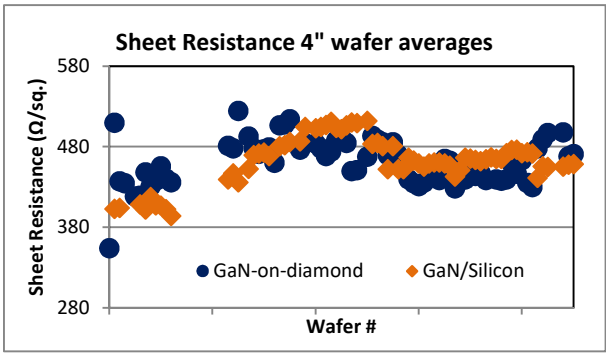

Fig. 4. Sheet resistance average on 100 wafers taken from the average of 100 measurements per wafer. Experimental wafers excluded.

CONCLUSIONS

From the data shown we have demonstrated the DDF process with characteristics consistent with volume manufacturing. In particular, the DDF process is robust to variations in the process and initial materials while maintaining the required thermal and electrical characteristics. We show good thermal and electrical characteristics across wafers and through batches of wafers, to date we have produced over 1000 wafers using this process and have the capability of producing 100's of wafers per year.

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ACRONYMS

2DEG: 2-Dimensional Electron Gas
DDF: Diamond Direct Formation
HEMT: High Electron Mobility Transistor
CV: Capacitance Voltage

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