DoD Microelectronics: Heterogeneous Integration with Compound Semiconductors and Photonics

Devanand Shenoy[1], Darren Crum[2], Brian Olson[2], Joshua Hawke[2]

[1]Office of the Undersecretary of Defense for Research and Engineering, Critical Technology's Office, Arlington, VA
[2]Naval Surface Warfare Center Crane Division, Crane, IN

Keywords: heterogeneous integration, microelectronics, multi-chip package, gallium nitride, co-packaged optics

Abstract - The Department of Defense (DoD) requires affordable access to advanced microelectronics that offers the performance necessary to address evolving threats in a contested environment. This necessitates solutions in state-of-the-art (SOTA) materials, devices, and architectures. Multi-chip package (MCP) prototypes leverage heterogeneous integration to combine the most advanced commercial digital and radio frequency (RF) technology. DoD-specific chiplets are integrated within assured assembly, packaging, and test facilities. Investments in advanced RF nodes and epitaxial materials offer superior access to millimeter wave (mmW) spectrum, while co-packaged optics (CPO) provide efficient, high-bandwidth data transfer. By aligning supply chain investments, DoD seeks to move towards true heterogeneous integration of compound semiconductors and photonics to produce high-performance transceivers and other subsystems needed to achieve spectral dominance for defense systems.

INTRODUCTION

The Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E)) Trusted and Assured microelectronics (T&AM) program is investing in the U.S. microelectronics sector to create broader competitiveness for our economic and national security. Technological superiority of national security missions depends on rapid development and transition of new technologies into capabilities faster, cheaper and with higher performance and greater security than any other nation. As a key enabling technology, microelectronics are crucial to achieving innovative products for nearly all modern defense systems. Future defense systems rely on agile tactical capabilities that can: integrate information across all domains and the electromagnetic spectrum, understand the operational environment, make decisions, and disseminate information. Microelectronics are essential to the hardware that provides DoD with overmatch capabilities against adversaries and positions the U.S. for global commercial advantage and competitiveness.

Despite the critical role of microelectronics technologies, fabrication and innovation ecosystem are increasingly moving overseas driven by commercial demands. U.S. production has dropped from about 37% in 1990 to nearly 12% today. A globalized supply chain increases security risks and hampers competitiveness by providing adversaries easy access to the same advanced technology. Furthermore, the rising costs of semiconductor design and manufacturing at the cutting edge has led to consolidation into a few suppliers that are driven by high product volumes. Based on design cost and yield considerations modern systems on chips aggregate a large range of functionality into a single monolithic chip.

For over a decade it has been challenging for the DoD to access SOTA microelectronics beyond the utilization of commercial off-the-shelf (COTS) chips. DoD's small product volumes and reliance on a broad range of discrete technologies and specialized designs do not align well with commercial fabrication. The DoD requires access to advanced microelectronics at low cost, as well as specialized materials, devices and architectures that provide the edge needed to defeat evolving threats in a contested environment. To address these challenges, OUSD (R&E) has established the T&AM program to drive innovation in key technology areas in partnership with commercial technology leaders and the defense industrial base (DIB). These efforts include investments in heterogeneous integration technologies and RF and optoelectronics (RF/OE) technologies.

HETEROGENEOUS INTEGRATION TECHNOLOGY

The recent industry trend toward chiplets and three dimensional (3D) packaging represents a paradigm shift that offers the DoD a unique opportunity to adopt leading edge technology. This monolithic die disaggregation into chiplets approach divides a complex design, such as a processor, into several small die. A chiplet is defined as a monolithic die with a single function or purpose that is designed to be integrated into a multi-chip package (MCP). Heterogeneous integration can be leveraged to combine the most advanced commercial digital and RF technology with DoD-specific chiplets in an assured assembly, packaging and test facility.

DoD's SOTA Heterogeneous Integrated Packaging (SHIP) program is developing and demonstrating a novel approach towards DoD sustained access to measurably secure, heterogeneous integration and test of advanced packaging solutions for customized DoD devices using SOTA chips packaged and tested in the commercial flow. Sustained

access is demonstrated by developing a series of multiple MCP prototype demonstrators for use in DoD military systems. MCP prototype designs demonstrate continually increasing scope of functionality, performance, and complexity. This will accommodate increasing functionality and performance needs of the military systems to meet their modernization goals. Advanced features such as optical interfaces, security, cyber protections, and 3D stacking will be incorporated as they become production ready. The resulting access model will become self-sustained and could be applied to multiple packaging vendors. The chiplet ecosystem will continue to expand with ever-increasing breadth of functionality and performance. Heterogeneous integration offers the following benefits for DoD:

- Allows post foundry manufacturing personalization for intellectual property (IP) protection, permitting die to be sourced from any foundry.
- Allows DoD specialty chiplet integration for greater performance for both digital and RF applications while achieving size weight and power (SWAP) needed for operational systems.
- Lowers cost and risk to integrate advanced technologies as they emerge, such as non-flash based non-volatile memory, non-silicon devices, neural networks, photonics, etc.
- Shortens transition time of SOTA microelectronics for DoD specific applications optimized to meet performance and/or security requirements and early and privileged access through sustained industry relationships.

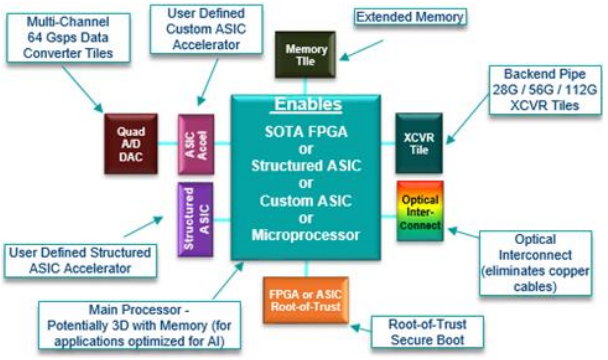


Figure 1. Notional Heterogeneous Integration Example

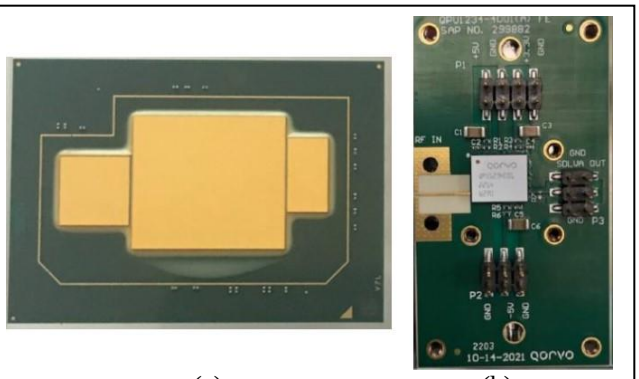
Under the SHIP program, Intel Federal and Qorvo are developing several prototype devices as performers under the SHIP Digital and SHIP RF programs, respectively. SHIP Digital is focused on the development of SOTA MCPs to drive size, weight, power, and cost (SWAP-C) reductions and expand DoD-wide access to chiplet-based MCP solutions. To that effect, reuse has been identified as a key component of the SHIP Digital model and is being realized by leveraging the existing design and layout IP between MCPs and the reuse of physical chiplets, which will reduce development time and cost. In contrast, SHIP RF focuses on design, packaging, and assembly as a service. Qorvo is developing design and assembly kits that will enable users to design SOTA RF packages with custom design flows, advanced packaging platforms, and a wide selection of material choices to support specific use cases. The performers, in conjunction with the DIB, are designing and building multiple prototypes that will be transitioned into fielded DoD systems.

The SHIP Digital program provides DoD access to Intel's SOTA microelectronics packaging capabilities. It leverages reuse of chiplets including field programmable gate arrays (FPGAs), custom application specific integrated circuits (ASICs), data converters, transceivers, and optical tiles, among other technologies. Chiplets, based on hard IP blocks, allow for disaggregation of fabrication at an optimized node process per die. A notional heterogeneous integration of disparate chiplet technologies is shown in Figure 1. Additionally, smaller die supported by chiplet integration have higher fabrication yield, optimizing cost per function. SHIP Digital will leverage commercial industry flow and capabilities to develop a business and operational model that allows for DoD and commercial IP to be seamlessly integrated using modular chiplet-based platforms. Transition of these products into military systems is essential to establish a healthy and robust ecosystem. SWAP-C savings are showcased by demonstration in exemplar systems which will drive interest to additional MCP and chiplet development. Once a thriving ecosystem is established, SHIP Digital will provide the DoD access to a robust catalogue of chiplets that can be configured, assembled, and packaged for standard, derivative, or custom parts. The MCPs developed under this phase of SHIP will all be integrated using Intel's commercial embedded multi-die interconnect bridge (EMIB) platform. This is a 2.5D package solution which efficiently combines multiple die to increase input-output (I/O) count and reliability compared to traditional planar solutions.

SHIP-RF will establish domestic manufacturing for SOTA heterogeneously integrated packaging for RF applications. The program will provide secure access to design, assembly and test for advanced packaging for DoD, DIB, commercial companies, as well as supporting other DIB collaborators. SHIP-RF will manage technology and customer IP with secure process and protocols by using Qorvo's commercial expertise and established history. SHIP-RF has three execution areas; the SHIP RF Design Center (DC), SHIP RF Assembly and Test Center (ATC), and advanced technology development. Qorvo is enabling access to advanced RF packages by developing design kits, maturing advanced packaging platforms, and offering a wide selection of material choices to support specific use cases through the SHIP RF Design Center (DC) and SHIP RF ATC. Qorvo has formed the SHIP-RF DC to operate as a hub for customer design submissions into the SHIP-RF ATC. This allows Qorvo and lead partners to test run engineering and revision tools developed for the design community in an external packaging foundry environment. Tools such as process design kits (PDKs), product lifecycle management (PLM), bill of material (BOM), engineering change orders (ECOs) and

supply chain management systems can be baselined for external foundry operation. Development of assembly design kits (ADKs) and integrated software design flows are underway.

The SHIP program will rely on collaboration between the DoD, DIB, and the microelectronics industry to develop a sustained model for access to SOTA packaging. The first prototypes developed with SHIP Digital and SHIP RF have been delivered (see Figure 2). Pilot programs and studies are underway to prove out environmental qualifications and quantifiable SWAP benefits.



(a) (b)

Figure 2. Delivered prototypes from the (a) SHIP Digital and (b) SHIP RF programs.

RF/OE Technology

In general, manufacturing processes for RF and photonic devices are relatively immature in comparison to silicon-based compute processes. Therefore, the DoD looks to partner with industry to accelerate the maturation of new material sources, devices, and packages that enable components, such as high-performance transceivers. As emerging dual-use performance requirements quickly escalate into millimeter wave (mmW) frequencies (30–300 gigahertz (GHz), there is a clear opportunity to collaboratively support a broad swath of evolving applications, such as defense, radio astronomy, remote sensing, automotive radars, imaging, security screening, datacom and telecom.

A sundry array of semiconductors offer access to higher-frequencies: Gallium Nitride (GaN), Silicon Germanium (SiGe), RF silicon on insulator (SOI), RF complementary metal oxide semiconductor (CMOS), Gallium Arsenide (GaAs), Indium Phosphide (InP), etc. However, the T&AM program has taken special interest in RF GaN epitaxy on Silicon Carbide (SiC) substrate primarily due to its superior SWAP and cooling benefits (see Figure 3).

The T&AM program has strategically partnered with the Defense Advanced Research Project Agency (DARPA), Air Force Research Laboratories (AFRL), Army Research Laboratories (ARL), the Office of Naval Research (ONR), and Naval Surface Warfare Center Crane to mature materials, fabrication, packaging, and open access design access to SOTA mmW GaN across the supply chain. Over nine science and technology (S&T) contracts have been transitioned into

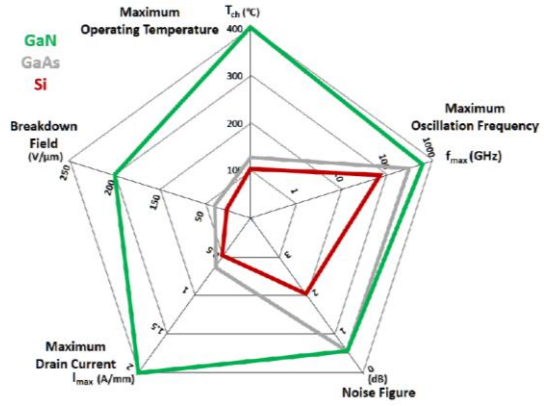


Figure 3. Comparison of GaN, GaAs, and Si devices across 5 key figures of merit for RF components.

three capstone maturation projects, which are uniquely designed to accelerate technology maturation across the supply chain (see Figure 3).

One capstone maturation project is the SOTA RF Gallium Nitride Foundries (STARRY NITE) project (see Figure 4). Here, the DoD has partnered with HRL Laboratories, Northrop Grumman Space Systems, and Qorvo to mature multiple production-grade mmW foundry nodes and

Figure 4. RF/OE investments mature RF GaN and Co-Packaged Optics and align with the DoD packaging ecosystem via demonstration programs including: SHIP, Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and innovate in the Packaging Ecosystem (STEAMPIPE), and Reshore Ecosystem for Secure Heterogeneous Advanced Packaging Electronics (RESHAPE). These efforts will accelerate transition across the supply chain.

advanced interconnect services. Open access design opportunities are made recurrently available at https://info.nstxl.org/starry-nite-mpw-program. This stimulates affordable and innovative designs, generates government purpose IP, and offers a platform for insertion of best-practice assurance. In 2023, the Eclipse capstone project will continue maturation of materials with advanced performance and then partner with mmW foundries, such as those in STARRY NITE, to demonstrate advanced device production. Furthermore in 2024, STARRY NITE will offer advanced interconnect multi-project wafer (MPW) runs. This will allow designers to apply advanced packaging techniques (e.g., flip chip onto interposer) to mmW GaN devices.

Ultimately, these MPW prototype designs not only serve as test chips to prove out the foundry offerings as they mature, but also target device transition into dual-use applications and programs of record (PoR).

To sustain RF IC technologies for DoD needs, future investment is being considered to mature and assure access to material, foundries, and packaging facilities that support GaAs, SiGe, InP, RF SOI and RF CMOS devices. In addition to RF GaN, these materials are critical to retaining U.S. leadership in 5G millimeter wave deployment. Power amplifiers for 5G communications are composed of semiconductor gallium nitride and polybutylene PBT-package power amplifier for 28GHz. Other materials such as Silicon-germanium (SiGe) power amplifiers too operate at higher frequencies, albeit at lower power rates than gallium-based devices. As vacuum electronics device (VED) vendors face extinction, end-of-life transition plans may be needed to leverage various solid state technologies for replacement (e.g., RF GaN, RF GaAs, RF CMOS, etc.). Just as active antenna systems reshaped the RF front-end ecosystem, it is anticipated that wideband amplification, switching, and adaptive filtering will foster the next wave of disruptive wireless technologies, and this will require advanced in various RF components and substrates.

In addition to RF devices, the DoD is investing in photonic integrated circuits (PICs). Presently, the PIC supply chain is extremely fragmented, but experiencing nascent commercialization to support production of silicon photonics, especially for emerging datacom capabilities. Data centers – once able to rely on parallelism – are now facing a data movement bottleneck, which can only be resolved by disaggregation techniques and CPO. CPO integrates PICs with electronic integrated circuits (EIC) inside MCPs to enable long-reach and high-bandwidth data I/O.

DoD seeks to harness the emerging CPO market demand through the capstone project Co-Packaged Analog-Driven High-Bandwidth Optical Chiplets (KANAGAWA). This effort partners with companies such as Ayar Labs, Intel, Lockheed Martin, and Qorvo to mature the design, fabrication, and packaging of optical I/O chiplets and lasers. Critical collaboration also exists with IBM Bromont and AIM Photonics' Testing, Assembly, and Packaging (TAP).

In contrast to using copper electrical wires on a circuit board, CPO intimately ingrates optical I/O into MCPs by leveraging integrated photonics manufacturing that produce compact optical chiplets. In combination with advanced microelectronic packaging methods that enable short wire lengths from EICs to PICs inside a package, CPO provides significantly lower power consumption and higher data rate than board-level systems. Recent demonstrations from the DARPA Photonics in the Package for Extreme Scalability (PIPES) program have produced Tbps-level data throughput from a single chiplet, consuming only 5 pJ/bit. Such technology offers to significantly expand the capabilities of defense ME. For example, (FPGA) with CPO can generate dramatically higher data rates when processing digital beamforming signals, opening up the possibility of new phased array radar architectures and element-level beamforming. By maturing the production process, KANAGAWA will transition CPO I/O technology directly into the DoD packaging ecosystem via demonstration programs like SHIP, STEAMPIPE, and RESHAPE.

The Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act is motivating a whole of government approach to on-shoring more microelectronics capabilities to promote both national and economic security. DoD's Microelectronics Commons is a CHIPS Act-funded national network that will create rapid pathways to commercialization for U.S. microelectronics start-ups, researchers, and designers from "lab-to-fab." The Commons research focuses on prototyping capabilities for a range of defense and commercial applications including those related to RF/OE such as: 5G/6G technology, electromagnetic warfare, and commercial leap ahead technologies.

In addition to leveraging commercial high-volume trends, the DoD has many unique applications of interest as well, and strongly supports open access programs and high-mix partners, such as AIM Photonics. A Distribution D Report (DoD and DoD contractors only) called "Picasso's Musicians" was recently published, assessing the industrial base for photonics in light of dual-use and DoD-unique needs. This report can be requested from OUSD(R&E) Microelectronics by emailing: osd.pentagon.ousd-r-e.mbx.ct-et-microe@mail.mil

CONCLUSIONS

DoD's T&AM program is investing in key technology areas of heterogeneous integration technology and RF/OE technology. By moving towards true heterogeneous integration with compound semiconductors and photonics, will strengthen and secure enabling domestic manufacturing technologies to support defense missions for years to come.

ACKNOWLEDGEMENTS

The authors would like to acknowledge OUSD(R&E) Microelectronics as the sponsor of the T&AM program and OUSD(R&E) S&T Futures for co-funding the effort. A special thanks to OUSD(R&E) Microelectronics, OUSD(R&E) S&T Futures, Naval Research Laboratories and Georgia Tech Research Institute for authorship of this report.

REFERENCES

[1] D. Crum, and J. Sotir, "State-of-the-Art Heterogeneous Integrated Packaging (SHIP) Program Prototype Device Design Methodology," GOMAC Conference, Virtual, 2022.

[2] D. Crum, B. Hamilton, T. Jones, B. Olson, and J. Sotir, "State of the Art Heterogeneous Integrated Program," GOMAC Conference, Virtual, 2021.