Mechanisms and Control of Photolithography Hotspots in Compound Semiconductor Manufacturing

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Abstract

One of the major challenges in photolithography's ability to consistently pattern fine geometries is differences in best focus across the wafer and within processing fields. These differences on the patterned side of the wafer are generally understood, well characterized, and corrected for when choosing and optimizing focus settings. However, unexpected and varying deformities on the wafer backside compromise the field leveling (shifting focus due to substrate height differences) during exposure. This results in poorly resolved pattern where the contamination was present. These defects are generally known as "hotspots." In this study, one failure mode with repeatable double aberrations is investigated and characterized. The results show that unintended backside mesas are formed due to a novel integrated defect mode comprising Si_xN_y deposition and GaAs wet etching. These mesas then give rise to hotspots during metal interconnect photolithography and result in yield loss of 1% or more. This study demonstrates the importance of detection, characterization, and minimization of patterning distortions to enable continued device advancement, yield improvement, and cost reduction in compound semiconductor manufacturing.

INTRODUCTION

Lithography is an indispensable technique in the semiconductor industry as a precursor for etch, deposition, and ion implantation [1-4]. Maintaining proper and consistent focus and dose control is critical for ensuring sidewall angle and feature sizing to meet device functionality and reliability needs [2]. Therefore, advancing lithography technology is essential for enabling device performance and improving die yields in the semiconductor industry [5]. Device features can be patterned at a fraction of the Abbe diffraction limit using innovative approaches such as immersion lithography, double or multiple patterning, resolution enhancement techniques, and much more [1, 6-8].

Beyond achieving denser patterning and smaller feature sizes, there are many practical challenges for robust lithography deployment [5, 9-11]. One such challenge is patterning distortions or "hotspots," which can be caused by contamination on the backside of the substrate, the stepper chuck, or both [9]. This compromises the field leveling (shifting focus due to substrate height) during exposure, which results in poorly resolved patterns where the contamination was present [10]. Advanced manufacturing approaches such as fault detection and classification (FDC) can be used to rapidly detect and minimize the impact of hotspots [12]. Once the contamination on the stepper chuck has been detected, a chuck-cleaning or "sticky" wafer can in some cases be used to remove the contamination without performing invasive and time-consuming maintenance on the tool [13]. In other cases, hotspots can be more subtle and challenging to resolve [12].

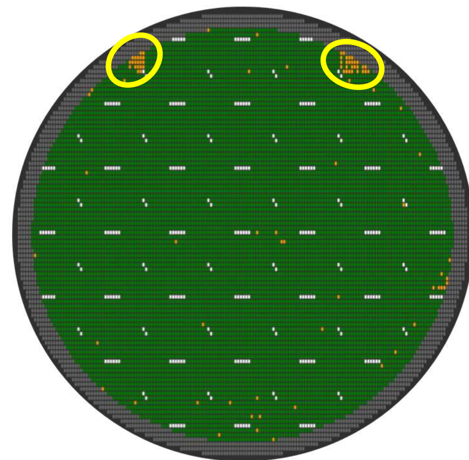

Fig. 1. Wafer map showing yield loss at 11 and 1 o'clock positions of wafer due to patterning distortions or "hotspots." Yield loss is on the order of 1% or more.

Skyworks Solutions has developed and implemented a multifaceted approach to detect, characterize, and minimize the occurrence of hotspots in photolithography patterning. The approach includes regular stepper hotspot monitor qualification checks, consistent wafer backside cleaning, use of "sticky wafer" to remove metal and other debris from the chuck, and in-line fault detection and classification. While these improvements have been invaluable, opportunities remain for further reduction of hotspots. In the current work,

a unique double hotspot is investigated and found to be caused by an integrated defect mode comprising Si_xN_y deposition, wet etching, and photolithography. The patterning distortions are particularly acute due to high patterning density in Device F. The results demonstrate the critical importance of rapidly identifying and controlling lithography hotspots in semiconductor manufacturing.

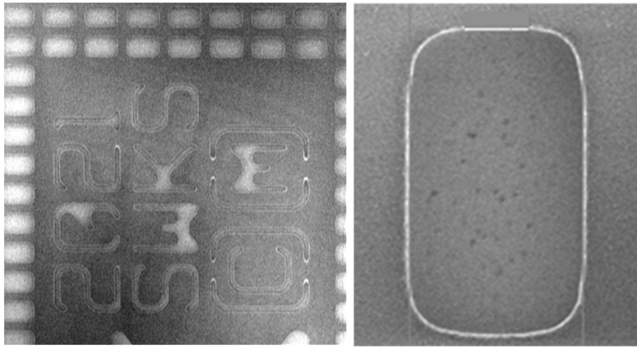

Fig. 2. Electron micrographs from hotspot areas showing poorly resolved and distorted features. Note the rounded corners and curved sides of the rectangle. These distortions are due to the stepper being misfocused as a result of non-planarity of the backside of the wafer.

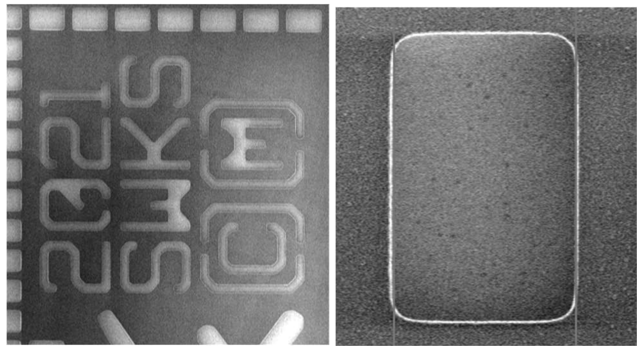

Fig. 3. Electron micrographs from non-hotspot areas showing well-defined and non-distorted features. The backside of the wafer is more uniform and planar, which results in the stepper being well focused. The sides of the rectangle are straighter, as desired, and the designed patterning density is achieved.

Experimental Procedure

Production wafers were characterized with automated optical inspections (AOI), process control monitor (PCM), and die probe. A unique failure mode, double aberrations in the first interconnect layer, was encountered with Device F. Defective and healthy dies were imaged using scanning electron microscopy (SEM). Once the frontside defects were characterized, wafer backside inspections were performed to determine the cause of the patterning distortions. Inspections were performed visually, with a Heidenhain MT12 depth gauge, and with a Zygo 3D optical profiler.

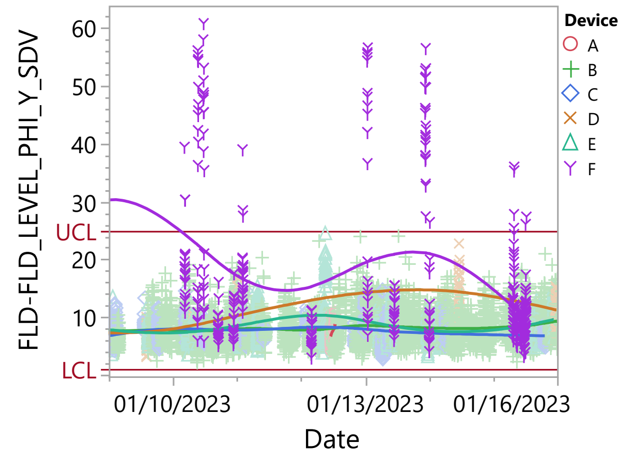

Fig. 4. Stepper field leveling FDC report showing higher variability for Device F.

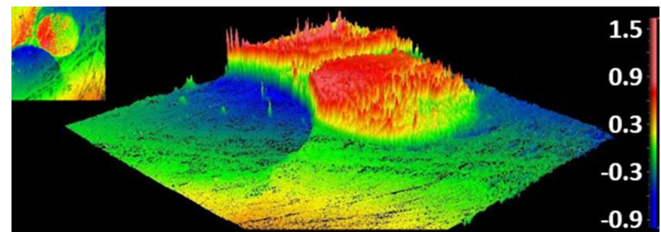

Fig. 5. Contour plot of unintended backside mesa beneath frontside hotspot at 11 o'clock position of wafer. A similar mesa was found at the 1 o'clock position (not shown). The mesas are approximately 1.2 µm in height and are formed when the collector contact wet etch is blocked due to surface modification from an earlier Si_xN_y deposition process. A top view of the mesa is shown in the inset for reference.

After characterizing wafer backside mesas, the production line was segmented to determine the source of the mesas. Controlled wafer orientation experiments were performed at various suspected operations prior to the photolithography step where the hotspots were detected. Lastly, backside mesas were characterized with energy dispersive X-ray spectroscopy (EDX) to determine their elemental compositions.

Results and Discussion

Die yields and device parameters were generally excellent upon ramping Device F to high volume production; however, wafers presented varying levels of yield loss due to recurring defects at the 11 and 1 o'clock positions of the wafer (Fig. 1). Visual inspections of the wafers verified double aberrations at these positions. Defective and healthy dies were then imaged

using SEM as shown in Figs. 2 and 3, respectively. SEM revealed that device features in the defective areas were poorly resolved and distorted as compared to intended features. The first appearance of these defects in-line was after the first interconnect photolithography step (prior to metallization and liftoff). FDC revealed that the field-to-field leveling parameters were elevated on Device F as compared to other devices (Fig. 4). Based on this data, it was thought that hotspots or backside contamination might be disturbing the first metal patterning for dies at the 11 and 1 o'clock positions of the wafer.

Backside wafer inspections revealed mesas beneath the defective dies. Mesa heights were determined to be approximately 1.2 µm using both a depth gauge and an optical profiler. A representative contour plot is provided in Fig. 5 for reference. The process flow of Device F was carefully compared with the flows of other devices to determine possible causes of the hotspots. The flow contains a wet etch (H_3PO_4 / H_2O_2) with a depth target of just over 1 µm. Therefore, a hypothesis was formulated in which the mesas could have been generated if these areas were rendered impervious to the etch process.

To test the blocked etch hypothesis, controlled wafer orientation experiments were performed at the wet etch step. It was found that backside mesas formed at the 11 and 1 o'clock positions irrespective of orientation during the wet etch process. This result showed that an incoming factor must be modifying the backside surface of the wafer at those locations. Therefore, wafer orientation experiments were performed at an earlier silicon nitride (Si_xN_y) deposition process. These experiments showed conclusively that the orientation of the mesas and patterning distortions could be directly controlled by wafer orientation during the Si_xN_y deposition process.

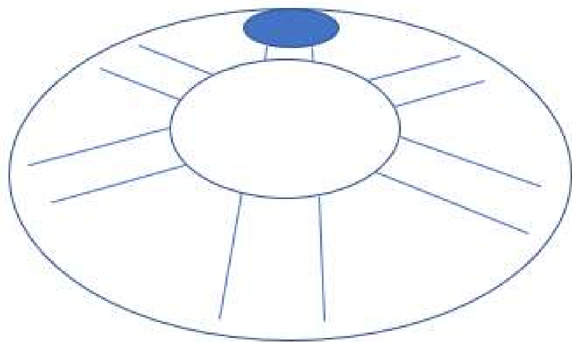

Fig. 6. Schematic showing stations in Si_xN_y deposition tool and handling forks at each station. The location of the forks has been strongly correlated to areas blocked during a subsequent wet etch process. The resulting wafer backside topography gives rise to frontside patterning distortions at photolithography.

Si_xN_y films in this study were deposited by plasma-enhanced chemical vapor deposition (PECVD) using a mixture of SiH_4, NH_3, and N_2 at 300 °C. A schematic of the interior of the deposition tool is provided in Fig. 6 for reference. Each wafer is processed serially through the stations in the deposition system. Wafers are handled by parallel ceramic forks at each station. The location of the forks was found to be strongly correlated to the backside mesas formed after wet etch and the pattern distortions after M1 photolithography.

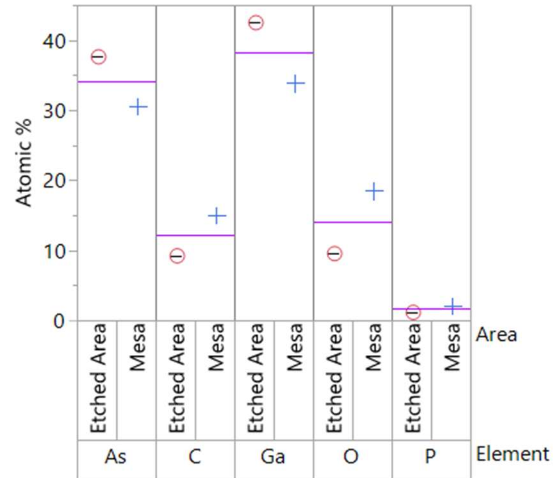

Fig. 7. EDX results from backside mesas (blocked etch areas) and uniformly etched areas. The mesas have a higher percentage of carbon, which may serve as a mask during a wet etch process. Note that H_3PO_4 (from the wet etch) is the source of the P.

Upon discovering the origin of the undesired mesas, they were then characterized with EDX. The results, provided in Fig. 7, show a slightly (5 at. %) elevated level of carbon in the mesas. It is theorized that the carbonaceous contamination may have blocked the wet etch process. The results show that the patterning distortions are caused by an integrated defect mode comprising Si_xN_y deposition, wet etch, photolithography, and high patterning density.

CONCLUSIONS

In this study a unique failure mode, double hotspots, has been characterized, investigated, and traced back to its source. Patterning distortions at the first metal interconnect layer are caused by a novel integrated mechanism comprising Si_xN_y deposition, wet etching, and photolithography. Wafer non-planarity combined with high patterning density gives rise to low yield in the hotspot areas. The results demonstrate the critical importance of identifying and controlling lithography hotspots in semiconductor manufacturing.

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Acronyms

AOI: Automated Optical Inspection
EDX: Energy-Dispersive X-Ray Spectroscopy
FDC: Fault Detection and Classification
M1: Metal-1 Interconnect
PCM: Process Control Monitor
PECVD: Plasma-Enhanced Chemical Vapor Deposition
SEM: Scanning Electron Microscopy
Si_xN_y: Silicon Nitride