Structural and Electrical Characterization of Schottky Barrier Diodes on 100 mm HVPE β-Ga_2O_3 Epiwafer Technology

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Abstract

X-Ray topography of halide vapor phase epitaxial (HVPE) β-Ga_2O_3 epiwafer and full-wafer electrical (current-voltage, capacitance-voltage) characterization of subsequently fabricated Schottky barrier diodes are reported for the first time. The wafer exhibited excellent carrier concentration uniformity, near-unity ideality factors, and low reverse leakage current using a Pt-based anode. Pulsed-mode forward bias I-V testing yielded current densities in the 250-300 A/cm^2 range.

INTRODUCTION

Monoclinic (β-phase) gallium oxide (β-Ga_2O_3) is the only ultra-wide bandgap (4.6-4.9 eV) semiconductor platform with a large area native substrate technology and the ability to grow high quality, thick (10-20 µm) homoepitaxial layers with controllable doping concentrations. These properties make β-Ga_2O_3 a leading candidate for next-generation power semiconductor devices with high power figure of merit. The high critical field of Ga_2O_3 (6-8 MV/cm) suggests that the breakdown performance of vertical devices can be maintained using a thinner epilayer, resulting in lower specific on-resistance, faster transit times, lower switching and conduction losses, and thus higher overall efficiency. Gallium oxide substrate and epitaxy technology has advanced tremendously since the first device demonstration a decade ago [1]. In 2022, crystal growth using several different methods (EFG, Czochralski, Vertical Bridgman) have yielded high quality crystals that have commercialized the 4-inch substrate technology required for device commercialization [2]. High growth rate epitaxial techniques such as MOCVD and HVPE have pushed commercial drift layer thicknesses with the expectation that high quality and low defect density epilayers will enable ultra-high voltage (>20 kV) vertical diodes and transistors [3].

EXPERIMENTAL

A 100 mm diameter HVPE β-Ga_2O_3 epiwafer on an n$^+$ (001) Ga_2O_3 substrate was supplied by Novel Crystal Technology, Inc. The average epilayer thickness was 9.6 µm, and average free carrier concentration of 1.5×10^{16} cm^{-3} was measured using the non-contact ECV technique. Across the wafer, measured epi thickness range was 8.8-10.1 µm and the carrier concentration range was 1.4-1.7 $\times10^{16}$ cm^{-3}. X-Ray topography (XRT) was performed at NRL using Rigaku XRTmicron X-ray topography system. Schottky barrier diodes were fabricated using a blanket substrate-side Ti/Au cathode annealed at 470 °C for 1 minute, followed by epi-side gridded Ni/Au anodes in order to facilitate defect characterization under bias. Electrical characterization of >3000 devices over the full 100 mm wafer (10 mm exclusion zone) was performed using a computer-controlled wafer prober and a Keithley 4200SCS semiconductor parameter analyzer for DC measurements and a Tektronix 371 curve tracer for pulsed-mode measurements. Large-diameter probes were utilized to minimize possibility of probe-induced leakage current [4].

RESULTS AND DISCUSSION

Figure 1a shows the g=(224) XRT, image of the wafer, using Cu Kα radiation, showing a number of structural defects such as slip planes near the edge of the wafer. Thus, a 10 mm exclusion zone was implemented in the electrical characterization of this wafer. Other regions of interest, shown in purple squares, exhibited dislocation bundles that will be the subject of further investigation of individual devices. The g=(020) XRT image, using Mo Kα, in Fig. 1b shows diffraction data from the substrate as well as the epitaxial layer on the wafer.

Figure 1c shows a photograph of the 100 mm wafer with fabricated vertical Schottky barrier diodes (SBDs). Electrical characterization plots obtained by I-V and C-V measurements are shown in Fig. 2-4. While the on-state resistance from the largest devices was about 2× higher (15-17 mΩ-cm^2) than the small SBDs in the PCM areas (Fig. 2a), the ideality factor and reverse leakage current (Fig. 2b-c) were very uniform across the wafer. In pulsed-mode, current densities of about 300 A/cm^2 range (~2.5 A current at 50% power, Fig. 4b) were routinely measured on the large-area devices. Reliable pulsed-mode mapping across the wafer was complicated by

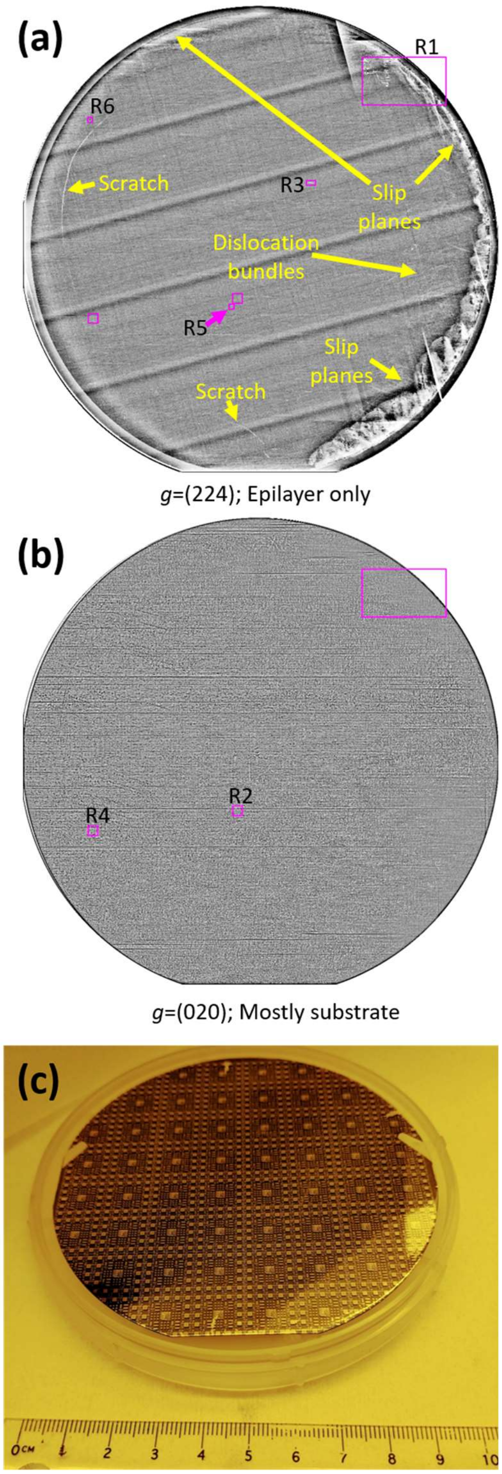

Fig. 1. X-Ray topographs of 100 mm β-Ga_2O_3 HVPE epiwafer along the (a) (224) and (b) (020) reflections obtaining signal from epilayer and substrate, respectively. (c) Photograph of same epiwafer processed with vertical Schottky barrier diodes.

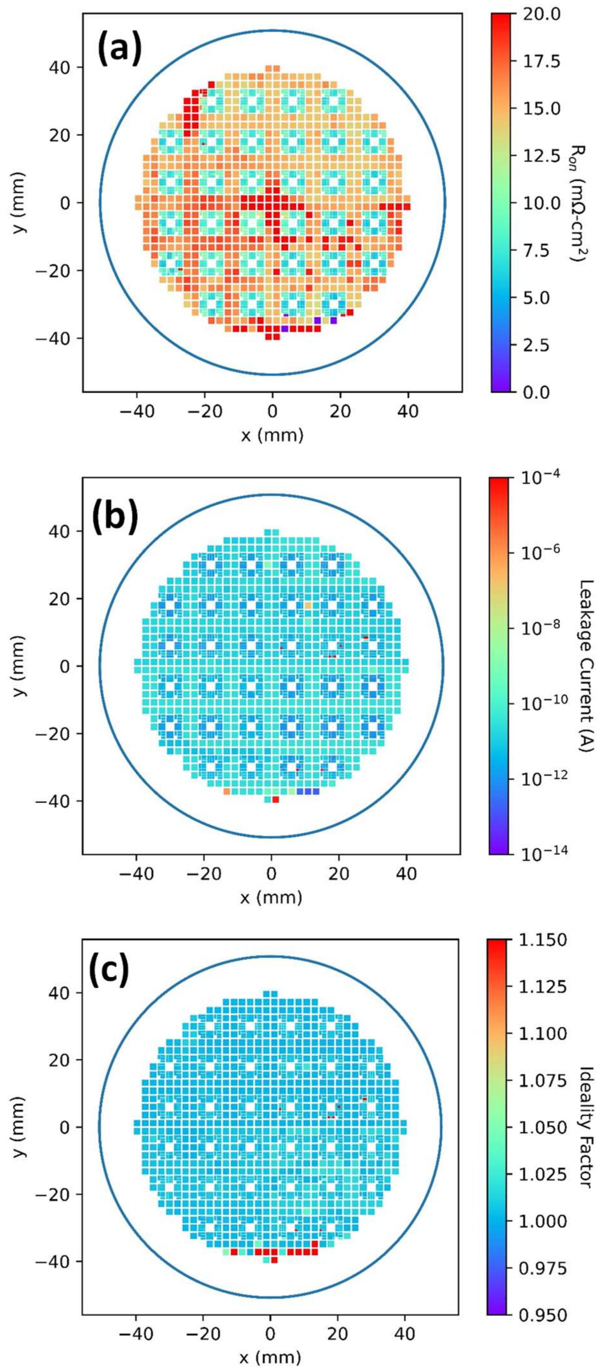

Fig. 2. Wafer-level automatic characterization of Schottky diodes: (a) on-resistance, (b) reverse leakage current at -10 V bias, (c) ideality factor. Large-area devices show up in orange and red color in (a). Wafer major flat is towards image bottom, with a 10 mm exclusion zone.

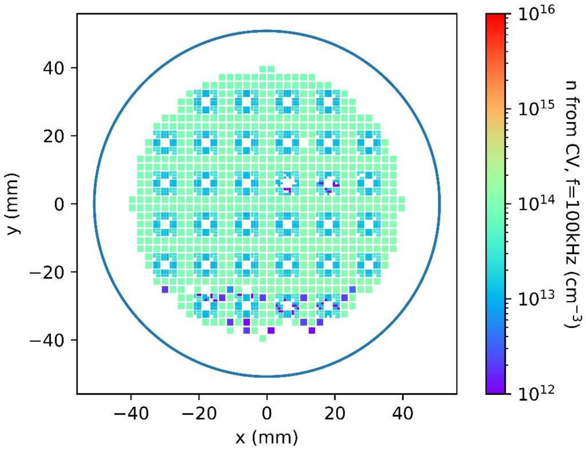

Fig. 3. Wafer-level automatic characterization of carrier concentration extracted from 100 kHz capacitance-voltage measurements. Wafer major flat is towards image bottom, with a 10 mm exclusion zone.

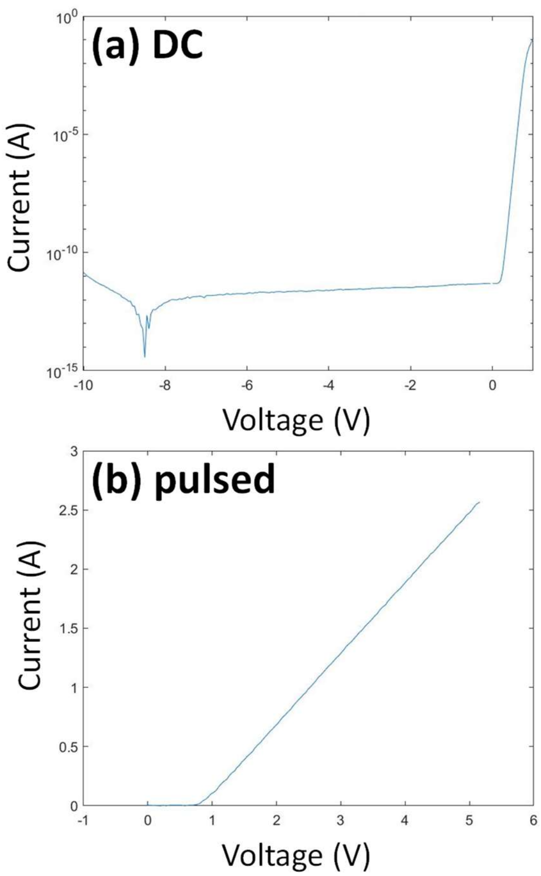

Fig. 4. Representative (a) direct-current (DC) and (b) pulsed I-V characteristics of Ga_2O_3 SBDs measured across the wafer.

4-probe alignment, compared to using a single probe for the DC measurements. However, reduced current density of about 250 A/cm^2 measured on some devices could be attributed either to epilayer thickness variation or potential thermal degradation under high forward bias power density.

CONCLUSIONS

For the first time, electrical and structural XRT characterization of β-Ga_2O_3 SBDs fabricated on commercial 100 mm epiwafers are reported. The results presented in this work further elucidate the need for wafer-level material and device characterization that is required for the commercialization of β-Ga_2O_3 power electronics [5, 6]. Further characterization will include reverse breakdown voltage, on-state hyperspectral electroluminescence imaging, and thermal characterization on selected devices based on these preliminary wafer-level results.

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ACRONYMS

EFG: Edge-defined, film-fed growth
MOCVD: metal organic chemical vapor deposition
HVPE: Halide vapor phase epitaxy
XRT: X-Ray Topography
C-V/I-V: capacitance-voltage/current-voltage
SBD: Schottky Barrier Diode