Nanocrystalline Diamond-Capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ Heterostructure Field-Effect Transistor

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ABSTRACT

In this work, we detail our fabrication process for incorporating a nanocrystalline diamond heat-spreading layer onto a β-Ga_2O_3 transistor as a candidate solution for top-side device-level thermal management for β-Ga_2O_3 devices. The resulting nanocrystalline diamond (NCD) capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistors show maximum DC power densities of ≥ 6.4 W/mm and a 40% decrease in the thermal resistance at the gate.

INTRODUCTION

The ultra-wide bandgap semiconductor, β-Gallium Oxide (β-Ga_2O_3), shows tremendous promise for next-generation power devices due to its high expected critical field strength of 6-8 MV/cm and the availability of high-quality single crystalline bulk substrates [1]. The low thermal conductivity (highest of 0.27 W (cm K)$^{-1}$ in [010] direction), though, is a well-known challenge for devices based on this semiconductor [1,2]. The development of high-performance β-Ga_2O_3-based power devices will require the incorporation of thermal management solutions [2]. Nanocrystalline diamond (NCD) can be used as an effective heat spreading layer for device-level thermal management [2] and has previously been incorporated into AlGaN/GaN devices [3,4]. Here, we demonstrate an NCD-capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistor (HFET) as a potential solution for top-side device-level thermal management for Ga_2O_3 power devices.

FABRICATION PROCESS

Figure 1 shows a cross-section schematic of the fabricated NCD-capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HFET. First, β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures were grown via ozone-assisted molecular beam epitaxy (O_3-MBE) and consisted of a 125 nm thick unintentionally doped (UID) Ga_2O_3 layer followed by a 28 nm thick $(Al_{0.19}Ga_{0.81})_2O_3$ (AlGaO) barrier layer on an Fe-doped (010) Ga_2O_3 substrate [5]. The AlGaO layer was delta-doped with Si ~3 nm above the interface. Both the AlGaO and

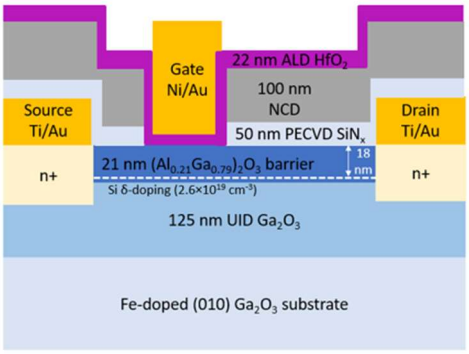

Fig. 1. Cross-section schematic of the β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HFET with NCD heat-spreading layer.

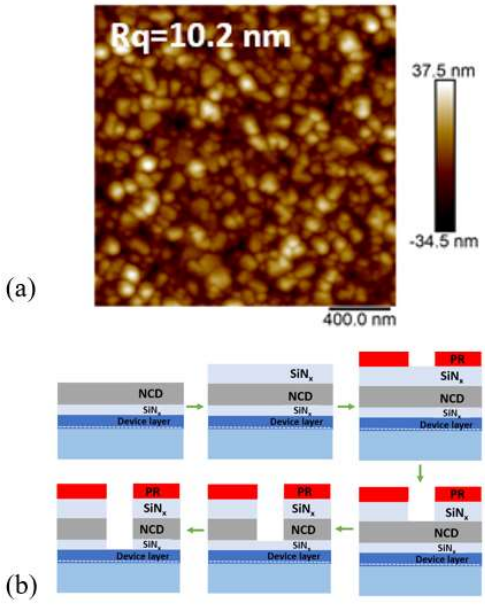

Fig. 2. (a) AFM of the NCD layer grown on the AlGaO/Ga_2O_3 heterostructure. Roughness was approximately 10.2 nm. (b) Process (clockwise) for removal of the SiN_x/NCD stack within the gate region.

the Ga_2O_3 layers were continuously grown in the MBE reactor, preventing unintentional Si from accumulating at the interface. Si ion implantation (activation anneal: 30 min, 925 °C in N_2) and e-beam evaporation of Ti/Au (anneal: 1 min, 470 °C in N_2) was used to form Ohmic source/drain contacts. The specific contact resistivity, mobility, sheet carrier concentration, and sheet resistance at room temperature were measured to be 4.3×10^{-4} Ω×cm^2, 54 cm^2/V·s, 1.26×10^{13} cm^{-2}, and 9.1 kΩ/□, respectively.

The next step in the fabrication process was to grow the NCD layer on the AlGaO/Ga_2O_3 heterostructure. The NCD layer is grown by microwave plasma enhanced CVD (MW-CVD), which requires the use of Hydrogen plasma. Hydrogen plasma has been shown to severely damage β-Ga_2O_3 and its alloys by etching deep pits into the surface. Because of this and also to provide a suitable surface for nanodiamond seed dispersion, a protective SiN_x barrier dielectric was deposited prior to NCD CVD. In this work, a ~50 nm SiN_x layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400ºC before the NCD growth process started. NCD nucleation sites were facilitated via a seeding method using detonation nanodiamond powder. The growth chamber was pre-treated with 200 sccm of H_2 at a temperature of 100 °C and a pressure of 15 torr for 1 h. NCD growth was then performed using a 1.5% CH_4/H_2 concentration at a temperature of 400 °C, pressure of 15 torr, and power of 800 W for ~6 h. The resulting NCD film thickness was ~100 nm and fig. 2 (a) shows an atomic force microscopy (AFM) image of the surface.

In order to finish the NCD-capped AlGaO/Ga_2O_3 HFET, the SiN_x/NCD stack must be removed from the gate region and the source/drain probing pads. An additional SiN_x layer was deposited by PECVD on top of the NCD film to act as a hard mask for the plasma etching process. After standard lithography, SF_6 (ICP 200 W, RF 50 W) was used to etch the top SiN_x mask. O_2 plasma with ICP 1000 W and RF 100 W was used to etch the NCD layer, followed by a second SF_6 etch to remove the SiN_x interlayer. This process is illustrated in Fig. 2 (b).

Lastly, a 22nm HfO_2 gate dielectric was deposited by atomic layer deposition, and the gate contacts were formed by lift-off of a 20/200 nm thick Ni/Au metal stack. The resulting device cross-section schematic is shown in Fig. 1. Figure 3 shows secondary electron microscopy (SEM) images of the gate regions of two of the devices, (a) and (b), that will be discuss in the results and (c) a region where the NCD film was fully removed. Thermal measurements were performed using a TMX Scientific T°Imager (532 nm, 100X objective); power dissipated was monitored using an oscilloscope, and the base temperature was maintained at 20 °C.

Results and Discussion

Two types of devices were investigated in this work. Figure 3 (a) shows an image of the gate for the first device, referred to as "MOS gate"; here, the SiN_x/NCD/SiN_x stack was fully etched from the gate region. Figure 4 (a) and (b) show the DC transfer and output characteristic for the "MOS gate" NCD-capped AlGaO HFET. A low on-state I_D (max of 6.8 mA/mm) was observed, which may be caused by SF_6-plasma damage to the AlGaO channel when removing the NCD/SiN_x film

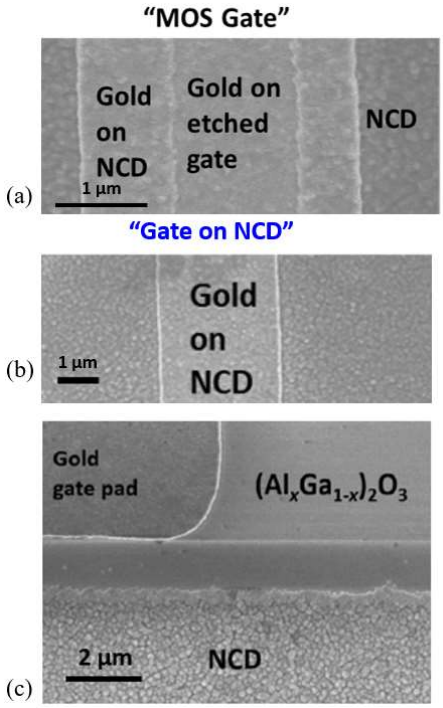

Fig. 3. SEM images of the gate for (a) the "MOS gate" and (b) the "Gate on NCD", and (c) an image showing the full removal of the SiN_x/NCD/SiN_x stack. Grains observed in the region labeled "gold on etched gate" in (a) is most likely from the evaporated gold, similar to the grains observed in (c) in the gold gate pad.

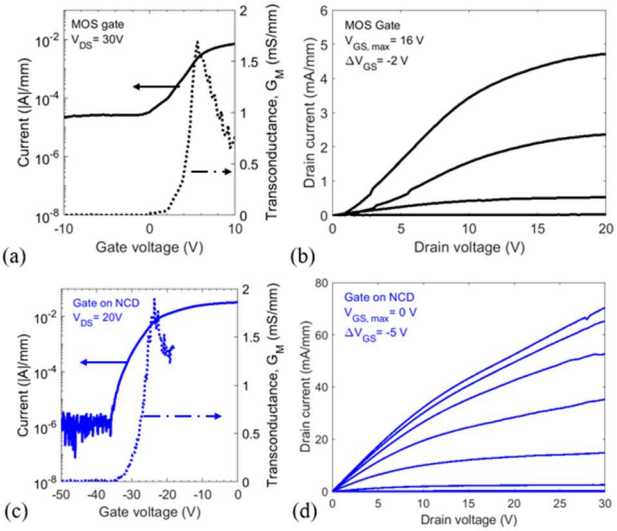

Fig. 1. DC transfer characteristics (a) and (c) and output characteristics (b) and (d) of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HFETs with the MOS gate (a, b) and with the gate on top of NCD (c, d). The devices both have the following geometry: L_{GS} = 2.5 µm, L_{GD} = 10 µm, and W_G = 75 µm.

from the gate region. The other device, called "Gate on NCD", is shown in fig. 3 (b) where the gate region was not fully etched before gate metal deposition. DC transfer and output measurements are shown in Fig. 4 (c) and (d) for this device which is still capped with NCD within the gate region. On-state I_D was over 10X higher when the AlGaO barrier in the gate region was not exposed to the O_2 plasma and SF_6 etches required to remove the NCD and SiN_x layers, respectively. While the SiN_x/NCD stack did protect the AlGaO active region from plasma damage, the large negative threshold voltage of the "Gate on NCD" device shows why the stack removal in the gate region is necessary. The process for removing the SiN_x interlayer will need to be optimize to achieve excellent device characteristics with the incorporation of this thermal management technique.

A maximum power density of ~6.4 W/mm, with a gate voltage of 0 V, was measured before catastrophic failure occurred on the "Gate on NCD" device. Figure 5 shows thermoreflectance images of (a) a reference uncapped device and (b) the "Gate on NCD" HFET. The power density of both devices is ~ 1.5 W/mm. The device without NCD showed a temperature rise at the gate of ~73 K, while the NCD-capped device only saw an increase of ~35 K. These images show that the NCD heat-spreading layer has great potential as a thermal management technique for β-Ga_2O_3 devices.

CONCLUSION

Self-heating in β-Ga_2O_3 devices due to the material's low thermal conductivity is a significant issue that must be mitigated in the development of these power devices. Here, we demonstrated a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistor with a nanocrystalline diamond heat-spreading capping layer. The NCD film was able to significantly reduce the temperature rise observed at the gate at a given power density. A maximum power density of 6.4 W/mm was reached with the NCD-capped device. Plasma damage from the removal of the SiN_x/NCD stack within the gate region was shown to have a negative impact on the device characteristics. Optimization of the SiN_x/NCD etch within the gate region will be required to maintain good device performance. Further improvements to the NCD layer (thicker NCD films, higher growth temperatures, etc.) will lead to this being an excellent thermal management technique for Ga_2O_3-based power devices.

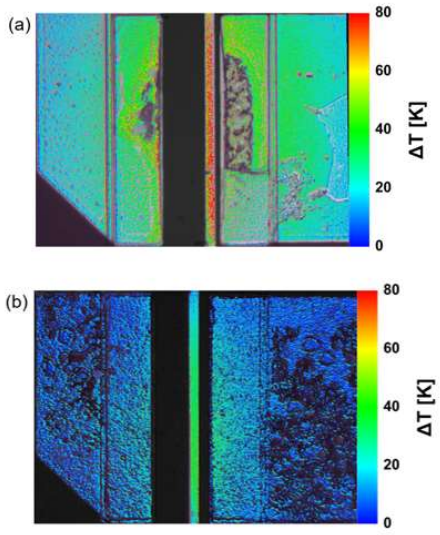

Fig. 5. Thermoreflectance images of a reference uncapped device (a) and the "Gate on NCD" HFET (b), both at a power density of ~1.5 W/mm.

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ACRONYMS

AlGaO: β-$(Al_xGa_{1-x})_2O_3$
HFET: Heterostructure field-effect transistor
MW-CVD: microwave plasma enhanced chemical vapor deposition
NCD: Nanocrystalline diamond