Sonic Lift-off (SLO) to Enable Substrate Reuse and Lower Manufacturing Cost

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Abstract

Substrate costs currently dominate the cost of wide bandgap (WBG) device manufacturing, limiting more rapid adoption of next generation devices. Sonic Lift-off (SLO) technology offers a novel pathway to reduce such costs by replacing wasteful mechanical backgrinding and enabling substrate reuse through an acoustically controlled device lift-off process. This study focuses on the methods and application of SLO on WBG materials such as GaAs, GaN and SiC. Surface analysis shows superior surface quality of the substrate after SLO without introducing sub-surface damage and defects.

INTRODUCTION

The wide bandgap (WBG) device market is expected to grow dramatically driven by mobility, clean electrification, and communication applications [1]. WBG device manufacturers are looking for solutions to lower the cost of WBG devices to capitalize on the superior performance of WBG materials in terms of higher voltage and frequency operation, lower switching losses, and higher thermal load capability compared to Silicon devices. Substrate costs currently dominate the costs of WBG device manufacturing, representing the single highest cost item for most of the next generation WBG applications.

Today's standard manufacturing processes for WBG-based devices typically require thinned devices, achieved by mechanically backgrinding, where the majority of the substrate material is wasted, leaving behind a high performing device. Substrate materials such as SiC, GaN and GaAs can consume up to fifty percent or more of total device manufacturing costs, depending on the specific application [2,3].

Crystal Sonic's Sonic Lift-off (SLO) technology provides a pathway for multiple wafer reuses, reducing the substrate cost proportionally with the number of reuses. SLO offers unique advantages over legacy thinning technologies (backgrinding) and other lift-off technologies under development in terms of wafer surface quality for reuse and loss-less device lift-off from the substrate.

SONIC LIFT-OFF (SLO) DESCRIPTION

SLO is a novel patented technology developed at Crystal Sonic, Inc. SLO uses the combination of initiating a crack front at one side of the wafer, pre-stressing of the substrate via a thermal gradient with a removable stressor to define the lift-off plane below the surface, and controlled application of acoustic pulses that guides a crack front through such plane at a controlled speed. This results in a separation of the device layer from its substrate, leaving the substrate surface ready for reprocessing the next device layer after no or minimal processing (see Fig. 1b). SLO has been demonstrated successfully on Si, GaAs, SiC, GaN and AlN.

The stressor layer has a different coefficient of thermal expansion (CTE) compared to the substrate which leads to thermally induced stress within the substrate when the system

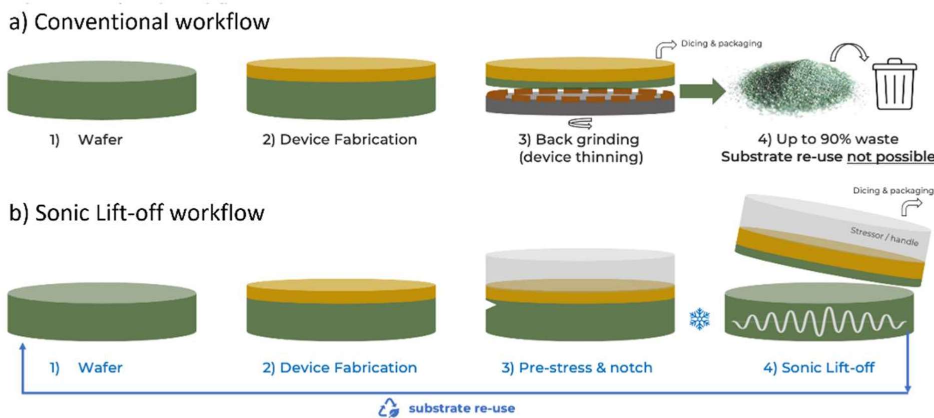

Fig. 1. a) Conventional device thinning process via mechanical back-grinding, and b) Sonic Lift-off process, splitting a fabricated device from the substrate via acoustic energy allowing for substrate reuse with minimal processing.

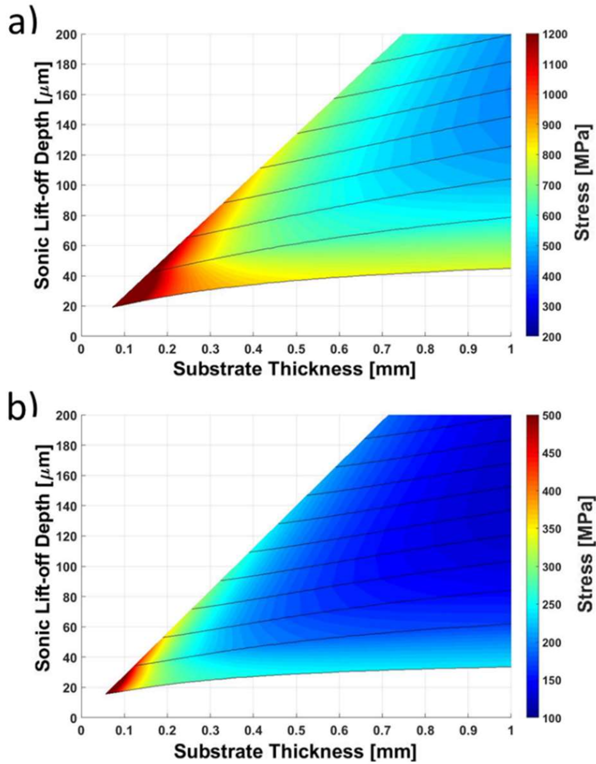

Fig. 2. Spalling Parameter Surface Plot (SP2) for lift-off applications on a) Silicon Carbide and b) Gallium Nitride substrates. Each isoline represents the Sonic Lift-off depth solutions for one stressor thickness. The contour map depicts the critical stress needed to propagate a crack for each combination of stressor and substrate thickness.

is cooled down. The thickness of the SLO layer primarily depends on the thickness and material properties of the stressor layer. The Spalling Parameter Surface Plot (SP2) is a framework capable of evaluating and predicting the thickness of the SLO layer for various material's properties and process parameters (substrate thickness and required stress) [4]. Figure 2 shows the SP2 for GaN and SiC substrate materials. The isolines depict a specific stressor thickness while the contour plot represents the stress required to propagate the crack under the specific combinations of stressor thickness and substrate thickness. The SP2 changes for each combination of stressor and substrate materials. Therefore, the SP2 aids with the selection of the most optimal stressor material and its thickness to achieve a desired SLO depth for a range of substrate materials and thicknesses.

Characterization of Sonic Lift-Off Surfaces

Conventional backgrinding introduces cracks and >10µm of subsurface damage due to the stresses introduces during the process [5]. Controlled and spontaneous spalling similarly utilize the mismatch in the coefficient of thermal expansion between two materials to propagate a crack through the material. However, the lack of acoustic waves to control the crack velocity leads to poor surface quality with large facets and roughness (Fig. 3a). Controlling the energy at the crack front during crack propagation permits reducing the crack velocity which has been shown to reduce surface roughness [6]. During SLO, acoustic pulses control the crack velocity leaving behind low roughness surfaces <1µm (Fig.3b). The quality of the surface allows for substrate reuse with minimal or no subsequent processing.

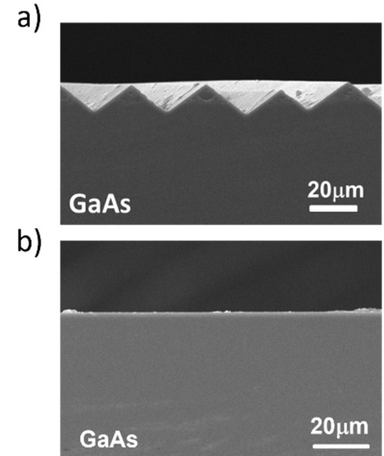

Fig. 3. Cross section SEM comparing surface quality for a) controlled/spontaneous spalling and b) Sonic Lift-off in GaAs from [7].

Wide bandgap wafers are processed with an offcut angle to improve the growth of the epitaxial layer and final performance of the devices [8]. Therefore, it is vital to retain the offcut angle of the original wafer after SLO to be capable of reusing the substrates. Figure 4a shows the cross-section SEM of a 4° offcut 4H-SiC substrate after spontaneous spalling. The crack was not controlled via acoustic waves and lead to large terraces. These terraces have a 4° angle with respect to the initial substrate surface following the (0001) plane. By reducing the crack velocity, the crack propagation is contained within the plane parallel to the initial substrate surface without deviating into other less energetically

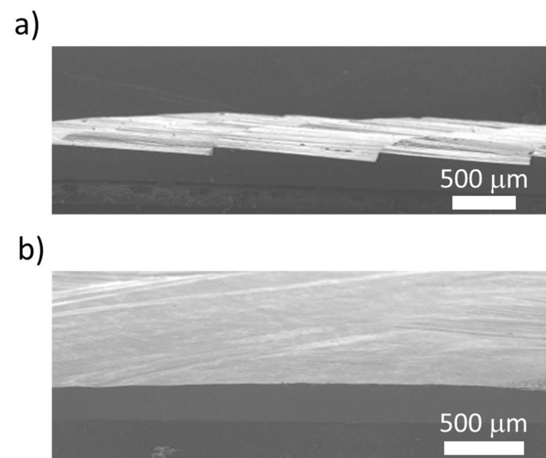

Fig. 4. Cross section SEM comparing the surface of 4° offcut 4H-SiC substrates after a) spontaneous spalling and b) Sonic Lift-off. Terraces in a) follow the (0001) plane in SiC.

favorable planes such as the (0001) plane. Figure 4b shows the substrate surface after SLO where the terraces are not present, and the original 4° offcut angle of the wafer is maintained.

The quality of the reused substrate is paramount to fabricate high-performing devices. X-ray topography (XRT) is a common method to inspect cracks in semiconductor wafers with a resolution of <10μm [9]. In XRT images the darkest areas appear in those areas with microcracks formation, and the different tones of greys show slight differences in thickness within the sample. Figure 5a shows an XRT image for a pristine GaAs wafer showing no dark areas regions which suggests the absence of microcracks in the initial substrate. Figure 5b depicts the substrate after SLO. The absence of dark areas are further evidence that subsurface microcracks are not generated during the process, something that is common with other techniques. Figure 5c depicts the substrate after spontaneous spalling (no acoustic control) where clear dark areas are seen throughout. The histogram of the pixel count for all samples is shown in Fig. 5d. The SLO substrates produce similar surface quality as the original substrates while spontaneous spalling creates microcracks in the substrate. As shown with the SEM and XRT analysis the SLO process does not introduce detectable sub-surface damage and defects.

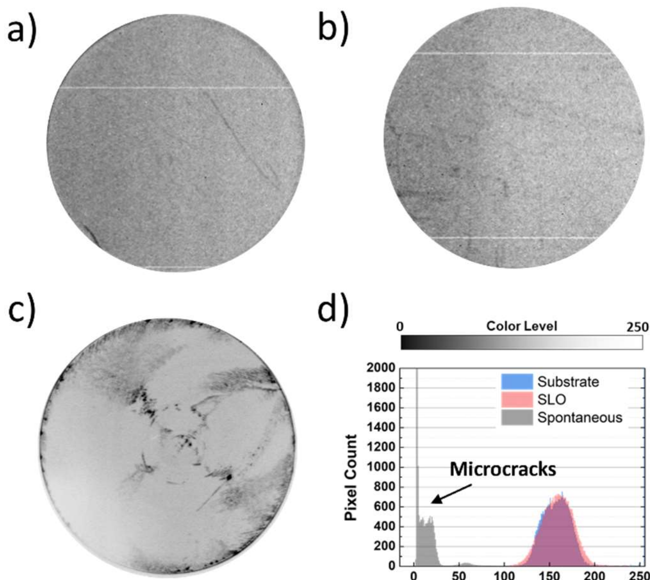

Figure 5. X-Ray Topography Images of GaAs for a) a pristine substrate, b) substrate after Sonic Lift-off and c) after spontaneous spalling. Dark regions represent microcracks formation. d) The histograms of the pixel count for each sample show microcracks formation after spontaneous spalling and no microcrack formation after the SLO process.

CONCLUSIONS

The Sonic Lift-off (SLO) process allows device separation from a host substrate, leaving the substrate wafer available for multiple reuses. SLO leaves behind high quality wafer surfaces for reuse and device lift-off from the parent wafer. Surface characterization with SEM and XRT shows the lack of defects in the substrate after SLO. SLO technology has great potential to reduce the cost of WBG devices manufacturing, thus accelerating the transition beyond Si-based power-, optoelectronics-, and RF devices towards WBG-based devices.

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ACRONYMS

WBG: Wide bandgap
SLO: Sonic Lift-off
SP2: Spalling Parameter Surface Plot
SEM: Scanning Electron Microscope
GaAs: Gallium Arsenide
SiC: Silicon Carbide
GaN: Gallium Nitride
AlN: Aluminum Nitride