Short-circuit Failure Mechanisms of 1.2 kV 4H-SiC MOSFETs under Different Drain Voltages

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Abstract

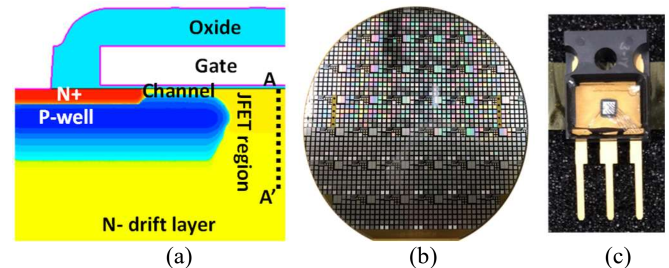
Short-circuit failure mechanisms of 1.2 kV 4H-SiC MOSFETs were demonstrated based on the power dissipation. In order to investigate the short-circuit failure, different drain voltages were applied under short-circuit conditions. To fairly compare the short-circuit failure mechanisms, identical 1.2 kV 4H-SiC MOSFETs fabricated on 6-inch wafer were utilized. At high power dissipation, which results in high junction temperatures, the short-circuit failure of the MOSFETs was governed by the high leakage current through the channel region. At low power dissipation, the MOSFETs failed due to gate-source failure as the MOSFETs were exposed to high temperatures for a long time, resulting in damage to the oxide. To further understand the short-circuit characteristics of MOSFETs under different drain voltages, non-isothermal simulations were conducted.

INTRODUCTION

Since power devices based on Si have reached their limit in power loss reduction, wide bandgap semiconductor materials such as 4H-SiC have gained traction to replace their Si counterparts due to their superior material properties; high critical electric field, high electron mobility, and high thermal conductivity. Hence, 4H-SiC enables a much thinner and higher doped drift layer, significantly reducing the drift resistance of the power device. On top of that, the unipolar structure, MOSFET, can be utilized, contributing to a reduction in the switching loss [1].

4H-SiC power MOSFETs with superior static characteristics have been developed. The reduction of $R_{on,sp}$ was achieved by reducing the channel resistance [2][3] and optimizing the device cell structure [4]. However, 4H-SiC MOSFETs have a critical concern during SC conditions due to the high current density and high electric field across the drift region [5]. 1.2 kV 4H-SiC MOSFETs have extremely high temperatures produced by self-heating, causing poor SC characteristics. The high temperatures under SC conditions can result in different failure mechanisms; parasitic NPN transistor latch up [6], gate oxide degradation [7][8], cracks in the ILD [9], and molten Al metallization [10].

In this paper, the short-circuit failure mechanisms of 1.2 kV 4H-SiC MOSFETs were studied by applying different drain voltages. Different SCWT and different SC failure mechanisms were obtained depending on power dissipation. To fairly compare the effect of power dissipation on 4H-SiC MOSFETs under SC conditions, 1.2 kV accumulation mode channel SiC MOSFETs were fabricated on the same, 6-inch wafer. In order to understand the SC failure mechanisms, non-isothermal device simulations were conducted as well.



(a) (b) (c)

Fig. 1. (a) Cross-sectional view of 1.2 kV 4H-SiC MOSFETs. (b) Fabricated SiC MOSFETs on 6-inch SiC wafer. (c) Packaged SiC MOSFETs.

FABRICATION

The devices were fabricated by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, using the same base process line [4]. A 10 µm thick drift layer with N-type doping concentration of 8×10^{15} cm^{-3} on 6-inch, N+ 4H-SiC substrate was used for the fabrication of proposed 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were used to form P-well/P+ body/JTE, and JFET/N+ source, respectively. After all implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by ultrathin (2 nm) thermal oxide and 48 nm of deposited oxide, followed by a POA in N_2O ambient. The N-type polysilicon was deposited and patterned for the formation of the gate. BPSG was deposited as ILD, then patterned and etched to make ohmic contact regions. Ni was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA at 965 °C for 2 mins. Ni was deposited on the backside and then followed by the same RTA process. A 4 µm thick Ti/TiN/Al stack was deposited for the source and gate metal. Silicon nitride and polyimide were used for the passivation. Finally, a solderable metal stack was deposited on the backside.

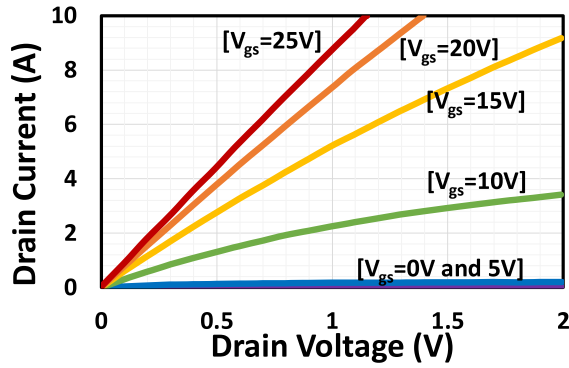
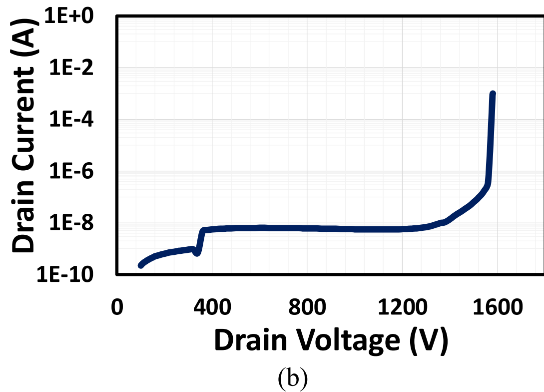


Fig. 2. Measured output characteristics of 1.2 kV 4H-SiC MOSFETs.



(b)

Fig. 3. Measured blocking characteristics of 1.2 kV 4H-SiC MOSFETs.

RESULTS

Figure 1 (a) shows the cross-sectional view of the 1.2 kV SiC MOSFETs which were fabricated on 6-inch SiC wafer as shown in Fig. 1 (b) and packaged in TO-247 cases as shown in Fig. 1 (c). The 4H-SiC epi-layer is designed to be 8×10^{15} cm^{-3} doped and 10 μm thick for the 1.2 kV MOSFETs. To achieve high channel mobility, an accumulation mode channel was used. A JFET implantation was also applied to reduce the JFET resistance.

Figure 2 shows the typically measured output characteristics of the fabricated 1.2 kV 4H-SiC MOSFETs. Figure 3 shows the measured blocking characteristics of the fabricated 1.2 kV 4H-SiC MOSFETs. Due to the well-optimized cell structure and edge termination, high breakdown voltages with low leakage current were achieved.

Figure 4 (a) shows measured short-circuit characteristics of the MOSFETs with different drain voltages: an identical gate voltage of 20 V and gate resistor of 20 ohm were used. The drain voltage (400 V, 600 V, or 800V) with gate voltage of 0 V was applied, and then gate voltage of 20 V was applied for the short-circuit conditions. Low drain voltages provide long SCWT due to low power dissipation, resulting in a low junction temperature from self-heating. Moreover, different failure mechanisms were obtained under a drain voltage of 400 V: the MOSFETs failed due to the issue with the gate under a drain voltage of 400 V. Unlike drain voltage of 400 V, MOSFETs failed during the measurement under 600 V and 800 V due to the high junction temperatures.

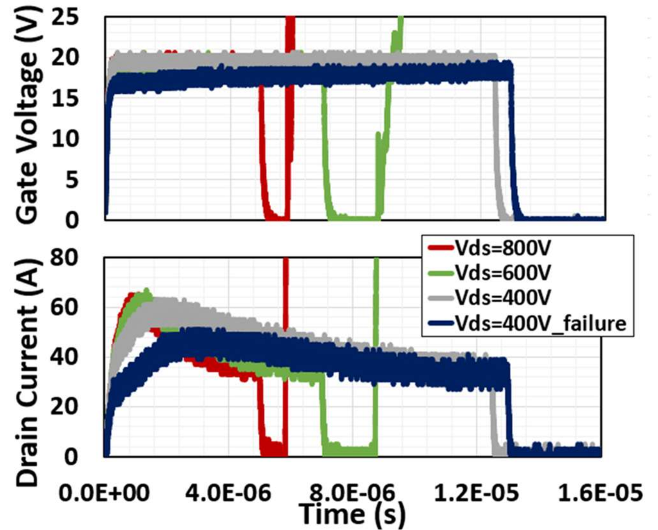
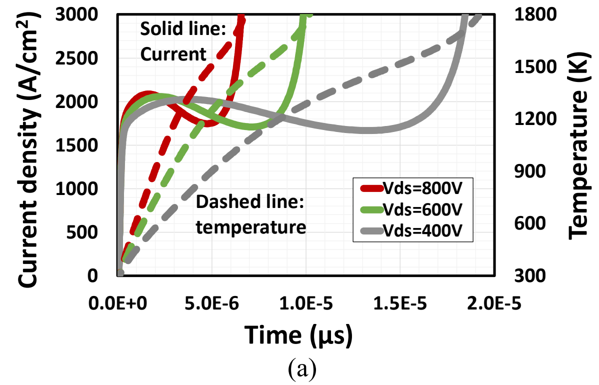
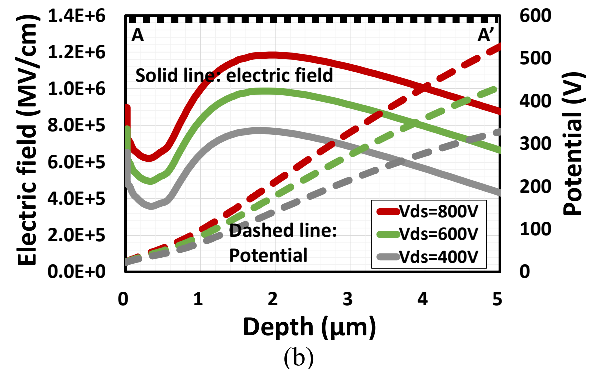


Fig. 4. Measured short-circuit characteristics of 1.2 kV 4H-SiC MOSFETs with different drain voltages.



(a)



(b)

Fig. 5. (a) Simulated drain current and maximum junction temperatures of 1.2 kV 4H-SiC MOSFETs with different drain voltages under short-circuit conditions. (b) Simulated electric field and electrostatic potential (A-A' shown in Fig. 1 (a))

In order to examine the short-circuit failure mechanism of the 1.2 kV 4H-SiC MOSFETs, non-isothermal Sentaurus 2D-simulations were conducted. Figure 5 (a) shows simulated drain current and maximum junction temperatures of 1.2 kV 4H-SiC MOSFETs with different drain voltages under SC

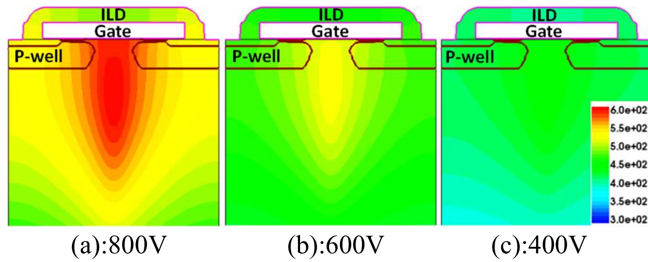


Fig. 6. Simulated cross-sectional view of temperature distribution of MOSFETs under drain voltage of (a) 800 V, (b) 600 V, and 400 V at time of 1μs.

conditions. Due to well-optimized simulation models, a similar trend to the experimental results is seen in the simulation. Low drain voltages provide long SCWT due to the low junction temperature. Heat generation is directly related to current density and electric field distribution across the MOSFETs [5]. With the increase of drain voltages, the electric field in the JFET region increases as shown in Fig. 5 (b). This is due to the high potential as shown in Fig. 5 (b).

Figure 6 shows the simulated cross-sectional view of the temperature distribution in the MOSFETs at a time of 1 μs. Due to the high electric field, a drain voltage of 800 V shows the highest temperature distribution. Moreover, the maximum temperature in the MOSFETs occurs in the middle of the JFET region.

To examine the failure mechanisms, the simulated cross-sectional view of the drain current and the temperature distributions of the MOSFET when the device fails is shown in Fig. 7. The MOSFETs failed due to the high leakage current through the channel region under a drain voltage of 800 V. Due to the relatively low potential barrier in the channel region, the high leakage current flows through the channel region at high temperatures. When the maximum junction temperature of the MOSFET reaches a temperature of approximately 1600 K, the MOSFET fails due to the high leakage current through the channel region regardless of the drain voltage.

Since it is difficult to reveal the SC failure mechanism, except for the high leakage current through the channel in the simulation, short-circuit failure mechanisms were examined by comparing the experimental and simulated results. Under drain voltages of 800 V and 600 V, the experimental and simulated SCWT are well matched, which means that the MOSFETs failed due to the high leakage current through the channel region. However, the simulated SCWT, which is governed by the high leakage current, is longer than the measured SCWT under a drain voltage of 400 V. In experimental results, under a drain voltage of 400 V, the MOSFETs failed not due to the high leakage current, but due to another failure mechanism. From the not fully applied gate voltage in the experimental results, the failure is due to the problem with the gate-source; gate oxide or ILD. In order to obtain the exact SCWT of the MOSFETs, the gate pulse width was increased by 0.5 μs until that single device failed as shown in Fig. 8. As a result, the damage to the gate oxide and

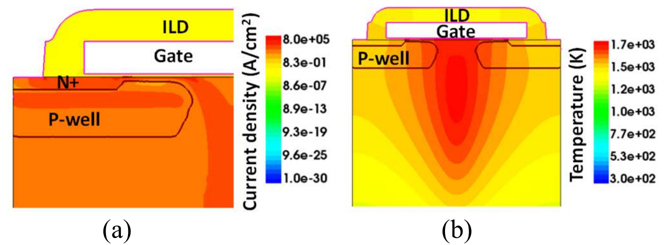


Fig. 7. (a) Simulated cross-sectional view of (a) drain current density and (b) temperature distribution of MOSFETs under drain voltage 800 V when the device is failure.

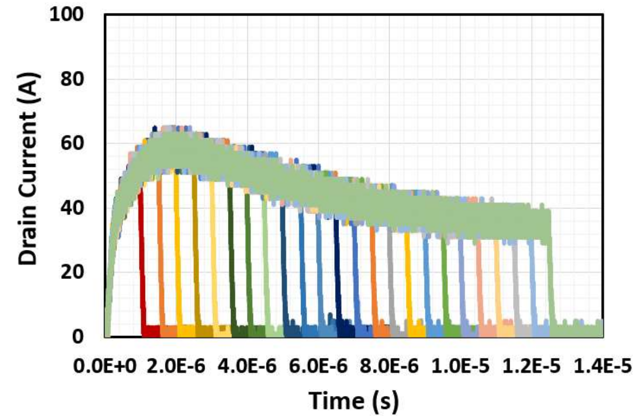


Fig. 8. Measured drain current of fabricated MOSFETs with different gate pulses under short-circuit conditions.

ILD was more accumulated in the MOSFETs having long SCWT. Moreover, the long SC condition degrades the gate oxide and ILD during the one measurement itself. When the gate oxide is degraded by FN tunneling and PF emission leakage currents during SC conditions, the applied gate voltages decrease by the leakage currents [7],[8]. However, there is no change in the gate voltage during the SC measurement, which mean that gate oxide is not damaged by FN tunneling and PF emission. Hence, the gate and source issue would be from a physical crack in the ILD.

It is discovered that depending on the power dissipation, different SC failure mechanisms occur. However, during SC conditions with high drain voltages, the gate oxide and ILD also degrade due to the high junction temperature even though the device mainly fails due to the high leakage current through the channel region. Hence, the quality of gate oxide and ILD need to be improved to further improve SC characteristics.

CONCLUSIONS

1.2 kV SiC MOSFETs were fabricated and evaluated to examine different short-circuit failure mechanisms. By applying different drain voltages, different SCWT and failure mechanisms were obtained. When high drain voltage is applied, the junction temperature abruptly increases, resulting in failure induced by the high leakage current through the channel region. However, when the MOSFETs are exposed to

high temperature, for a long time, the SiO_2 becomes damaged, causing gate-source issues.

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REFERENCES

[1] J. W. Palmour *et al.*, "Silicon Carbide Power MOSFETs: Breakthrough Performance from 900 V up to 15 kV," in *Proc. 26th Int. Symp. Power Semiconductor Devices ICs*, Jun. 2014, pp. 79-82. doi: 10.1109/ISPSD.2014.6855980.

[2] G. Y. Chung *et al.*, "Improved Inversion Channel Mobility for 4H-SiC MOSFETs Following High Temperature Anneals in Nitric Oxide," *IEEE Electron Device Letters*, vol. 22, no. 4, pp. 176-178, Apr. 2001. DOI: 10.1109/55.915604.

[3] W. Sung *et al.*, "A comparative study of channel designs for SiC MOSFETs: Accumulation mode channel vs. inversion mode channel," in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, May 28-June 1, 2017, pp. 375–378. DOI: 10.23919/ISPSD.2017.7988996.

[4] D. Kim *et al.*, "An Inclusive Structural Analysis on the Design of 1.2kV 4H-SiC Planar MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 804 - 812, Sep. 2021. DOI: 10.1109/JEDS.2021.3109605

[5] J. Sun *et al*., "Comparison and analysis of short circuit capability of 1200V single-chip SiC MOSFET and Si IGBT," *in 2016 13th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS)*, Jan. 2016, pp. 42–45. doi: 10.1109/IFWS.2016.7803752.

[6] Z. Wang *et al.*, "Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs," *IEEE Tran. on Power Elec.*, vol. 31, no. 2, pp. 1555-1566, Feb. 2016. DOI: 10.1109/TPEL.2015.2416358

[7] T.-T. Nguyen *et al.*, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2445–2455, May 2015, doi: 10.1109/TPEL.2014.2353417.

[8] M. Sometani *et al.*, "Temperature-dependent analysis of conduction mechanism of leakage current in thermally grown oxide on 4H-SiC," *Journal of Applied Physics*, vol. 117, no. 2, p. 024505, Jan. 2015, doi: 10.1063/1.4905916.

[9] P. D. Reigosa *et al.*, "Effect of short-circuit stress on the degradation of the SiO2 dielectric in SiC power MOSFETs," *Microelectronics Reliability*, vol. 88–90, pp. 577–583, Sep. 2018, doi: 10.1016/j.microrel.2018.07.144.

[10] K. Han *et al.*, "New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs," *in 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 108–113. doi: 10.1109/WiPDA.2018.8569178.

ACRONYMS

Si: Silicon
SiC: Silicon Carbide
MOSFET: Metal–Oxide–Semiconductor Field-Effect Transistor
Ron,sp: Specific On-resistance
SC: Short-Circuit
SCWT: Short-Circuit Withstand Time
JTE: Junction Termination Extension
POA: Post Oxidation Anneal
BPSG: Borophosphosilicate glass
ILD: Interlayer Dielectric
RTA: Rapid Thermal Annealing
SEM: Scanning Electron Microscope
FN: Fowler–Nordheim
PF: Poole-Frenkel