Reliability assessment of HTOL stressed VCSELs with camera-based beam profilers

Hao-Tien Cheng[1,2], Taixian Zhang[3], Yun-Cheng Yang[1,2], Te-Hua Liu[2,4], Chao-Hsin Wu[1,2,4,5,*]
[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
[2]Center for Quantum Science and Engineering, National Taiwan University, Taipei, Taiwan
[3]LiVe Optronics, Taipei, Taiwan
[4]Graduate School of Advanced Technology, National Taiwan University, Taipei, Taiwan
[5]Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan
Email: chaohsinwu@ntu.edu.tw

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Abstract

This paper presents a beam profiling technique to study vertical-cavity surface-emitting laser chips subjected to high-temperature operating life (HTOL) stress tests. The HTOL-stressed VCSEL chips are comprehensively analyzed to obtain their light-current-voltage curves, near-field beam profiles, and cross-sectional scanning electron microscope images. This beam profiling technique could be helpful for reliability studies and quality assurance of VCSEL chips before final product shipment.

INTRODUCTION

The backbone of the modern Internet is now made entirely of optical technology, which has completely replaced traditional copper wires for the interchange of information around the globe. Vertical-cavity surface-emitting lasers (VCSELs) have high efficiencies, high modulation bandwidths, and compact sizes and have been the first choice for transceiver deployment in optical interconnect applications [1]. Meanwhile, over the past few years, state-of-the-art 850-nm VCSELs have demonstrated beyond 30 GHz bandwidths and enabled exceeding 100 Gbps with individual VCSEL links [2].

To ensure minimal downtime in commercial and industrial applications, the endurance and reliability of VCSELs have been of top interest for device designers to ensure resilience to degradation due to operation in harsh working environments [3]. Optimizing the device lifetime, including tuning the active region and distributed Bragg reflector (DBR) stack designs, takes much work to ensure minimal performance deterioration at higher temperatures. The epitaxial wafer growth recipes have been continuously optimized to minimize device early failures due to defects, delamination, and epi-related issues. Various methods have been proposed to improve the reliability of VCSELs, namely polyimide passivation, atomic layer deposition passivation, and implantation [4]. Besides, the back-end production process such as packaging and sorting may induce charges to the devices that may cause electrostatic discharge (ESD) during the operation of the devices, causing premature device failures [5].

High temperature operation life (HTOL) test is employed to determine the long-term effects of bias and temperature stress on semiconductor devices. It is primarily used for evaluating device reliability and accelerates the simulation of the devices' operating conditions [6]. The HTOL simulates the operation of the devices' operating conditions in an accelerated manner and is primarily used to assess the reliability of the devices. HTOL is also commonly applied to evaluate the reliability, operation lifetime, and mean time to failure (MTTF) of various integrated circuits and optoelectronic components [7].

It is hard to ascertain the zone of the failing region and the root causes for the failure of semiconductor devices. The industry has been using conventional transmission electron microscopy (CTEM) and plan-view transmission electron microscopy (PV TEM) to study the dark line defects (DLDs) and corrosion-based defects in VCSELs. One thing that interests us is that the emitting feature of VCSELs allows using camera-based beam profilers to study the emission characteristics to ascertain the failing regions. It may be an efficient, quick, and affordable method to study the cause and the zone of weakness in devices and eventually for improving modern VCSEL manufacturing.

In this study, we perform a comprehensive analysis on HTOL-stressed VCSELs using light-current-voltage (L-I-V) characteristics, beam profiling, focused ion beam (FIB), and CTEM to study the degradation characteristics of datacom 850-nm VCSEL at elevated temperatures. A beam profiling technique on HTOL-stressed VCSELs is proposed to study the effect of the accelerated aging to the electro-optical performance of VCSEL devices. We hope our investigation could be a useful reference for reliability studies, and product pre-shipment environmental stress screening (ESS) in

VCSEL manufacturing plants. Near-field beam profiling can be useful to find root causes of device failures and lower the defect parts per-million (DPPM) for VCSEL product shipments.

METHODS

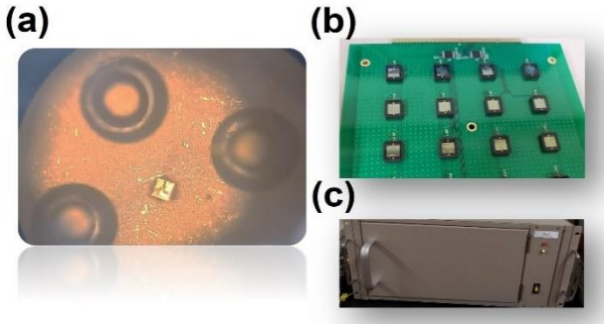

Fig. 1. HTOL stress tester setup of (a) a TO-46 packaged VCSEL device, (b) photodetectors on the tester boards, and (c) the HTOL stress tester.

VCSEL chips were packaged in TO-46 packages and put into an HTOL stress tester which consists of a thermally controlled chamber for high-temperature accelerated aging, as illustrated in Fig. 1. The HTOL tester consists of multi-channel current sources to provide currents to devices and silicon photodetectors to characterize the optical emission power of individual devices.

The HTOL tester consists of large-area photodetectors to monitor the real-time optical emission power of individual VCSELs during the HTOL stress test. Thermosensors and large heat spreaders were placed near the TO-46 packaged devices to ensure even heating is applied. HTOL-stressed devices are put into further analysis to investigate their failure mechanisms.

A homemade beam profiler is built with a microscopic system with an installed Spiricon SP928 compact beam profiler to capture the near-field beam profile of the HTOL-stressed VCSEL chips [8]. They are also sent to CTEM to observe any manufacturing-related issues or defect formation that may cause the early device failure.

RESULTS

(1) HTOL stressed aging

The stress test temperatures and currents were configured as 100 ° C and 7.5 mA for the HTOL stress aging for over 2000 hours. The HTOL stress test conditions are selected to study the random device failures that could be due to "infant" failures. The normalized optical versus stressed duration is plot in Fig. 2. After the 2,000 hours HTOL stress duration, most of the devices showed little sign of degradation except two devices (Device B and D) which failed at ~150 hours. We suspect these "infant" failures were victims of either ESD damage, process imperfections, or package damage.

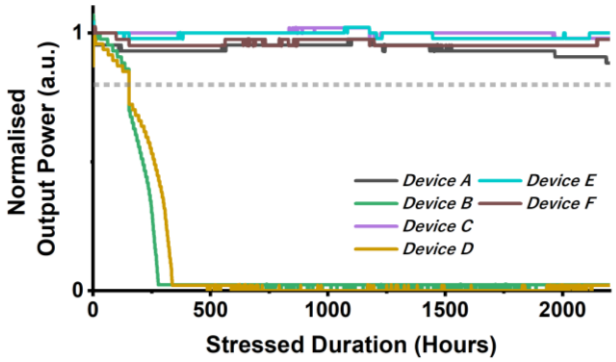

Fig. 2. Normalized emission power at different stress duration at 100 ˚C and 7.5 mA.

(2) L-I-V characteristics

The L-I-V characteristics of four HTOL-stressed devices are measured and compared in Fig. 3. The two failed devices exhibit significantly higher threshold currents and weaker optical output powers. The degraded chips showed increased lasing thresholds and slightly declined optical output powers. Meanwhile, the four chips showed similar I-V characteristics at forward-biased conditions. Suggesting that forward I-V characteristics may not be an effective method to screen out the failed or degraded VCSEL chips. Therefore, we require other methods to differentiate the HTOL-passed, HTOL-degraded, and HTOL-failed VCSEL chips.

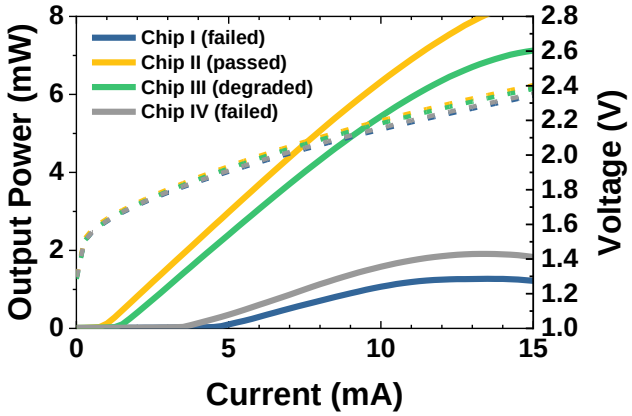

Fig. 3. L-I-V curves of HTOL-stressed chip after 2500 hours of 100 ˚C and 7.5 mA HTOL stress.

(3) Beam profiling

Similar studies have been performed to investigate the various changes in the emission beam characteristics of the failed devices, and near-field imaging could be a proven rapid method to inspect possible degradation in VCSEL emitters [9].

In Fig. 4, the HTOL-passed VCSEL device shows a Gaussian-like beam profile, as most of the power may be emitted in the fundamental mode. The HTOL-failed chip shows a dimmer emission in the central region and dark zones in the beam profile (white-dotted-circled regions). The beam profile's uneven distribution is likely due to damage, melting, or delamination in the current window apertures [10] [11]. One-dimensional power distribution plots of the beam profile images are shown in the lower subfigures of Fig. 4, the HTOL-failed chip showed uneven shifting of the optical power intensity (the power shift to the right-top corner of the VCSEL beam as shown in the two-dimensional beam profile pattern).

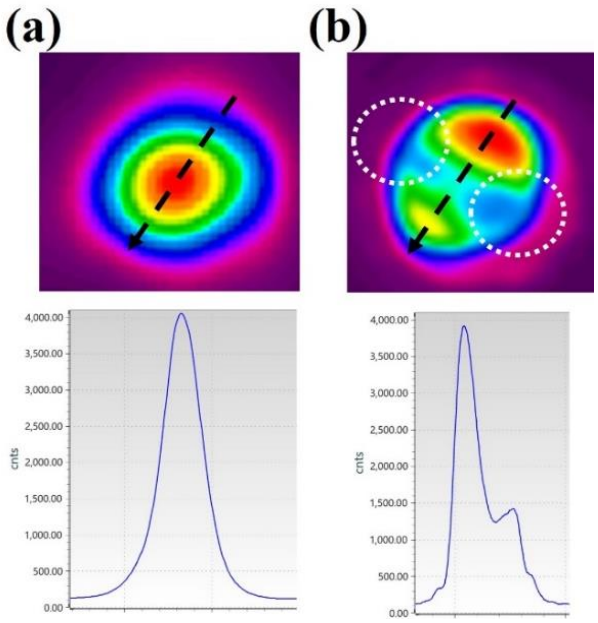

Fig. 4. Near-field beam profile pattern of two HTOL-stressed chips (a) an HTOL-passed device and (b) an HTOL-failed device.

(4) Material analysis

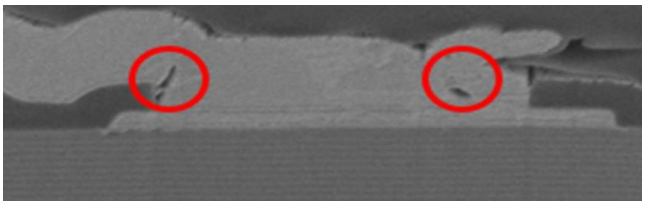

Fig. 5. SEM image of the cross-sectional view of a HTOL-failed device where circled regions denote bubbles in the metal plating.

The beam profile of the HTOL-failed chip suggests that some issues may have caused the devices' early failure and resulted in partial damage of the VCSEL emitting active regions. FIB was applied for cross-sectional sample preparation on some of the failed and degraded chips. And the prepared sample was studied using a scanning electron microscope (SEM) to study their possible roots of failure. On one of the failed VCSEL chips, we discovered bubbles between the plating layers and the p-type metal contact metallization layers.

DISCUSSION

The material analysis along with the beam profiling results suggest that process imperfections may cause the "infant" device failures. As shown in Fig. 5, bubbles in the edges of metal plating can be identified. The metal layer has several air bubbles. Due to the possibility of charge buildup brought on by the presence of air in these spaces, component failure and ESD are both probable to occur. Therefore, in addition to process uniformity, it is best to avoid the metal deposition phase of the production process as much as feasible. And we speculate that the bubbles could be the root cause for the formation of dark-line-defects that could result in the early failure of GaAs-based semiconductor devices such as VCSELs.

The near-field beam profiling technique could be a useful and rapid method to identify and spot damaged regions in VCSELs. And there have been prior reports that DLD-related damages could be observable using beam profiling [11]. But few have attempted to cross-reference material analysis results with the beam profiles of HTOL-stressed VCSELs.

The HTOL, beam profiling, FIB, SEM, CTEM, and PV TEM results can be studied from a broad perspective to predict the failure model and design a modified ESS plan to screen out chips with a higher probability of failing and eventually improve the probability of survival. In comparison, material analysis tools like FIB, SEM, CTEM, and PV TEM are costly and time-consuming. The beam profiling technique could be a fast and rapid alternative for quick dissection of VCSEL defects and failures, which could be employed in large-scale wafer-level testing for screening failing chips in VCSEL manufacturing.

CONCLUSION

In this paper, we performed a comprehensive analysis on HTOL-stressed VCSELs to study the device characteristics after accelerated aging. The novel beam profiling technique presented in this work could spot and identify the damaged regions in HTOL-stressed VCSELs. The beam-profiling method may be useful for identifying zones of weakness or process defects in VCSEL chips without the need for expensive and time-consuming materials analysis electron microscopy services and other material analysis services. The fast and affordable beam profiling technique allows semiconductor reliability engineers and VCSEL

manufacturers to discover and investigate VCSEL failures quickly and efficiently.

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ACRONYMS

CTEM: conventional transmission electron microscopy
DBR: distributed Bragg reflector
DLD: dark line defect
ESS: environmental stress screening
ESD: electrostatic discharge
FIB: focused ion beam
HTOL: high temperature operating life
L-I-V: light-current-voltage
MTTF: mean time to failure
PV TEM: plan-view transmission electron microscopy
SEM: scanning electron microscopy
TO-46: transistor outline packaged at case style 46
VCSEL: vertical-cavity surface-emitting laser