Scalable Selective Area Doping for Manufacturing of Planar Vertical Power GaN Devices

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Abstract

Selective area doping remains a key hurdle toward scalable manufacturing implementation of many power GaN device topologies. Effective ion implanted dopant activation has been shown at NRL using a scalable process dubbed Symmetric Multicycle Rapid Thermal Annealing allowing controlled doping of both high-quality bulk GaN and widely available, inexpensive heteroepitaxial GaN on sapphire. Here we show highly efficient (>70%) activation of ion implanted silicon with high mobility exceeding 160 cm^2/Vs and TCAD calculations predicting ion implanted JTE termination structures capable of near ideal breakdown for planar p-i-n diodes.

INTRODUCTION

Gallium nitride (GaN) is a leading material for next generation high power devices owing to its superior figures of merit over current state of the art materials as well as its increasing market share in RF applications generating economies of scale. For power devices, vertical architectures are especially advantageous[1]–[6]. In GaN, recent work has demonstrated 6kV diodes as well as large area 10A, 3.5kV diodes showcasing the capability of GaN[7], [8]. Among the challenges persisting for ease of commercialization include the efficient ion implant activation for n-type, p-type, and durable semi-insulating materials while maintaining the quality and low unintentional doping of unimplanted material. This remains difficult due to instability of GaN at ambient pressures for temperatures high enough to remove ion implant damage and activate dopants, often leading to material degradation and excess unintentional carriers[9], [10]. Here we demonstrate efficient activation of ion implanted silicon in GaN while maintaining film quality and low carrier density of unimplanted material and its potential application to termination structures of high power GaN devices.

RESULTS & DISCUSSION

Unintentionally doped (UID) Ga-polar GaN templates were grown on sapphire 2.2 microns thick by MOCVD. Ion implants were made approximating a 300nm deep, ~1e19 cm^{-3} box profile, with a localized surface concentration of

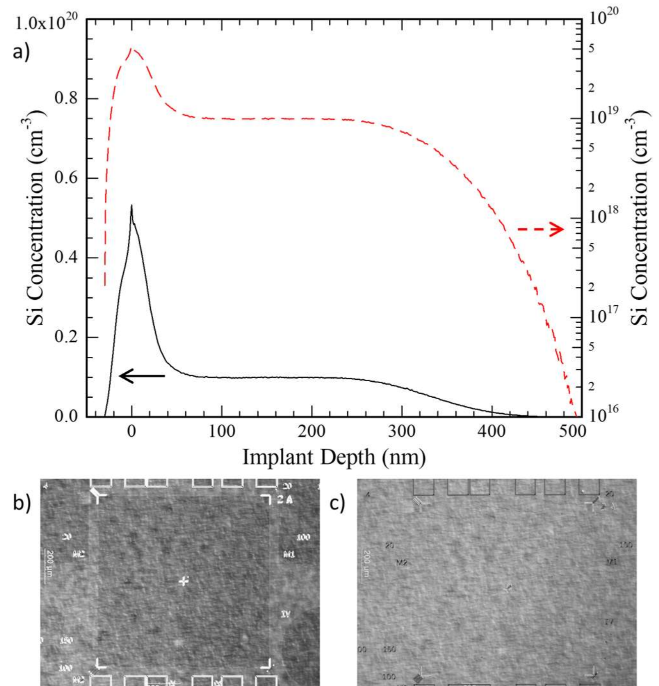

Fig. 1. a) Silicon implant concentration profile SRIM calculation in linear scale (solid) and log scale (dashed), b) As-implanted Nomarski image exhibiting implant contrast, c) As-annealed Nomarski image showing damage removal.

5e19cm^{-3} to facilitate contacts, for a total dose of 5e14cm^{-2}, as shown in Fig. 1a. Implants were performed at ambient and high temperature (500°C) as well as with an additional matching nitrogen implant to maintain stoichiometry and reduce vacancy formation. Annealing was conducted via Symmetrical Multicycle Rapid Thermal Annealing (SMRTA) at temperatures up to 1530°C, as shown in Fig. 2, at moderate pressures (~30 bar) where GaN is thermodynamically stabilized to ~1000°C. Successful stabilization of the metastable GaN material up to 1530°C was achieved with a combination of the moderate pressure, a protective PECVD SiNx cap, and rapid heating and cooling at rates up to 300 K/s during SMRTA. Contacts were made using typical Ti/Al/Ni/Au and measured as deposited with a typical

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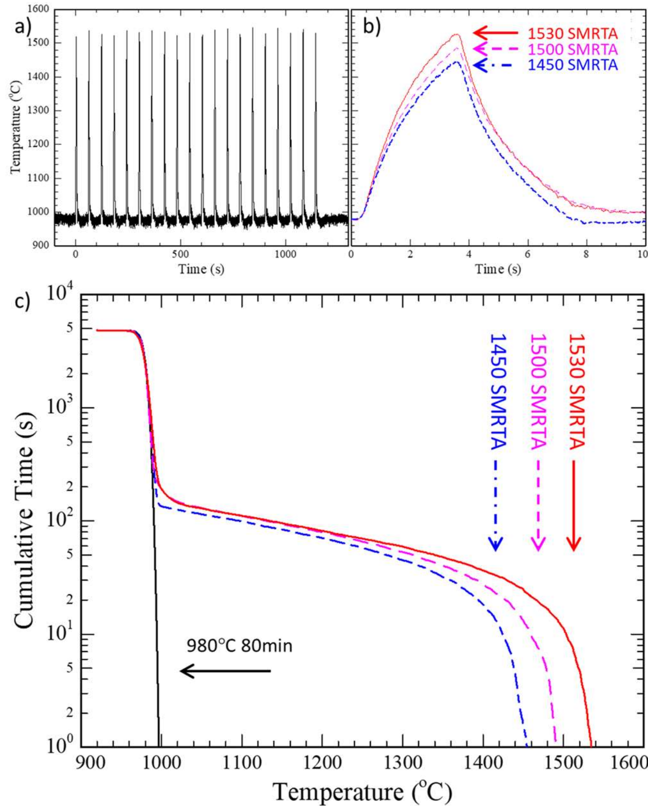

Fig. 2. Example SMRTA temperature profile. (a) 1530°C peak temperature SMRTA with 20 pulses separated by 60 seconds, (b) average pulse plotted for increasing peak temperature SMRTA from 1450°C to 1530°C, and (c) and integrated duration at or above temperature vs temperature plot for an 80 minute 980°C anneal and SMRTA anneals at 1450°C, 1500°C, and 1530°C target peak temperatures.

measured specific contact resistance of order 10^{-5} ohm-cm^2 by TLM as shown in Fig. 3.

Contrary to initial expectations, high temperature silicon implants did not prove advantageous and produced poor mobility with a greater sheet carrier concentration than the implanted dose indicating significant damage generation and retention after annealing. Compensation with room temperature co-implanted nitrogen after the high temperature silicon proved beneficial but still inferior to the ambient temperature silicon implant alone. Implantation of silicon at room temperature yielded a maximum mobility of 160 cm^2/Vs, beyond 70% activation efficiency, as shown in Fig. 4, while maintaining the unimplanted UID material quality after a 1500°C SMRTA with consistent mobility to the as-grown material and electron concentrations from 10^{16} to 10^{17} cm^{-3}, as shown in Fig. 5. Sequential co-implantation with both silicon and nitrogen at room temperature exhibited slightly reduced mobility compared to silicon alone while the activation efficiency was comparable indicating that the additional defects generated from the nitrogen implant proved equally or more deleterious in this case than any benefit from maintaining material stoichiometry.

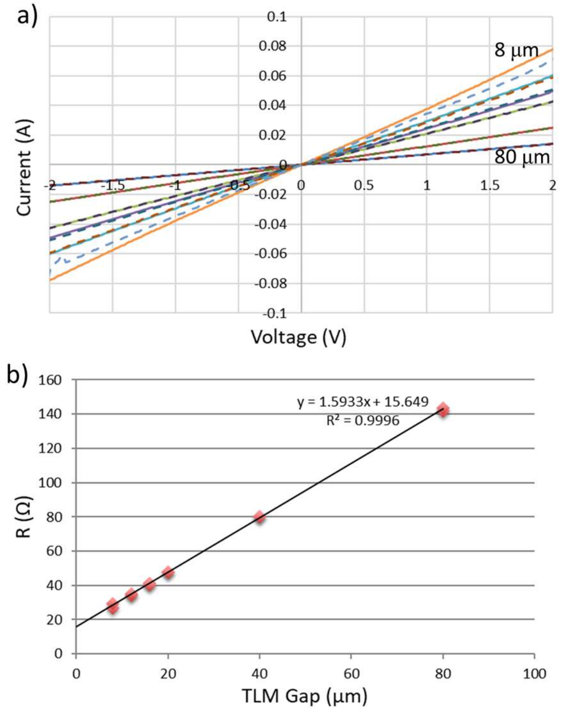

Fig. 3. Linear transmission line measurements of implanted and annealed films showing (a) good ohmic contact from 8 to 80μm distances and (b) good linear extrapolation to low contact resistance after a 1500°C SMRTA.

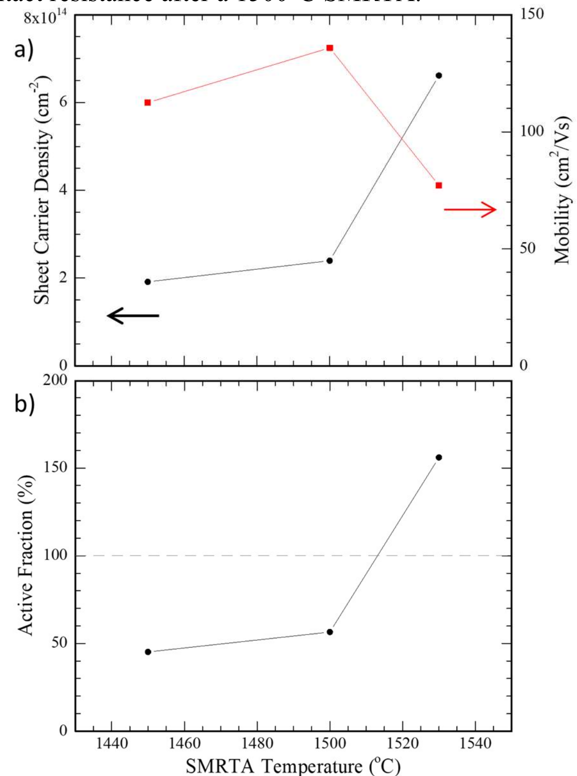

Fig. 4. Sheet carrier concentration, mobility, and activation efficiency for standard SMRTA anneals with peak temperatures from 1450°C to 1530°C.

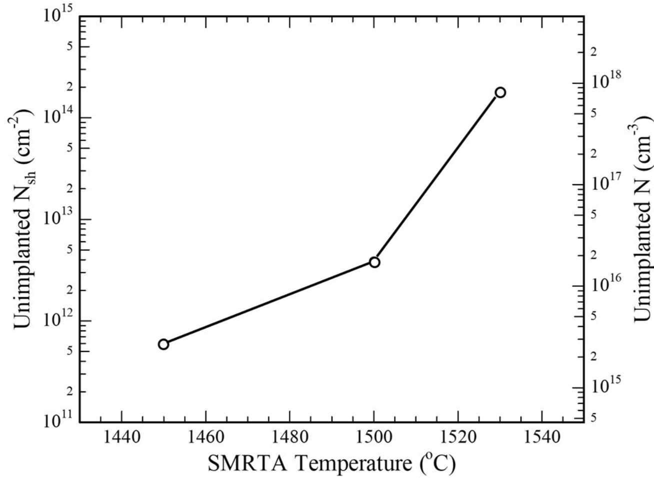

Fig. 5. Unimplanted sheet and volumetric carrier density after annealing as a function of nominal peak SMRTA temperature.

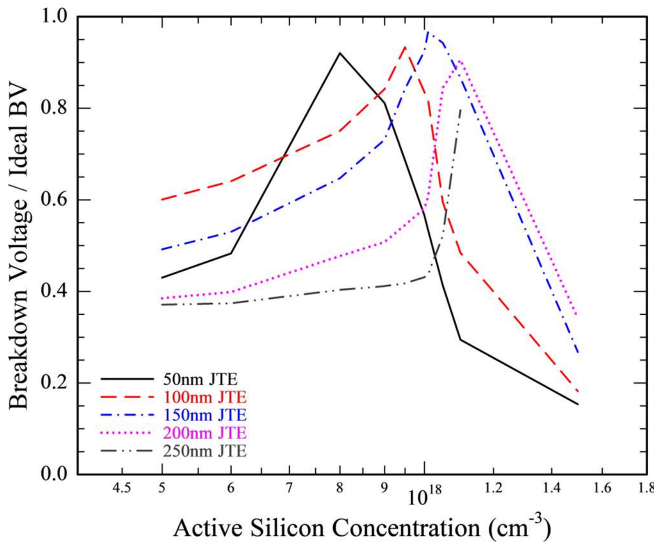

Fig. 6. Calculated breakdown voltage for ion-implanted JTE compensating as-grown p-i-n diode stack as a function of counter-doping concentration for various JTE thicknesses achieving near parallel plane breakdown voltage.

Additionally, TCAD calculations indicate that silicon ion implanted terminations into as-grown p-i-n diodes can yield high voltage devices with breakdown nearing ideal parallel plane values, as shown in Fig. 6 for a simulated 4.5kV structure. As inherent to any JTE based termination, the active charge density is critical, producing a relatively sensitive process window for a given JTE thickness. Due to the precision of ion implantation, such precise control of the implantation dose is accessible while guard ring or hybrid terminations provide further process latitudes[11]. For such a 4.5kV diode, the drift layer must maintain doping below 10^{16} cm^{-3}. Such capabilities have proven readily accessible within the SMRTA process with the demonstrated capability to maintain low unintentional doping of the drift layer while simultaneously activating the implanted dopants efficiently.

Conclusions

The demonstration of highly efficient and effective implanted n-type dopant activation simultaneously coupled with maintaining low UID film carrier density show ion implantation is ripe to be applied to device topologies in GaN. Furthermore, simulations show effective termination methods can be achieved with such implanted and annealed material at the 5kV device node and beyond. The demonstration using low cost and high dislocation density heteroepitaxial GaN further suggest significant potential for low cost or application to higher performance substrate technologies for widespread device applications. This simultaneous capability enables new high power device topologies and freeing device designers from the difficulties and drawbacks of regrowth.

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Acronyms

GaN: Gallium Nitride
UID: Unintentionally Doped
MOCVD: Metalorganic Chemical Vapor Deposition
SRIM: Stopping Range of Ions in Matter
SMRTA: Symmetric Multicycle Rapid Thermal Annealing
PECVD: Plasma Enhanced Chemical Vapor Deposition
TLM: Transmission Line Measurement