Large Diameter Epi-Ready InP on Si (InPOSi) Substrates

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INTRODUCTION

For RF as well as for optoelectronic applications, InP has been clearly proven to be a material of choice as far as technical performance is considered. But this material has also been very often quickly discarded from the industrial roadmaps, for several key reasons: 1) too expensive; 2) too fragile, 3) limited to low volume and 4) limited to small diameter substrates. We consider in this paper a substrate approach based on wafer bonding to address these limitations. These engineered substrates have been designed to be epitaxy compatible. In this paper, we report on the InPOSi substrates development as well as on the growth by Metal Organic Vapor Phase Epitaxy (MOVPE) of test structures on 100 mm InPOSi substrates.

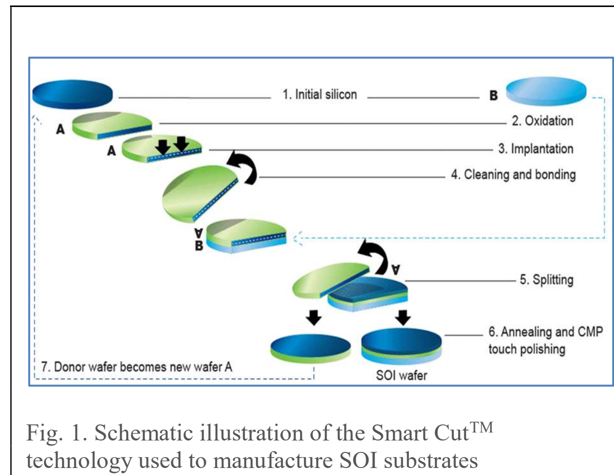

Fig. 1. Schematic illustration of the Smart Cut^{TM} technology used to manufacture SOI substrates

LARGE DIAMETER INPOSI SUBSTRATES

Figure 1 shows the Smart Cut^{TM} technology used to produce the best-in-class SOI substrates. In this process, a thin layer is transferred from a silicon substrate (donor) to another silicon substrate (receiver). A SiO_2 layer, which becomes a buried SiO_2 layer at the end of the process, isolates the SOI layer from the substrate and is formed on at least one of the two wafers. Afterwards, these substrates are attached via wafer bonding. The thin layer is, thereafter, detached from the donor substrate owing to the full wafer-scale in-depth splitting provoked by a preliminary hydrogen ion implantation.

Figure 2 illustrates schematically how the Smart Cut process, a wafer bonding and layer transfer process, can be used to transfer a thin monocrystalline InP film on a Si substrate [1, 2, 3].

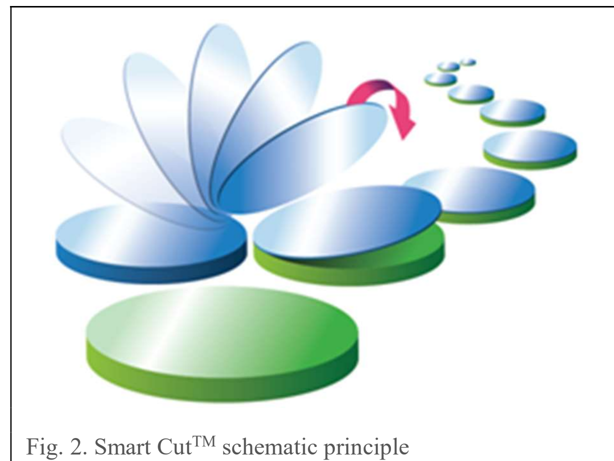

Fig. 2. Smart Cut^{TM} schematic principle

As a result, substrate cost and quantities can be optimized thanks to the capability of the Smart Cut process to re-use many times the same buk InP donor substrate to generate many InPOSi substrates. Substrate robustness is greatly enhanced thanks to the mechanical properties of the handle Si substrate.

Figure 3 shows a picture of a 100mm InPOSi wafer.

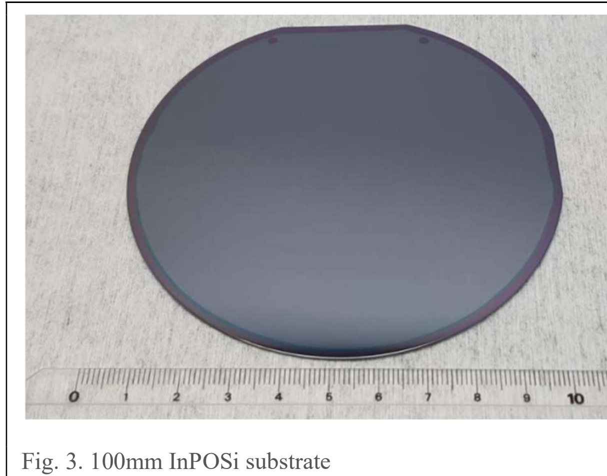
Fig. 3. 100mm InPOSi substrate

Depending on the applications, some of the final properties of the InPOSi substrates can be adjusted, such as the doping (Fe, S, and Zn), the crystalline orientation ((100) on-axis or a few degrees off), and the crystalline quality (threading dislocations densities level, for instance) of the incoming bulk InP. The same Smart Cut InP process can also be applied to other receiver substrates. Other material combinations have already been demonstrated with this process, such as ”InP on GaAs”, ”InP on sapphire”, but also ”InP on Ge” or ”InP on InP”.

The typical thickness of InP films range from 0.2 to 0.7 µm. Regarding the SiO_2 thickness, it is defined before wafer bonding and can be adjusted with a large flexibility by adjusting well known oxide formation parameters. In this work, SiO_2 film thicknesses from 0.2 to 1.5 µm have been fabricated. Further work is presently underway to decrease even further the thickness of the SiO_2 buried layer.

Surface roughness is one of the parameters that affect the quality of the epitaxy. After the layer transfer, the surface roughness equivalent to epi-ready bulk InP substrates was ensured through chemical mechanical polishing (CMP). Figure 4 shows two AFM scans (1×1 µm ² and 30×30 µm ²) obtained after this step in the case of an InPOSi substrate. The Rq values of the obtained surfaces on the 1×1 µm ² and 30×30 µm ² AFM scans were 0.176 nm and 0.254 nm, respectively, confirming that the surface roughness was adequate for the epitaxial growth step on InPOSi substrates.

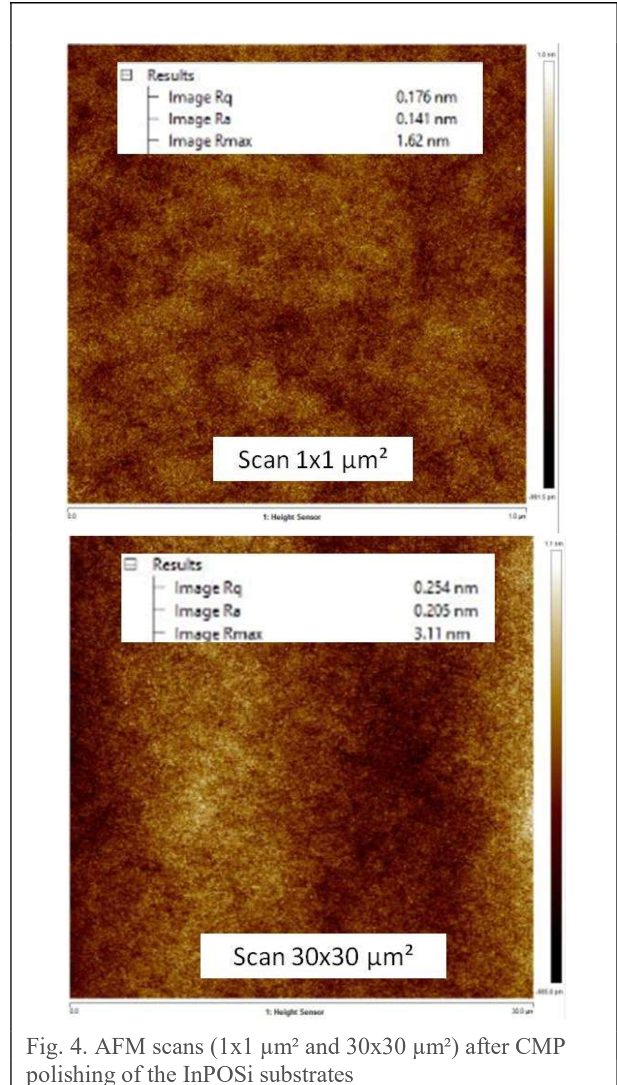

Fig. 4. AFM scans (1x1 µm² and 30x30 µm²) after CMP polishing of the InPOSi substrates

EPITAXY ON INPOSI SUBSTRATES

These InPOSi substrates have been designed to be compatible with a subsequent epitaxial growth step, in which the thin InP film acts as a seed layer for epitaxy. In this paper we focused on MOVPE, and most of the preliminary work related to epitaxy has been done on 100 mm substrates, with epitaxial runs done by two partners: III-V lab and LTM.

Figure 5 shows a Transmission Electronic Microscopy (TEM) cross-section of a Multiple Quantum Well (MQW) structure grown by MOVPE at III-V Lab (see also [2]) on a Smart Cut InPOSi substrate. One can see from bottom to top: the handle Si substrate, a SiO_2 intermediate layer, the Smart Cut InP layer (seed layer for the epi) and the MQW epi stack. No crystalline defect such as threading

dislocations or stacking faults can be detected, reflecting a good quality of the epi stack.

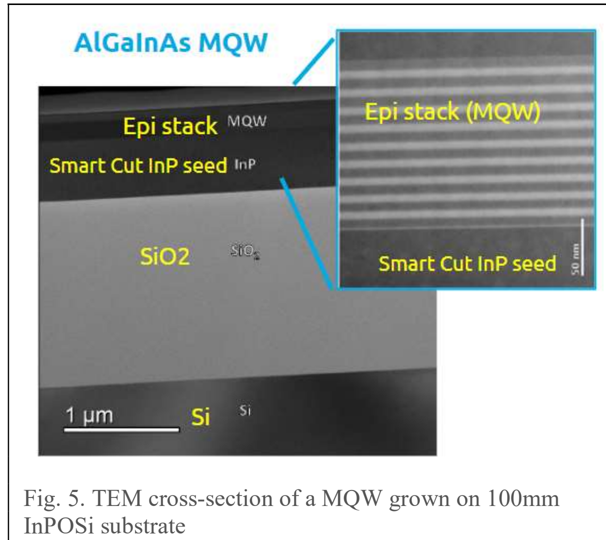

Fig. 5. TEM cross-section of a MQW grown on 100mm InPOSi substrate

Figure 6 shows a AFM view of the same MQW epitaxial stack grown on InPOSi substrates. As opposed to surface roughness before epitaxy (see figure 4), the surface after epitaxy exhibits well developed atomic terraces.

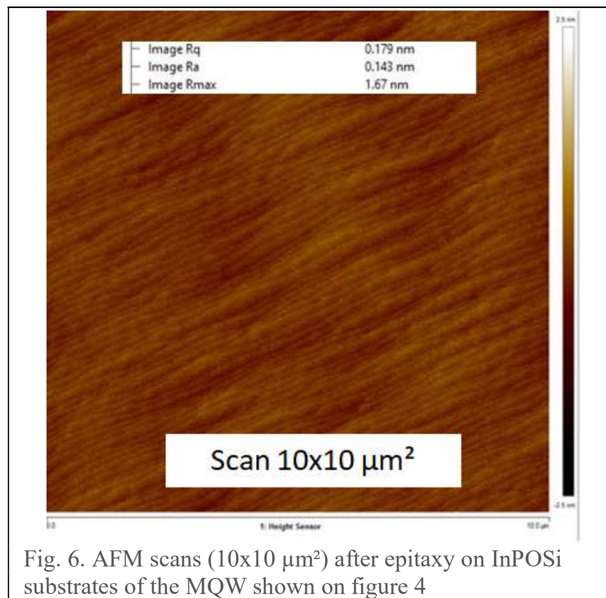

Fig. 6. AFM scans (10x10 µm²) after epitaxy on InPOSi substrates of the MQW shown on figure 4

Figure 7 compares X-ray diffraction (XRD) profiles obtained during the same growth run from two samples: one MQW grown on the 100 mm Smart Cut InPOSi and the same MQW grown on a reference buk InP. As seen in Figure 7, the XRD profiles indicate similar quality of the MQW epi stack for the two wafer substrates.

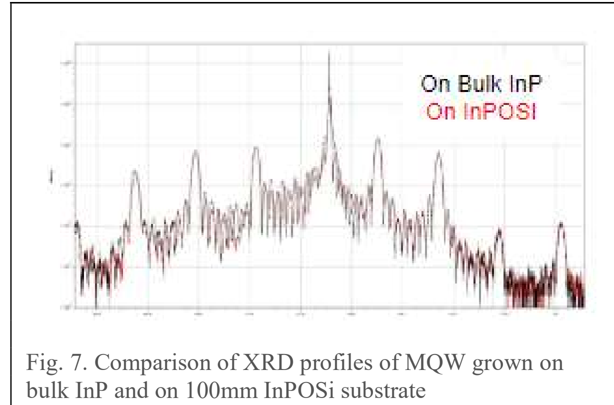

Fig. 7. Comparison of XRD profiles of MQW grown on bulk InP and on 100mm InPOSi substrate

On those Smart Cut InPOSi substrates, similar MQW structures have also been grown by MOVPE at LTM. The µPL spectra at room temperature show a peak around 1.5 µm corresponding to the targeted 9 nm QWs. 150 measurements points have been taken along the 5 cm radius. The variation of the peak position is below 10 nm and the full width at half maximum lies between 39 and 42 meV, showing the good uniformity of the material quality on the whole 100 mm wafer.

CONCLUSIONS

InPOSi substrates based on the Smart Cut process have been proposed to address historical limitations of bulk InP: high cost, high fragility, low volumes and very small diameter limitation. Beyond developments on InPOSi substrates, MOVPE on these substrates are presented for vehicle test structures such as MQWs, showing very encouraging results. Among the perspectives, on-going developments aim to evaluate more complex epitaxial stack structures and to scale InPOSi technology to larger wafer diameters.

ACRONYMS

InPOSi: InP On Si substrate
SOI : Silicon On Insulator
MQW: Multiple Quantum Well.

REFERENCES

[1] B. Ghyselen, C. Navone, M. Martinez, L. Sanchez, C. Lecouvey, B. Montmayeul, F. Servant, S. Maitrejean, I. Radu; "*Large-Diameter III–V on Si Substrates by the Smart Cut Process: The 200 mm InP Film on Si Substrate Example*", physica status solidi (a) Volume 219, Issue 4.

[2] C. Besançon, G. Cerulo, D. Néel, N. Vaissiere, D. Make, F. Fournel, C. Dupré, C. Jany, F. Bassani, S. David, T. Baron, J. Decobert *; "Comparison of AlGaInAs-Based Laser Behavior Grown on Hybrid InP-SiO2/Si and InP Substrates*", *IEEE Photonics Technology Letters,* vol. 32, no. 8, April 15, 2020.

[3] L. Sanchez, F. Fournel, B. Montmayeul, L. Bally, B. Szelag, L. Adelmini. *"Collective Die Direct Bonding for Photonic on Silicon"*. ECS Transactions 86, n° 5 (20 july 2018): 223. https://doi.org/10.1149/08605.0223ecst.