Morphology Control of Growth by Hydride Vapor Phase Epitaxy on Faceted GaAs Substrates Produced by Controlled Spalling for Low Cost III-V devices

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Keywords: HVPE, low-cost, high-throughput, epitaxy, spalling

Abstract

In this work, we apply the morphology control of hydride vapor phase epitaxial (HVPE) growth to planarize faceted, non-planar substrates. Controlled spalling is a promising high-throughput substrate reuse technology that could reduce substrate costs for III-V devices; however, the spalling fracture for (100)-oriented GaAs substrates produces a regularly corrugated surface of facets that are 5 – 20 µm in height. We discuss how to planarize these surfaces using only a few minutes of HVPE growth and how to minimize the impact on throughput when integrating faceted wafers into a potential manufacturing process at scale.

Introduction

Hydride vapor phase epitaxy (HVPE) is a reemerging growth technique with potential for low-cost, high throughput epitaxial growth [1]. HVPE growth has a demonstrated ability to control growth rates on different crystallographic facets, which enables control of the growth behavior to achieve a desired morphology [2]. Growth on non-planar surfaces can enable use of low-cost substrates and advanced non-planar device architectures, advancing the economics and capabilities of many compound semiconductor technologies. Non-planar surfaces include those resultant from substrate reuse techniques, such as spalling [3]–[5], selected area growth or epitaxial lateral overgrowth [2], selectively-etched structures [6], growth on as-sawn wafers [7], etc. Additionally, non-pristine surfaces, as resulting from technologies like epitaxial liftoff [8] and Ge-on-Ge engineered substrates [9], may also be candidates for morphology controlled growth. Here, we focus on growth on faceted substrates produced by controlled spalling because spalling is a promising high-throughput substrate reuse technology for III-V photovoltaic applications [10], [11]. Substrate reuse stands to reduce overall costs of III-V PV production by 50% [10], [11], which could enable the use of III-V PV in applications outside of high-value space markets that can benefit from their superior efficiency, high specific power, and mechanical flexibility, while still reducing costs in these existing markets.

A major limitation to application of controlled spalling in industrial process flows is the formation of a regularly corrugated surface with 5-20-µm-high facets after spalling (100)-oriented GaAs [3]. Fig. 1. provides an example of a spalled surface. Growth of flat epilayers, which enable most devices to perform at their best, requires morphology control to use spalled (100) GaAs substrates. We develop HVPE growth conditions that favor growth on the facet faces rather than the (100) surface, enabling evolution of the faceted morphology to a planar surface with minimal growth [12]. We track the morphological evolution during planarization by examining cross-sections of GaAs buffers with marker layers to extract growth rates on faceted {n11} and planar (100) surfaces. We discuss the impact of facet size and growth rate anisotropy on production throughput and cost.

Planarizing Spalled Wafers

In this work, we consider faceted substrates that were produced by controlled spalling of n-type, (100)-oriented GaAs wafers with a 6˚ offcut toward (111)A using an electroplated nickel stressor layer. The nickel stressor layer was deposited on full 2” wafers using galvanostatic electroplating following procedures described in [13], [14]. Wafers were then spalled in the [0 -1 1] direction (orthogonal to the 6°A offcut) to yield a faceted surface consisting of nominally {n11}B planes with roughly 6 µm peak-to-trough height [15].

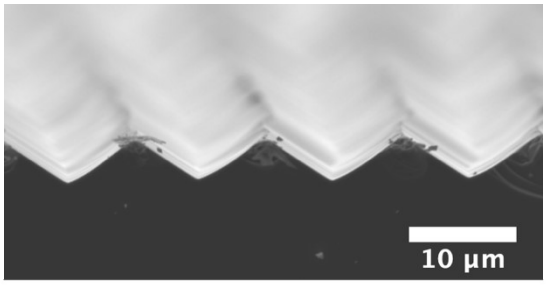

Fig. 1. Scanning electron micrograph of a cross-sectioned spalled (100)-GaAs wafer.

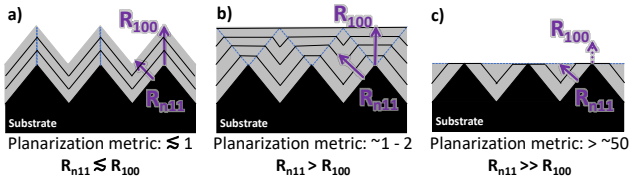

Fig. 2. Schematic depiction of planarization growth on faceted substrates the cases of a) equal facet and planar growth rates, b) greater facet growth rate, and c) much greater facet growth rate.

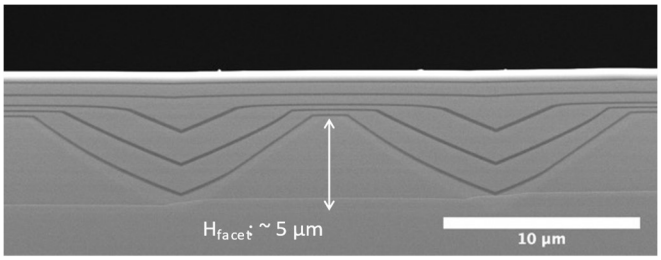

Fig. 3. SEM micrograph of a cross-sectioned planarization sample. Five GaAs layers are separated by thin AlGaAs marker layers, which give contrast due to doping. Each GaAs layer consists of 100 s of growth.

We developed planarizing GaAs buffer growth using a custom built, two-growth-chamber dynamic HVPE reactor, described elsewhere [16]. Planarizing GaAs buffer layers employed growth conditions that maximize the ratio of facet to (100) growth rates. We varied GaCl and AsH_3 flow, which were previously identified to have an effect on planarization efficiency [12]. Approximately 50-nm-thick AlGaAs marker layers were grown after every 100 – 200 s of GaAs growth to track the evolution of the growth surface over a total of five GaAs layers. Samples were then cross-sectioned by cleaving and imaged in a scanning electron microscope (SEM) to observe the evolution of the growth surfaces.

Fig. 2. describes a few idealized cases of planarizing growth in terms of the ratio of the facet growth, R_{n11}, to the (100) growth rate, R_{100}. We also refer to this ratio as the planarization metric. In Fig. 2a., $R_{n11} \leq R_{100}$, the initial growth is conformal. By contrast, Fig. 2c. depicts planarization that occurs rapidly. The (100) growth is negligible, and the troughs fill in using the least amount of material possible, equivalent to a planar growth of half the facet height. Fig. 2b. describes an intermediate case, where planarization is achieved with a few microns of growth on the (100) surface. Fig. 3. shows a cross-sectional SEM micrograph of an HVPE growth with a planarization metric of ~4.5. This growth exhibits similar, although slightly stronger planarization behavior to Fig. 2b. We achieved this planarization metric by increasing GaCl and decreasing AsH_3 flow rates, as suggested by [12].

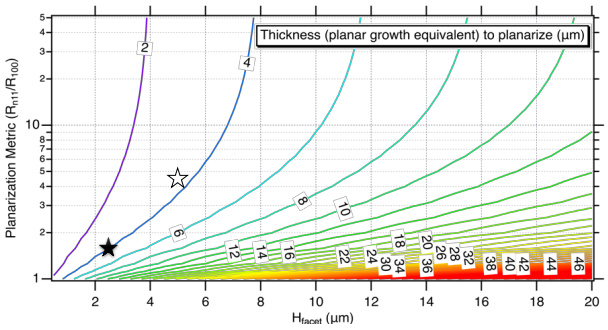

Fig. 4. Calculated thickness to planarize for given facet heights and planarization metrics. The stars denote planarization metrics achieved in [12] (black, filled) and in this work (white, unfilled).

Planarization Throughput for D-HVPE Process

We used the geometry described in Fig. 2b. to calculate the necessary thickness and growth time to planarize facets of a given height and for a range of planarization metrics. We report thicknesses as the amount of material equivalent to a planar growth. We also assume the planarization metric to be constant throughout the growth, although in reality this may vary slightly as the growth progresses due to changing facet/(100) surface area, and any potential effects of surface diffusion. First, we consider the necessary thickness to planarize. Fig. 4. summarizes this result within a realistic range of parameters: facets up to 20 µm tall and R_{n11}/R_{100} ratios up to 50. The upper left is the optimal case to minimize materials consumption – small facets and high planarization metric will require the least growth to planarize. The thickness to planarize asymptotes to half of the facet height (i.e., only filling in the facets) as the planarization metric increases, yielding the behavior shown in Fig. 2c. Our initial study of planarization yielded a planarization metric of ~1.5 on top of ~2.5-µm-highfacets, shown by the black (filled) star in Fig. 4 [12]. Recently, we made improvements to the planarization growths, resulting in a roughly 3× higher planarization metric, which is exampled in Fig. 3. This improved planarization case, denoted by the white (unfilled) star in Fig. 4, was demonstrated on ~5 µm tall facets. This case required roughly the same amount of material to planarize because the facets were larger in this case. These larger facets are associated with spall depths required for PV device lift-off, thus 5 µm tall facets are more typical for a process that reuses wafers for PV device growth. The excess material to planarize, subtracting the amount needed to fill in the facets, decreased from ~2.5 µm to ~1.5 µm for the improved planarization case.

Next, we calculated the time to planarize, given the actual R_{n11} of ~0.9 µm/min associated with the observed planarization metric of 4.5. Fig. 5a. plots these results with the time to planarize in minutes. Note that an increasing planarization metric decreases R_{100} with a fixed R_{n11} in this calculation. The model agrees well with our observation of

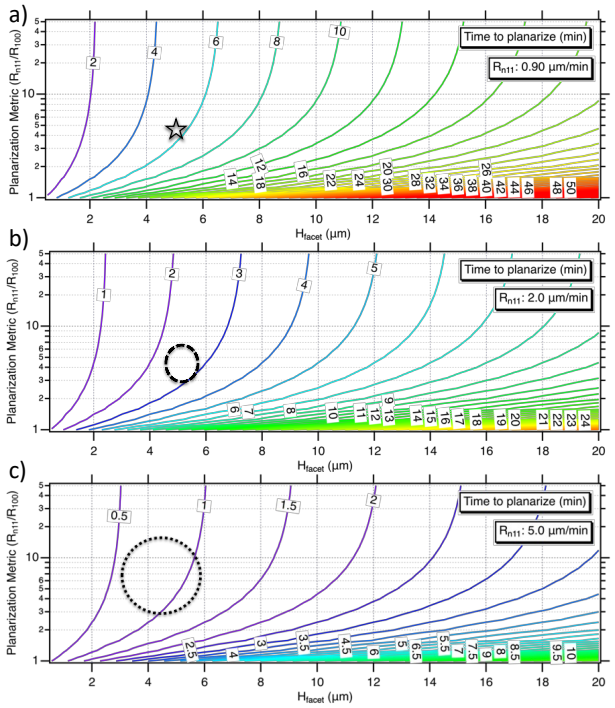

Fig. 5. Time to planarize for given facet height and planarization metrics, assuming R values of a) 0.9 μm/min (already achieved in Fig. 3.), b) 2.0 μm/min (possible in near term), c) 5.0 μm/min (highest HVPE growth rate yet demonstrated).

planarization in roughly three 100s-long layers of growth shown in Fig. 3., which is marked by the star. Slight differences between this model and reality stem from a non-constant planarization metric during growth. Fig. 5a. also indicates that increasing the planarization metric further will not reduce the time to planarize significantly, although this would reduce the required GaAs thickness by up to a few microns. If facet size remains a constraint, another reduction in growth time may be obtained by increasing the overall growth rate at a given planarization metric. The observed R_{n11} of ~0.9 μm/min is not at a limit of growth rate for planarizing conditions. In these calculations, we scale the overall growth rate by increasing R_{n11} to rates that one might expect with near-term and longer-term optimization. In Fig. 5b., we demonstrate the effect of increasing R_{n11} to 2.0 μm/min given the same range of planarization metrics. This greatly expands the range of facet heights that can be planarized in 5 min or less growth time. If the same planarization metric can be achieved (denoted by the dashed circle), 5 μm facets will be planarized in under 3 min. We have demonstrated significant increases in planar growth rates, achieving greater than 5

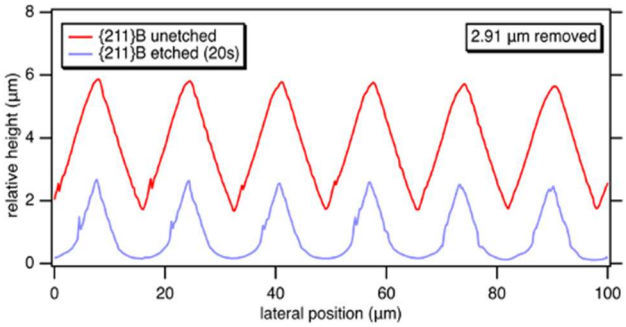

Fig. 6. Surface profiles from optical profilometry over unetched and etched regions of a spalled GaAs surface.

μm/min by varying the input flow rates in other studies [17]. Fig. 5c. plots the time to planarize, assuming that we can achieve a 5 μm/min growth rate on facets while maintaining the same planarization metric. This best-case scenario (larger dashed circle) demonstrates a lower limit of planarization time on the order of 1 min for typical facet heights.

Of course, planarization time may be reduced by also reducing facet height. Improvements to the spalling process may yield such reduction in facet size, although such a discussion is outside the scope of this work. Even if improvements to spalling technology cannot reduce facet height, chemical etching provides another means at reducing facet scale. Alkaline wet etches can provide anisotropic etching, provided they are kinetically limited [18]. This anisotropy can selectively etch {n11}B facets faster than (100). Fig. 6. shows line profiles taken on an optical profilometer over areas of unetched and etched spalled surfaces. We measure these line profiles on either side of a boundary between masked and unmasked surfaces to measure the amount of material removed, given by the offset between the profiles. The etch removed ~3 μm of material (planar material equivalent) in 20s, reducing the facet height by nearly half. Etching spalled surfaces offers an additional degree of freedom to a potential industrial process flow that incorporates spalled wafers.

Our current planarization conditions could smooth typical 5 μm tall facets in ~5 min. Planarization conditions also require low V:III ratios, which help to keep epilayer growth costs down by improving group V utilization [10]. Further, this morphology control can be applied to other relevant surface morphologies, and the development of device-quality growth on non-planar substrates will expand device-design capabilities, enabling growth of devices that possess non-planar architectures (e.g., lateral photonic structures [6]) or devices that would benefit from the conformal growth mode that produces corrugated epilayers. Broadly, new directions in compound semiconductor technology can benefit from the use of morphological control via HVPE growth.

CONCLUSIONS

Here, we demonstrate morphology control leading to planarization of spalled GaAs surfaces. We also discuss the practical considerations necessary for planarizing faceted GaAs surfaces using HVPE growth. Overall, current planarization conditions already enable growth times on the order of 5 min, and these times stand to be reduced by increasing growth rate and reducing facet size via optimization of the spalling fracture or by wet chemical etching. Thus, we envision a pathway to integrate spalled (100) GaAs substrates with HVPE growth, enabling low-cost III-V materials and devices.

ACKNOWLEDGEMENTS

The authors would like to acknowledge David Guiling for materials growth. This work was authored by Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes. This work was supported by the Operational Energy Capability Improvement Fund from the Office of Operational Energy - Innovation. A.K.B. acknowledges support from the National Science Foundation Graduate Research Fellowship Program under Grant No. DGE-1646713. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the National Science Foundation.

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ACRONYMS

HVPE: Hydride Vapor Phase Epitaxy
PV: Photovoltaics
SEM: Scanning Electron Microscope