The Application of High-Volume Manufacturing Heterogeneous Packaging Technology to Simplify Highly Complex Systems

D. Robertson[1], Md Hasnine[1], G. Kent[1], N. Salazar[1], B. Rosario[1], S. Morris[1]

[1]Qorvo Inc | Richardson, TX USA | Dylan.Robertson@qorvo.com | (469)316-9262

Keywords: System in Package (SiP), Heterogenous Integration (HI), GaN, GaAs, Radio Frequency (RF), Surface Mount Technology (SMT), Die Attach, Reliability

ABSTRACT

System in package (SiP) platforms have been growing rapidly because of their high degree of flexibility in packaging architecture. SiP is a powerful packaging platform that enables the integration of multiple packaging technologies such as fine-pitch flip chips, wafer-level packaging, wire bonding, and passive components in SMT assembly within a single module. In addition to the packaging technology, there are important technical requirements for a SiP solution such as substrate design, high-density SMT placement, thermal management, and thermo-mechanical reliability. SiP technology provides a path to heterogeneous integration (HI) solutions. Heterogeneous integration is fully used to provide a compact solution with a complex front-end module that combines multiple semiconductor technologies such as GaAs, GaN, Si, SAW/BAW, and switches with passives.

In this paper, we will demonstrate how high-volume SiP techniques were used to break down a highly complex and expensive system into integrated module packages such as front-end module, switch filter, and amplifier package in land grid array (LGA) footprint. These modules leveraged the air cavity package format as opposed to the overmold format to mitigate the dielectric loading effect. We will also discuss how the material used for die attach is crucial for the reliability and performance of power devices in the SiP RF module. Silver (Ag) sintering has become a popular solution for power devices because of its high thermal conductivity and ability to function at extremely high temperatures. We aim to offer insight into the limitations, processing difficulties, and optimization of Ag sintering die attach assembly for RF SiP over-molded modules in high-volume production.

INTRODUCTION

Future communication systems demand quicker reception, transmission, and processing of massive amounts of data. Data volumes are expanding rapidly, but power availability is not keeping pace. Hence, the next-generation modules must process more data while also becoming increasingly power-efficient per bit. This will necessitate a scalable technology with a smaller form factor [1-2]. The drive towards heterogeneous integration (HI) is necessary to sustain the progress achieved over the years as per Moore's Law. HI involves constructing large systems from smaller components - System in Package (SiP) - that are independently designed, packaged, connected, tested, produced, marketed, and integrated [3]. System in Package (SiP) technology has experienced rapid growth in radio frequency (RF) applications due to its highly flexible packaging architecture. RF SiP is a potent packaging platform for 5G base stations and allows for the integration of various packaging technologies like fine pitch flip chip, wafer level packaging, wire bonding, and SMT assembly of passive components within a single module [3-6]. The design of the substrate, high-density SMT placement, die-attach, thermal management, and thermo-mechanical reliability are key technical requirements for a successful SiP solution [4-9]. Historically, onshore ITAR-compliant packaging for SiP assemblies has been insufficient to create high-frequency high-performance modules. However, through SHIP-RF, Qorvo Inc has enabled many package assembly processes for the integration of RF SiP modules in high-volume production environments. This paper will discuss how Qorvo Inc broke down a complex and expensive system into five small, low-cost SiP modules.

This paper then aims to examine the challenges and optimization of these package assembly processes in both over-molded and air cavity packages. As SiP microelectronics modules continue to become more compact, the use of a mixture of technologies (GaN, GaAs, Si, SiGe, etc.) and assembly methods (flip chip, die-attach, etc.) has become crucial in ensuring adequate clearance between individual components. The paper will provide a comprehensive understanding of these complex assembly processes and their implications for heterogeneous integration.

EXPERIMENTAL PROCEDURE

Test Vehicle 1 feature five air cavity laminate-based RF surface mount SiPs with Land Grid Array (LGA) footprints. These packages were designed by BAE Systems in partnership with Qorvo Inc through the SHIP-RF program. The modules combine BAE Systems' custom GaAs MMICs with commercial ICs and components. The die dimensions range from 0.25mm^2 to 5.25mm^2. The dimensions of each module measure less than or equal to 10mm x 10mm and are assembled on a Printed Wiring Board. Together, these five modules

integrate amplifiers, filters, couplers, switches, attenuators, and capacitors. A 6-layer laminate with stacked thermal and signal vias was selected for high frequency and low loss performance.

The Test Vehicle 2 features a compact over-molded System-in-Package (SiP) module. With dimensions of 60mm^2, the test vehicle comprises of seven wire-bonded dies, two flip chip dies, and an array of passive components. The dies utilized in this study are a blend of GaAs and Si die, with varying sizes ranging from 0.25mm^2 to 2.25mm^2. A four-layer laminate substrate was selected for this experiment.

ASSEMBLY MATERIALS AND PROCESS

In Test Vehicle 1, following the high thermal conductivity die attach and wire bonding process, the air cavity package underwent the lid sealing process. This process involved the application of epoxy on the wall area, placement of the lid, and subsequent curing.

For the die attachment process in Test Vehicle 2, a hybrid Ag sintering material was selected for its consistent and reliable manufacturability. The passive components were assembled using a water-soluble paste, while a flux was employed for the flip chip assembly. These choices were made to ensure a high-quality, high-reliability, and efficient assembly process. The die attach procedure was optimized with regard to aspects such as the dispensing pattern, material coverage, and fillet height. Inline processing and data collection were performed for all crucial responses of the die attach process, such as bond line thickness (BLT), resin bleed-out, and die shear strength. Furthermore, cross-sectional analysis was conducted to measure fillet height and verify BLT measurements. Before the wire bonding process, a plasma cleaning step was carried out.

RESULTS AND DISCUSSION

Test Vehicle 1 implements a portion of a system designed by BAE Systems. Initially, the design was rolled into a single large C&W system which, while a mature and reliable technology, drove up cost and module size due to manufacturing difficulty. However, by utilizing Qorvo Inc's layout design kits/environments, and advanced package assembly design rules, the sub-system was broken down into five air-cavity laminate SiP modules. Figure 1 illustrates this system breakdown, and Figure 2 illustrates a typical air cavity RF SiP module. Qorvo Inc's advanced package assembly design rules support package miniaturization and ensured a small form factor for each module in Test Vehicle 1. The small form factor of these five modules led to an overall system size reduction and added capability when compared to the original single large C&W design. Test Vehicle 1 demonstrates Qorvo Inc's path to enabling optimal SWaP-C (size, weight, power, cost reduction) tradeoffs and further developing the SiP platform for multiple markets including defense, cellular, and 5G infrastructure.

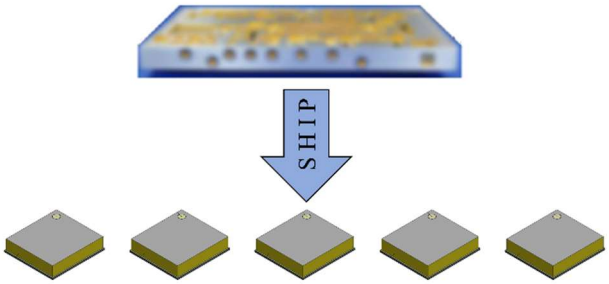

Figure 1: Test Vehicle 1 – Breakdown of C&W system into 5 SiP modules

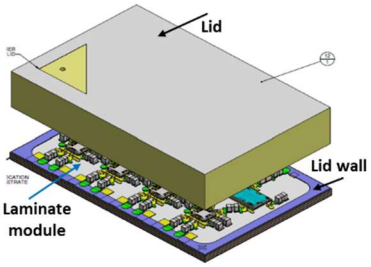

Figure 2: Typical air cavity RF-SiP module

To improve the manufacturing readiness and reliability of the SiP platform, Qorvo Inc performed extensive reliability tests on multiple parts of the assembly process. An important reliability test that Test Vehicle 1 (air-cavity package) underwent and passed was the MSL and gross leak test. This test involves placing the package in a container filled with a specific liquid at 125°C and observing it for 30 seconds to check for any bubbles emerging from the package, as shown in Figure 3.

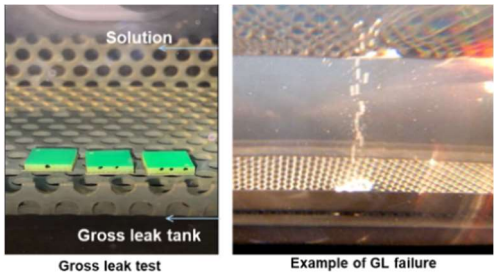

Figure 3: Gross leak test of air cavity SiP module

Packages with a size of approximately less than 8x8 mm are currently passing the gross leak test after undergoing MSL3, while packages with a size greater than 8x8 mm are passing MSL5 and the gross leak test. Efforts are being made to enhance the MSL3 and gross leak capability of larger packages. The successful passing of MSL3 and gross leak tests ensures that the module is leak-proof during board-level assembly and washing processes. This also enables us to utilize silver sintering die attach for high-power modules of

certain sizes (as proven by reduced silver migration through bHAST testing).

The coverage of die attach material is a crucial factor in determining the strength of the die after the curing process. It is imperative that there is enough material present beneath the die to ensure maximum strength. Both standard and optimized manufacturing conditions resulted in 100% material coverage for all the dies. As seen in Figure 4, the optimized die attach coverage is depicted.

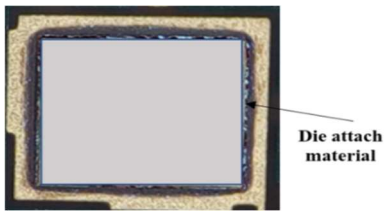

Figure 4: Die attach coverage in die

The term "fillet height" refers to the material that rises along the edges of the die, which helps to provide mechanical stability. An excessive fillet height can result in the contamination of the top surface of the die. As shown in Fig. 5, SEM cross-section and optical inspection were used to assess the fillet height on a sample of dies with optimized manufacturing conditions.

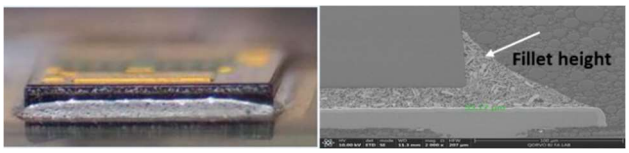

Figure 5: Die attach fillet

The thickness of the die attach bond line (BLT) plays a significant role in reducing stress and improving thermal management. By finding an optimized BLT, it is possible to achieve good results without encountering any cracks or delamination, while balancing the tradeoff between mechanical reliability and thermal management. As depicted in Figure 6, the measured BLT falls within the specifications of approximately ~ 20-40 µm.

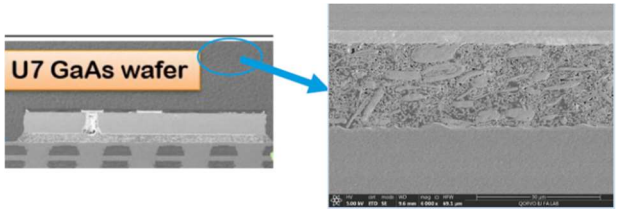

Figure 6: Die attach bond line thickness measurement

The die shear strength exceeded the specified limit for all dies, and this is not a problem given the selected sintering material. The die shear failure mode was typical, with all dies exhibiting cohesive failure. Fig. 7 illustrates this type of failure mode.

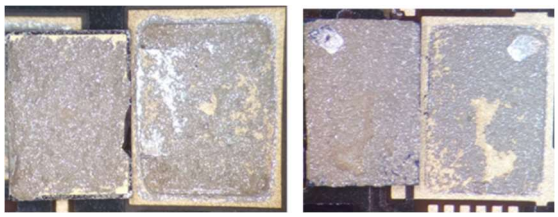
Figure 7: Die shear cohesive failure mode

The increasing component density of SiP modules, coupled with tighter tolerances and smaller solder mask webs, poses a significant challenge in terms of throughput, yield, and reliability due to the potential for resin bleed out (RBO). Resin bleeds out can result in a number of issues, such as covering the wire bonding area with bleed out from the periphery of the die, leading to non-adhesion on pads and weak wire bonds. It can also contaminate the top surface of the die, creating compatibility problems with the mold compound and causing bond degradation, delamination, and decreased thermal cycle reliability. Figure 8 illustrates a typical SiP module and the associated RBO.

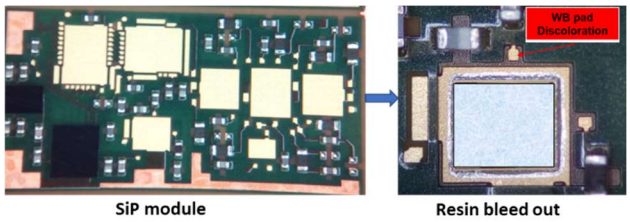

Figure 8: SiP module and resin bleed out

Through a comprehensive study using the Design of Experiments (DOE) method, it was determined that certain factors can effectively reduce the occurrence of resin bleed out (RBO). These factors include laminate design, laminate surface roughness, the implementation of an additional micro-etching process, and pretreatment of gold plating, among others. In response to this discovery, Qorvo Inc has optimized these parameters for their high-density SiP module, resulting in an increase in component density and a reduction in the solder mask web.

In conclusion, the results of the reliability evaluation indicated that the over-molded System-in-Package (SiP) module successfully passed all required qualification tests, including MSL3/3-8X reflow, uHAST (96 & 192 hours), thermal cycle (700 & 1400 cycles), and did not show any signs of delamination. Given its proven success, this tried-and-true SiP and heterogeneous integration module design and manufacturing process have now been implemented into large-scale production.

CONCLUSIONS

In this study, we examined the process of assembling and producing heterogeneous RF SiP modules in high-volume production settings. The mixed assembly process poses challenges due to resin bleed-out during die-attach, particularly with increased component density and stricter tolerances. We found that optimizing certain parameters such as laminate design, laminate surface roughness, micro-etching, and pretreatment gold plating can decrease resin bleed-out. Qorvo Inc utilized these optimizations, resulting in a 5-10% increase in component density and a reduction of 30-50 µm in the solder mask web. The reliability evaluation showed that both over-molded and air cavity RF SiP modules passed all necessary qualification tests, including MSL3 preconditioning and gross leak tests. This demonstrates that heterogeneous integration in RF SiP technology is poised for growth and innovation, enabling the production of next-generation RF modules domestically.

ACKNOWLEDGMENTS

The authors would like to thank the Qorvo Inc and BAE Systems staff for their support during this work.

REFERENCES

[1] Anderson, K., "Advances in Heterogeneous Integration for RF SiP Packaging", Microwave Product Digest (https://www.mpdigest.com/2020/07/23/advances-in-heterogeneous-integration-for-rf-sip-packaging/).

[2] Lau, J., Li, M., Xu, I., Chen, T., Tan, K. H., Li, Z., ... & Lee, R. (2019, May). Feasibility Study of Fan-Out Wafer-Level Packaging for Heterogeneous Integrations. *In 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)* (pp. 903-909). IEEE.

[3] Heterogeneous integration roadmap, 2019, "Single-chip and Multichip Integration" (Heterogeneous Integration Roadmap, Version 1.0 (ieee.org)).

[4] Garnier, A., Castagné, L., Gréco, F., Guillemet, T., Maréchal, L., Neffati, M., & Simon, G. (2021, June). System in package embedding III-V chips by fan-out wafer-level packaging for RF applications. In *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)* (pp. 2016-2023). IEEE.

[5] Wu, J., Anderson, M. J., Coller, D., & Guth, G. (2003, October). RF SiP technology innovation through integration. In *Fifth International Conference on Electronic Packaging Technology Proceedings, 2003. ICEPT2003.* (pp. 484-490). IEEE.

[6] Tai, K. L. (2000, January). System-in-package (SIP) challenges and opportunities. In *Proceedings of the 2000 Asia and South Pacific Design Automation Conference* (pp. 191-196).

[7] Hasnine, M., Rosario, B., Kent, G. and Salazar, N., "Ag Sintering Die attach Solution for System in Package RF module- Assembly, Process Challenges and Resin Bleed Out Optimization" SMTAi, 2021.

[8] Neff, B., Huneke, J., Nguyen, M., Liu, P., Herrington, T., & Gupta, S. K. (2005, March). No-Bleed die attach adhesives. In *Proceedings. International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces, 2005.* (pp. 79-81). IEEE.

[9] Jin, H., Xu, K., Naungayan, L., & Quinones, J. (2016, October). High thermal conductive die attaches paste using polymer and micron-size silver for a power semiconductor package. In *International Symposium on Microelectronics* (Vol. 2016, No. 1, pp. 000326-000331). International Microelectronics Assembly and Packaging Society.

ACRONYMS

BAW: Bulk Acoustic Wave
bHAST: Biased Highly Accelerated Stress Tests
BLT: Bond Line Thickness
C&W: Chip and Wire
DOE: Design of Experiment
LGA: Land Grid Array
GaAs: Gallium Arsenide
GaN: Gallium Nitride
HI: Heterogenous Integration
IC: Integrated Circuit
ITAR: International Traffic in Arms Regulations
LGA: Land Grid Array
MCM: Multi-Chip Module
MMIC: Monolithic Microwave Integrated Circuit
MSL: Moisture Sensitivity Level
RBO: Resin Bleed Out
RF: Radio Frequency
SAW: Surface Acoustic Wave
SEM: Scanning Electron Microscopy
SHIP-RF: State-of-the-Art Heterogeneous Integrated Packaging – Radio Frequency
SiGe: Silicon Germanium
SiP: System in Package
SMT: Surface Mount Technology
SWaP-C: Size, Weight, Power, Cost Reduction
uHAST: Unbiased Highly Accelerated Stress Test