3-D Derived Structure Electromagnetic Simulation for Enhancement Mode Low Noise pHEMT Technology.

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Abstract

For operating Radio Frequency Integrated Circuits (RFIC's) at higher frequency bands, considerations of coupling effects between nearby matching elements and metal line crossovers become an important issue due to compact chip design. An accurate electromagnetic (EM) simulation is needed for circuit implementation. In this paper, 3-D structure modeling using a derived layer technique is proposed in the Advanced Design System (ADS) Momentum structure definition for accuracy improvement. Several passive and active circuits were fabricated with the *WIN* PIH1-Y2 process for 3-D structure modeling verification. The measurement results are in good agreement with simulation.

INTRODUCTION

In the past, coupling effects of passive components were less important in front-end circuit designs due to their lower operating frequencies. Now, 5th generation communication (5G) is the most important specification for global communication circuits [1]. The main frequencies for 5G are sub-6 GHz and millimeter wave at 28 GHz. For GaAs process technology, two or three metal layers are usually provided for the designs. Metal line crossover structures are inevitable for compact layouts. In mm-wave frequency bands, coupling effects from metal line crossovers, as well as coupling effects of nearby matching elements, have to be taken into consideration as part of matching network designs to achieve predictable circuit performance [2].

Electromagnetic (EM) simulation software such as Momentum RFpro in the Advanced Design System (ADS) is a popular RF electronic design automation (EDA) tool. In traditional EM structure setup, an inductor with air-bridge structure usually exhibits inaccuracy at higher frequency bands due to the lack of dielectric layers under the air-bridge. A new 3-D structure setup using derived layer technique is proposed for accuracy improvement in this platform. The coupling effect of air-bridge structures in GaAs technologies can be precisely predicted after circuit-level verification.

In this paper, several passive and active circuits are fabricated based on the proposed EM simulation. The passive circuits, a *K*a-band band-pass filter (BPF) and a Lange coupler, are fabricated with crossover air-bridge lines in the designs. The simulated and measurement results are in good agreement. The Lange coupler is also applied in a balanced amplifier (BA) design for an improvement of input and output return losses. For active circuit verification, a low noise amplifier (LNA) and a Balanced amplifier are fabricated. The LNA exhibits a measured 3-dB bandwidth of from 10.6 to 31.8 GHz with a small-signal gain of 15.5 dB. The BA exhibits a measured 3-dB bandwidth of from 24.6 to 34.8 GHz with a small-signal gain of 13 dB and good return losses.

TABLE I
KEY PROCESS CHARACTERISTICS OF PIH1-Y2

	parameters	value
DC VD=1.5V	Gm Peak (mS/mm) Peak Transconductance	970
	Idmax (mA/mm) Maximum Drain Current	620
	IDSS (mA/mm) Drain Current at Vg=0	7E-05
	Vto (V) Threshold Voltage	0.31
	BVGD (V) G-D Breakdown Voltage	15
RF VD=1.5 V. VG@Gm Peak	f_T (GHz) Cut-off Frequency	107
	CGS (fF/mm) Gate/Source Capacitance Density	1330
	CGD (fF/mm) Gate/Drain Capacitance Density	90

EM SIMULATION SETUP AND CIRCUIT DESIGNS

PIH1-Y2 provided by *WIN* Semiconductors Corporation is an advanced GaAs technology platform which employs low-k dielectric layers for compact layouts. In this process, 0.18 µm enhancement-mode (E-mode) pHEMTs, PIN diodes, vertical Schottky barrier diodes, and 0.5 µm E-/D-mode logic pHEMTs are integrated together. The E-mode pHEMT provides excellent RF performance with a 6 V operating voltage. The key process characteristics are summarized in TABLE I.

Including the substrate layer structure is a pre-requisite for 3D viewing and EM simulations in Momentum. The substrate starts the definition of the cross-section of the product, which consists of multiple layers of metal traces, insulating material, ground planes, vias that connect traces, and the air that surrounds the board. The layer structure of the device is shown in Fig. 1. It is a stacked structure with 1st metal and 2nd metal, with air (layer name is SPAN) and SiN_x as inter-metal dielectric layers, and then connected by

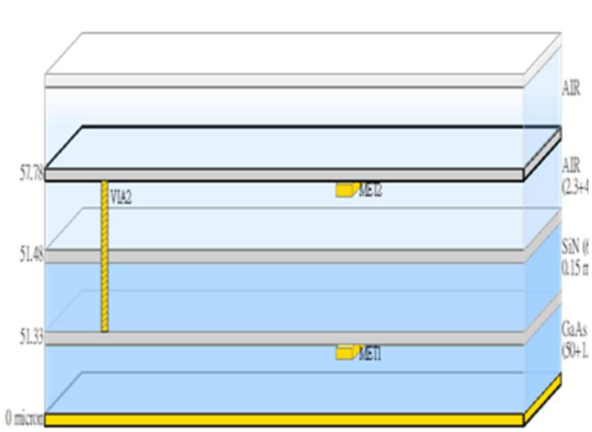

Fig. 1. Substrate definition of PIH1-Y2 technology.

"VIA2".

However, there is still a difference between the cross-section and the 3D-view for complicated structures like air-bridges. That usually leads to inaccuracy compared with measured data. The Air-bridge structure is stacked through two layers of metal and the air and insulating films, to create a cavity to prevent short circuits between the two overlapping metals, as shown in Fig. 2.

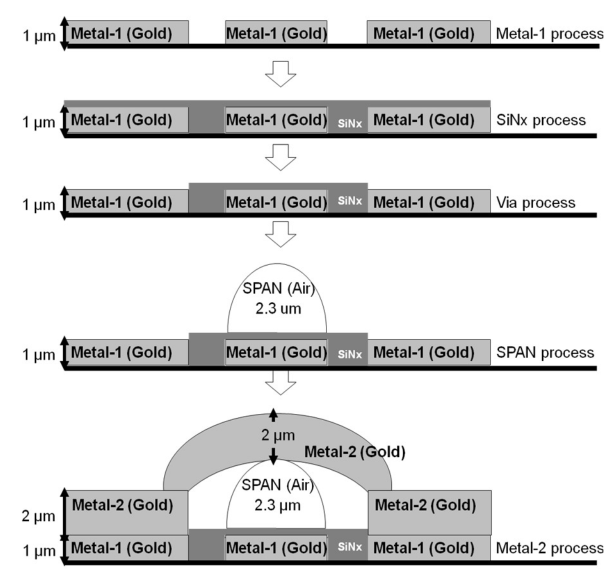

Fig. 2. Air-bridge structure and process flow. The metal thickness is 3 μm.

Fig. 3 shows a procedure to achieve a 3D-view with traditional substrates. The substrate consists of three parts - dielectrics, metal layers, and via layers. The dielectrics should be defined in the first step, then metal and via layers are imported into the substrate. Whether the "SPAN" layer is described in the layout or not, the air always exists in traditional substrates. Thus, the metal is thicker than in the actual structure that is without "SPAN" in its layout. In conclusion, the difference between cross-sections of the actual process and the 3D-view of the EM simulation is from a different establishment of the structure. Therefore, the "derived substrate" has been developed to solve this problem.

A derived layer is a technology layer where shapes are automatically derived from other technology layers. The derived layers can replace and generate shapes by specifying the type of operation, such as AND, OR, and XOR, while preprocessing the layout for physical EM simulations.

The 3D derived structure is created through the following steps. First, the difference of the metal structure position between SEM cross-section and simulation layout must be defined, as shown in Fig. 4. Second, derived layers (Air-bridge top and air bridge bottom) are inserted upon the derived structure. Then, the inserted layers are redefined by writing the operation of Boolean, in which layers are merged. The derived substrate is established by embedding these materials and newly derived layers. After the layer setup procedure, the new structure is achieved which is closer to actual structure, as shown in Fig. 5.

Several passive and active circuits have been demonstrated to verify the proposed 3-D structure modeling. A Lange coupler and a BPF are the passive circuits for *K*a-band applications. To achieve high out of band rejection in the BPF, an asymmetrical compact resonator structure is adapted to achieve two controllable transmission zeros at lower and upper stopbands, respectively. Compact chip size and low insertion loss in passband can be obtained [4]. Two

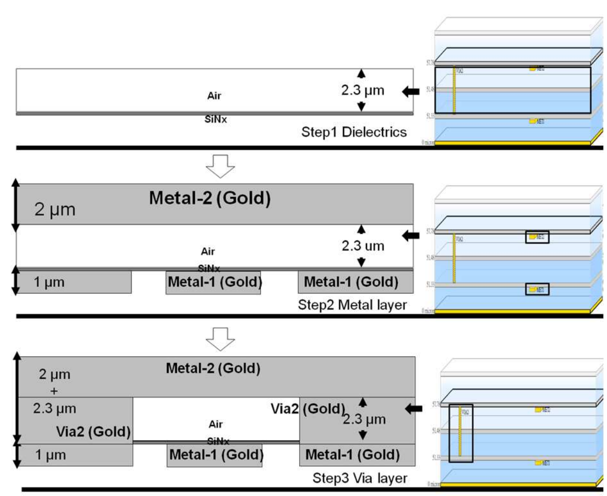

Fig. 3. 3D view of traditional substrate. The metal thickness is 5.3 μm.

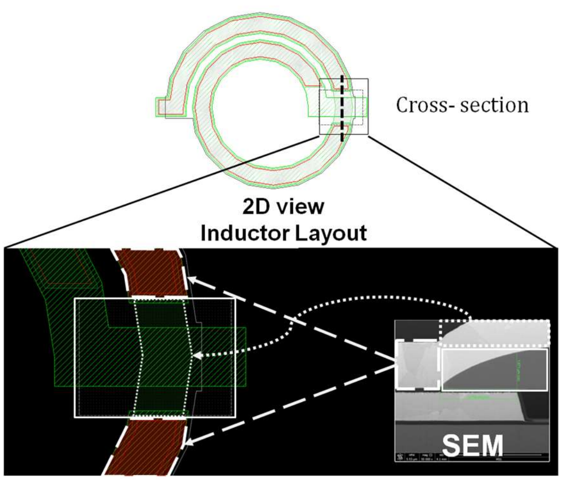

Fig. 4. Inductor layout and SEM cross-section. Observing SEM cross-section, 2nd metal is separated into "air-bridge top" (dotted line) and "air-bridge bottom" (long dotted line) layers by air cavity (solid line).

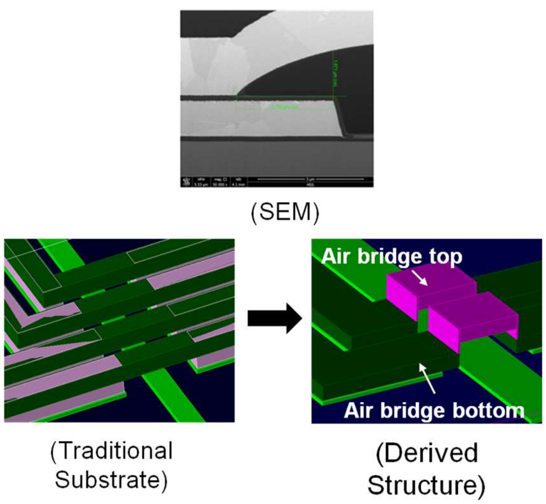

Fig. 5. Actual layer structure compared with old and new 3D image from ADS.

active circuits, an LNA and a BA with crossover air-bridge lines, are implemented as well.

The LNA is a 2-stage configuration with both-side source degeneration inductors. The first stage is designed for minimum noise figure with a 4 × 25 μm device. The second stage is with impedance matching for small-signal gain performance. The choice of the source-degeneration inductor should be a trade-off between the device maximum available gain and minimum noise figure [5]. The simulated noise figure is better than 2 dB over bandwidth of from 12.8 to 31.8 GHz.

The BA is composed of two gain amplifiers and two Lange couplers. The gain amplifier is a 2-stage configuration with R-C feedback. The R-C feedback is adopted to improve the stability and the input/output matches of the amplifier. The first and second stages are both matched for gain with the same 4 ×5 0 μm device. The simulated output 1-dB gain compression point is 10.4 dBm at frequency of 30 GHz.

EXPERIMENT AND MEASUREMENT RESULTS

The comparison of measurement and simulation for the inductor and capacitor components is shown in Fig.6. The result shows that the accuracy becomes worse at higher operating frequency based on the traditional substrate setup, as shown in Fig. 6 (b) and (d). Both of the components with the derived structure show not only a better prediction at self-resonant frequency, but an accuracy improvement of 15% at 60 GHz, as shown in Fig. 6 (a) and (c).

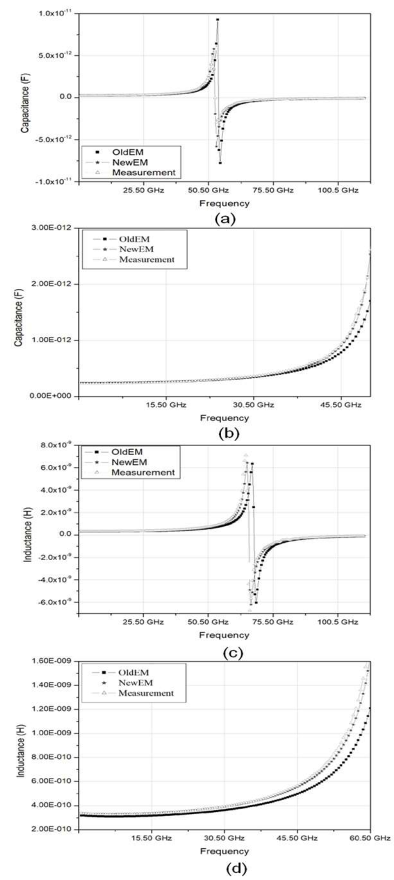

Fig. 6. Simulated and measured curves: (a)(b)capacitance, and (c)(d) inductance.

To have further circuit verification, another passive circuit, a Lange coupler, is used to verify accuracy. The EM simulation and measurement of the Lange coupler are plotted in Fig. 7. The measured results exhibit good agreement with simulations. Pass-band bandwidth is from 24 to 38 GHz, the measured amplitude and phase imbalance are better than 0.5 dB and 6 degrees, respectively. The chip photo of the BPF is shown in Fig. 8. with a chip size of 1.25

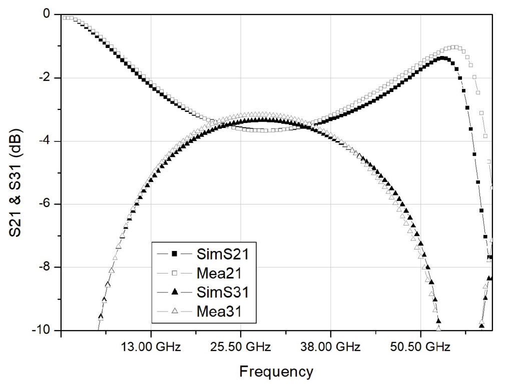

Fig. 7. Simulated and measured S-parameters of Lange coupler.

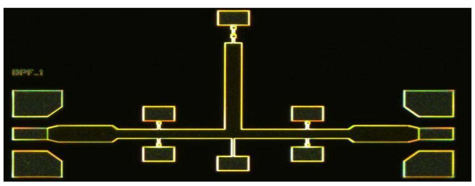

Fig. 8. Chip photo of *K*a-band BPF.

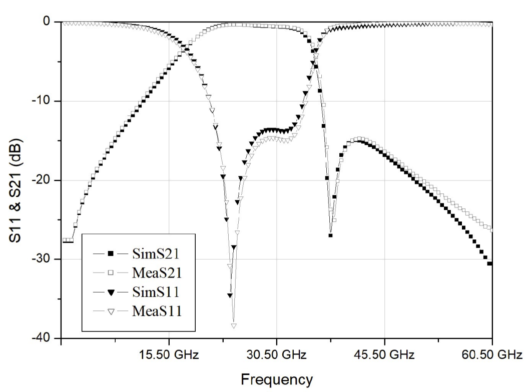

Fig. 9. Simulated and measured S-parameters of *K*a-band BPF.

$\times$ 0.7 mm^2. The EM simulation and measurement of the BPF are plotted in Fig. 9. The pass-band insertion loss is 0.4 dB with good return losses better than 15 dB. For verifying the accuracy of active circuits, a broadband LNA and a BA are fabricated. The chip photo of the LNA is shown in Fig. 10. The chip size is 2 $\times$ 1 mm^2. The dc bias is 4V with a total current consumption of 11 mA. The LNA is measured via on-wafer probing. The simulated and measured S-parameters are plotted in Fig. 11. The measured small-signal gain is 15.5 dB with a 3-dB bandwidth of from 10.6 to 31.8 GHz. The measured average input and output return losses over the 3-dB bandwidth are better than 5 and 8 dB, respectively.

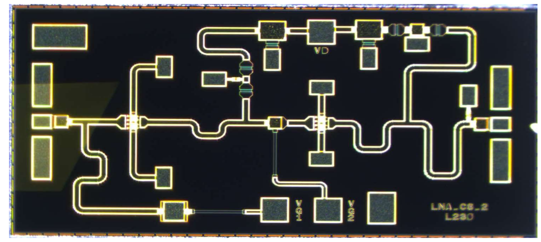

Fig. 10. Chip photo of broadband LNA.

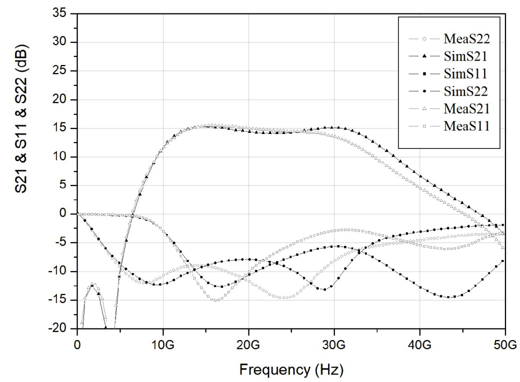

Fig. 11. Simulated and measured S-parameters of broadband LNA.

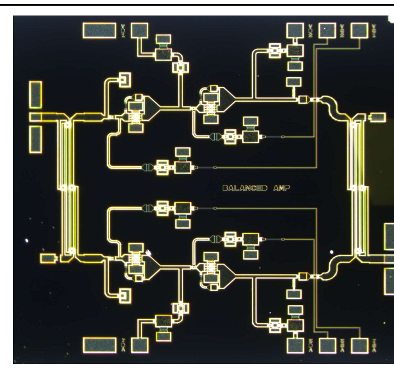

Fig. 12. Chip photo of *K*a-band BA.

The chip photo of the BA is shown in Fig. 12, with a chip size of 2.5 $\times$ 2.5 mm^2. The dc bias of the BA is 4 V with a total current consumption of 46 mA. The simulated and measured S-parameters are plotted in Fig. 13. The measured small-signal gain is 13 dB with a 3-dB bandwidth of from 24.6 to 36.8 GHz. The measured average input and output return losses over the 3-dB bandwidth are better than 12 and 15 dB, respectively.

CONCLUSIONS

3-D structure modeling using derived layer techniques is successfully demonstrated in the *WIN* PIH1-Y2 technology. The new substrate setup is functional and can achieve high accuracy in simulation up to 60 GHz based on the measurement results. The proposed method can be further applied to all GaAs technologies with air-bridge structures for high frequency RFIC design.

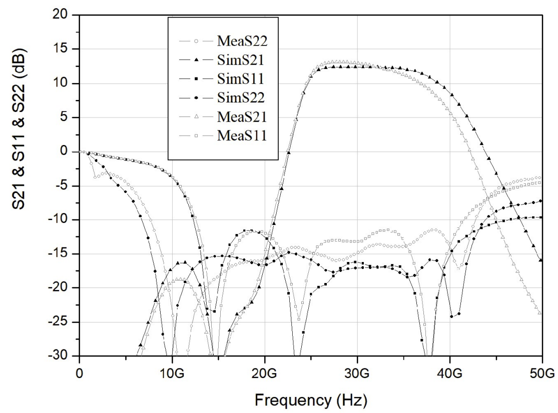

Fig. 13. Simulated and measured S-parameters of *K*a-band BA.

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ACRONYMS

RFIC: Radio Frequency Integrated Circuit
EM: Electromagnetic
mm-wave: Millimeter wave
MIM: Metal-Insulator-Metal
BPF: Band pass filters
BA: Balanced amplifier
LNA: Low noise amplifier