Design and Optimization of 1.2 kV SiC Trench MOSFETs Using a Tilted Ion Implantation Process for High Breakdown Voltage

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Abstract

This paper simulates a structure that suppresses electric field crowding on gate oxides in 1.2 kV SiC trench MOSFETs by using a tilted ion implantation process. By applying the tilted ion implantation process, both edges and bottom of the trench vulnerable to the electric field are protected. Also, it overcomes the reliability problem which is a limitation of devices with trenched gates. For comparative analysis, the tilt angle for ion implantation into the trench was modeled through TCAD simulation. A high breakdown voltage of 1577 V was achieved for an optimized tilt angle of 18.2°, but the on-resistance characteristics were degraded due to the deletion region extensions from the implanted P^+. In order to improve conduction characteristics of the proposed device, a higher doping concentration of the drift layer was also used.

INTRODUCTION

SiC trench MOSFETs have the problem of high electric field crowding on the gate oxide in blocking mode [1-5]. To solve this problem, our group studied forming p-shielding by implanting a high concentration of aluminum into the bottom of the p-base of those MOSFETs [6]. This structure is effective in suppressing the electric field crowded on the edge of the trench, but we found that when a high voltage is applied, the bottom of the trench is insufficiently protected and becomes vulnerable to the electric field.

To correct this, a structure capable of protecting the bottom of the trench using a tilted ion implantation process was designed. The tilted ion implantation process involves setting the wafer at an angle to the direction of the ion-beam during the ion implantation process [7]. The depletion layer of p-shielding formed on the sidewall and bottom of the trench by the tilted ion implantation protects the trench from the electric field [8]. This study aims to improve the electric field concentration phenomenon and the reliability of 1.2 kV SiC trench MOSFETs by applying a tilted ion implantation process. Tilted ion injection effectively protects the gate oxide from electric fields, thereby enabling stable high-voltage operation without any additional patterning to form p-shielding structures.

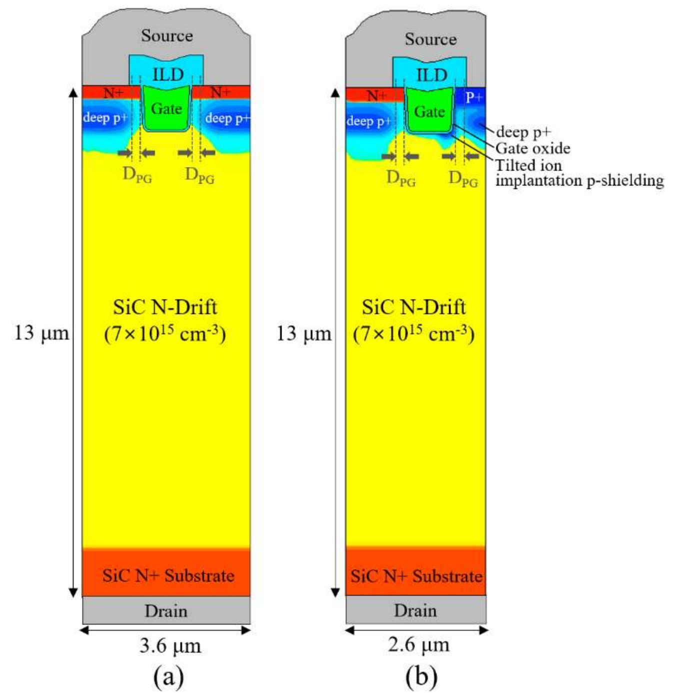

Fig. 1. Schematic device structures of 1.2 kV SiC trench MOSFETs with (a) conventional p-shielding and (b) tilted ion implantation p-shielding.

SIMULATION METHODS

The design and analysis of the tilted ion implantation p-shielding device and the conventional p-shielding device were conducted for the 1.2 kV SiC trench MOSFET using Sentaurus TCAD simulations. For all structures, an n-type 4H-SiC drift layer with a concentration of 7×10^{15} cm^{-3} and 12 μm thick was used, and the peak concentration/junction depth of the p-layer, N^+ and P^+ is 2.0×10^{17} cm^{-3}/0.79 μm, 2.7×10^{19} cm^{-3}/0.27 μm, and 1.3×10^{20} cm^{-3}/0.84 μm, respectively. The SiC trench MOSFET was simulated by process simulation, and the Okuto Avalanche model, Shockley-Read-Hall

Recombination model, and Auger Recombination model were used to analyze the blocking characteristics.

SIMULATION RESULTS

Figure 1 shows the schematic device structure of a 1.2 kV SiC trench MOSFET with (a) conventional p-shielding and (b) tilted ion implantation p-shielding. The deep p^+ of each structure was used to suppress an electric field crowded on the edges of the trench. Through previous studies, an optimized D_{PG} of 0.5 μm was applied, which is the gap between the deep p+ and the trench [6]. From analyzing the simulated electrical characteristics, the gate oxide was destroyed at 1092 V in structure (a), while the high breakdown voltage of 1577 V was predicted in structure (b) with a tilt angle of 18.2°. This is because the depletion line formed by the p-shielding with tilted ion implantation protects the trenched gate.

Figure 2 shows the electric field distribution when the same voltage of 1000 V was applied to the structures with (a) conventional p-shielding and (b) tilted ion implantation p-shielding. In structure (a), a high electric field of 4.7 MV/cm was concentrated at the bottom of the trench, whereas in structure (b), the electric field at the bottom of the trench was considerably suppressed. Accordingly, the model predicts that a device having a tilted ion implantation p-shielding structure can withstand a higher driving voltage than an existing device and consequently, the reliability of the device can be improved.

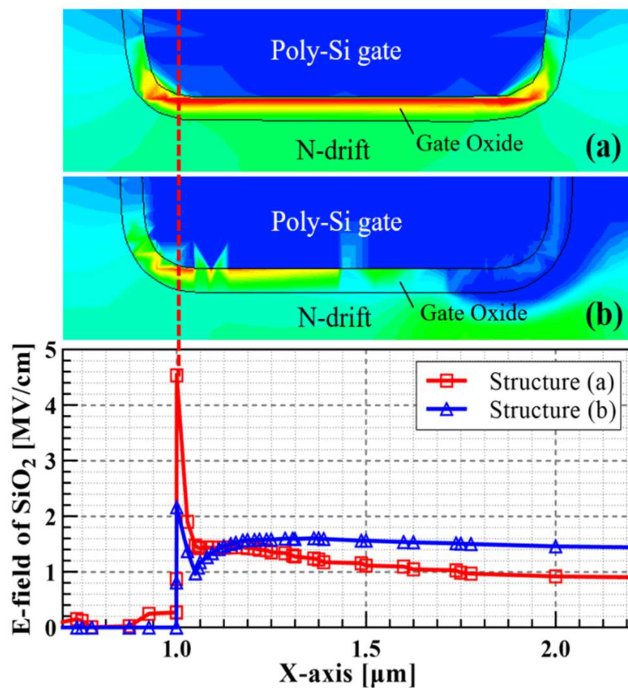

Fig. 2. Comparison of the electric field distribution at 1000 V of the (a) conventional p-shielding structure and (b) 18.2° tilted ion implantation p-shielding structure.

Figure 3 illustrates a possible process flow for a 1.2 kV SiC trench MOSFET with tilted ion implantation p-shielding. In stage (a) the trench is etched using a SiO_2 mask. A deep p^+ junction is implanted to reduce the electric field concentrated at the edge of the trench, with a single energy of 700 keV and dose of 1×10^{15} cm^{-2}. When performing tilted ion implantation, some ions are implanted into the sidewall of the trench. In order to prevent this problem, a thin oxide film is deposited in stage (b).

Subsequently, aluminum is implanted with a tilt angle in stage (c). Ion implantation is performed twice with energies of 50 keV and 70 keV, both at a dose of 5×10^{14} cm^{-2}. The area of p^+ for protecting the bottom of the trench varies according to the tilt angle. When the tilt angle is increased, the area covering the bottom of the trench is reduced, and the protective effect of the trench and the breakdown voltage is decreased. However, when the tilt angle is decreased, the area covering the bottom of the trench is increased, preventing the formation of a channel. Therefore, it is necessary to optimize the tilt angle.

Following the completion of ion implantation, all oxides are removed, and high-temperature annealing is performed at 1800°C for 30 min. Finally, a gate oxide, ILD, and passivation are formed, and source and drain electrodes are attached to analyze the electrical properties in stage (d).

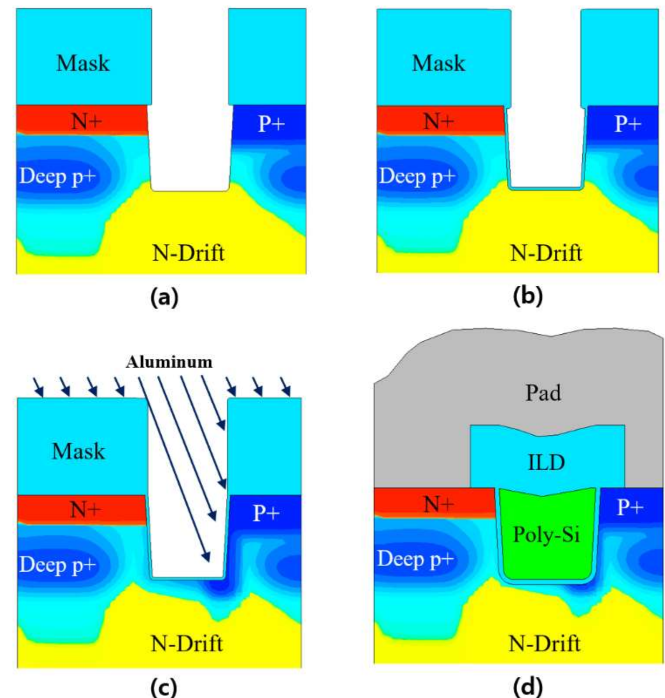

Fig. 3. Proposed process flow of a 1.2 kV SiC trench MOSFET with tilted ion implantation p-shielding.

Figure 4 and Equation (1) show calculation procedures to obtain the optimal implantation angle to effectively protect the gate oxide trenches with the tilt ion implantation process principle and angle calculation method. The tilt angle varies depending on the depth of the trench and the thickness of the

mask. In this structure, a trench depth of 1.0 μm and a mask thickness of 1.0 μm are used.

$$tilt\ angle\ \theta = tan^{-1}\left(\frac{Non-implante\ \ region\ length}{Mask\ thickness + Depth\ of\ trench}\right) \quad (1)$$

The electrical characteristics change depending on the tilt angle for ion implantation. Tilt angles of 11.3°, 18.2°, 21.8° and 26.6° are angles at which p-shielding ion-implanted from the trench sidewall covers 60, 40, 20, and 0 % of the trench bottom, respectively.

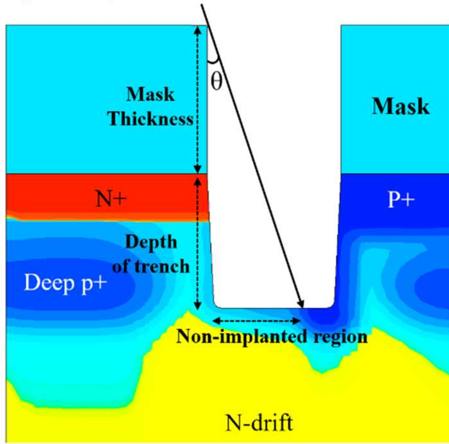

Fig. 4. Calculation of the implanted angle to form P+ shielding structures on the trenched gate.

The simulated I_D-V_{DS} curves, on-resistance, and breakdown voltage characteristics depending on the tilt angle are shown in Figure 5 and Table 1.

We see a high breakdown voltage of 1717 V when the tilt angle is 11.3°, but a considerably high on-resistance value of 12.0 mΩ-cm^2 was predicted. It can be concluded that 18.2° is the best angle tested for this structure because it has a high enough breakdown voltage for 1.2 kV devices.

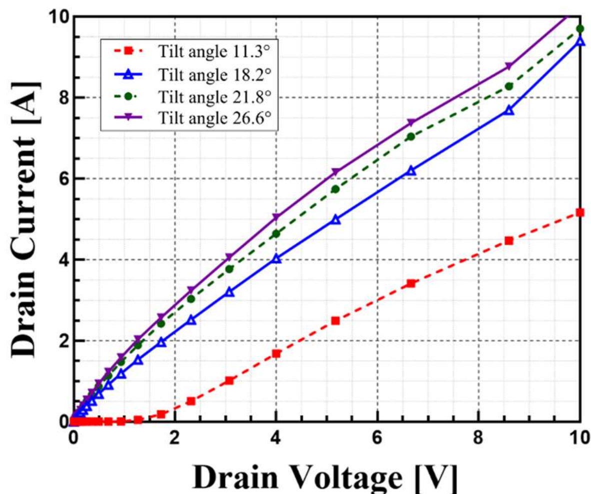

Fig. 5. Predicted I_D-V_{DS} curve for different tilt angles for an ion-implanted SiC trench MOSFET.

TABLE I

$R_{ON,SP}$ AND BV CHARACTERISTICS VERSUS TILT ANGLE FOR THE ION-IMPLANTED SIC TRENCH MOSFET.

Tilt angle [°]	$R_{on,sp}$ [mΩ-cm^2]	BV [V] and Type	
11.3	12.0	1782	Avalanche
18.2	4.7	1577	Oxide break
21.8	4.3	1470	Oxide break
26.6	3.1	1327	Oxide break

The calculated maximum electric field of SiO_2 at 1200 V for each tilt angle is shown in Fig. 6. As the tilt angle increases, the area surrounding the trench bottom of the depletion layer created by p-shielding decreases and the gate oxide is less protected from the electric field. In all cases, the highest electric field is concentrated at the lower left of the trench. Hence, considering the characteristics of the conduction mode and blocking mode of the device, it can be concluded that a tilt angle of 18.2° with low on-resistance characteristics while ensuring a stable breakdown voltage value is best for these simulation conditions.

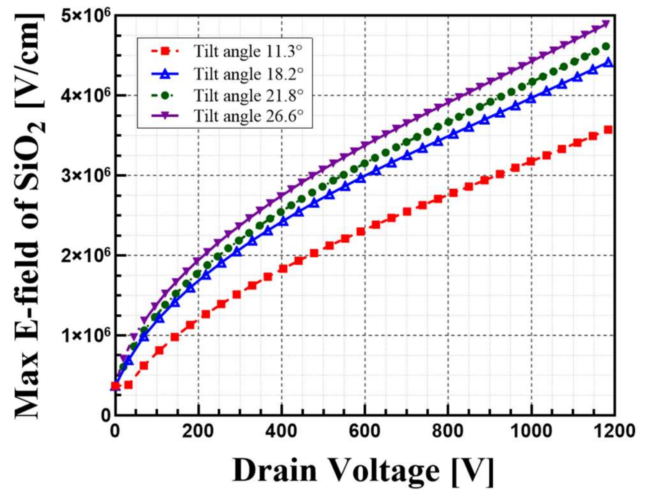

Fig. 6. Max E-field of SiO_2 in 1.2 kV SiC trench MOSFETs with tilt angles of 11.3°, 18.2°, 21.8°, and 26.6°.

A high breakdown voltage was achieved through the tilted ion implantation process, but the on-resistance increased. This was improved through the optimization of the device structure and concentration of the drift layer. In structure (b) of Figure 1, since only the left channel of the trench is used when the device is in the conduction mode, a small cell pitch is possible by reducing the right of D_{PG} in Figure 7 (b), which leads to improved specific on-resistance performance. In addition, by increasing the concentration of the drift layer from 7×10^{15} cm^{-3} to 8×10^{15} cm^{-3}, a low on-resistance of 2.8 mΩ-cm^2 and a high breakdown voltage of 1627 V were finally achieved in Figure (c).

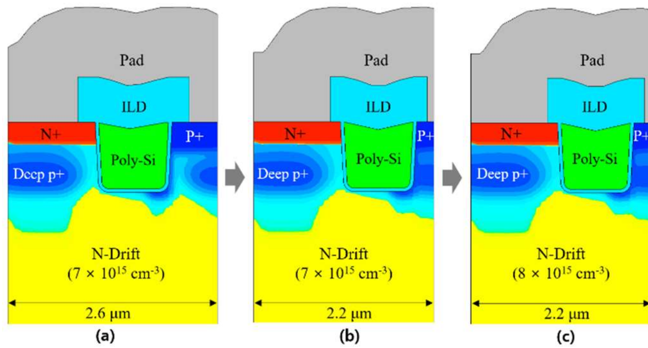

Fig. 7. The Schematic device structure of an optimized 1.2 kV SiC trench MOSFET with 18.2° tilted ion implantation p-shielding.

TABLE 2

COMPARISON OF $R_{ON,SP}$ AND BV CHARACTERISTICS OF 1.2 KV SIC TRENCH MOSFET WITH #1 18.2° TILTED ION IMPLANTATION P-SHIELDING, #2 STRUCTURE WITH REDUCED CELL PITCH AND #3 STRUCTURE WITH REDUCED CELL PITCH AND HIGH DRIFT LAYER.

Structure	Concentration of the drift layer [cm^{-3}]	Cell pitch [μm]	$R_{on,sp}$ [mΩ-cm^2]	BV [V]
#1	7×10^{15}	2.6	3.8	1577
#2	7×10^{15}	2.2	3.2	1737
#3	8×10^{15}	2.2	2.8	1627

CONCLUSIONS

In this paper, a device was designed using a Sentaurus TCAD simulation and applying a tilted ion implantation process with a structure that disperses an electric field crowded on a gate oxide. P-shielding with tilted ion implantation protects not only the sidewall of the trench but also the bottom from the electric field. The electrical characteristics of the device change depending on the tilt angle, and it was confirmed that the tilt angle 18.2° was optimized for this simulation condition, considering both the conduction mode and the blocking mode. Analysis of the electrical characteristics of the ion-implanted p-shielding at 18.2° showed a breakdown voltage of 1577 V and an on-resistance of 3.8 mΩ-cm^2. Also, a stable breakdown voltage and low on-resistance were obtained by adopting structural optimization and a high concentration of drift layer.

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ACRONYMS

SiC: Silicon Carbide
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
$R_{on,sp}$: Specific on-resistance
ILD: Inter Layer Dielectric