A new methodology to extract saturation velocity of $In_{0.53}Ga_{0.47}As$ QW HEMTs

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Abstract

In this abstract, we investigated carrier transport properties for $In_{0.53}Ga_{0.47}As$ quantum-well high- electron-mobility transistors (HEMTs), in the sense of effective mobility(μ_{n_eff}) and saturation velocity(v_{sat}). Especially, characterize that the carrier transport properties in HEMTs do not account for the effect of each individual unit process and device integration and can be challenging for short-channel devices. To do so, we proposed a methodology that explained the L_g scaling behavior of transconductance(g_m) in saturation, enabling to the extraction of values of μ_{n_eff} and v_{sat}. For a methodology of transconductance modeling, we fabricated $In_{0.53}Ga_{0.47}As$ HEMTs with L_g from 10 mm to sub-30 nm. This exhibited excellent agreement between measured and modeled g_m, yielding physically meaningful values of μ_{n_eff} and v_{sat}. To improve RF characteristics of HEMT devices, it is essential to increase g_m performance together with analysis v_{sat} using the proposed method in this work.

INTRODUCTION

Indium-rich $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ quantum-well (QW) high-electron-mobility transistors (HEMTs) on InP substrates have evinced the excellent balance of current-gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), and the lowest noise figure characteristics at all frequency regions [1-4]. Since the $In_xGa_{1-x}As$ material has electron mobility easily in excess of 10,000 cm^2/Vs at 300 K than other materials. In the meantime, many studies have shown a record of high-frequency characteristics with $In_xGa_{1-x}As$ materials, such as f_T = 738 GHz by Jo *et al*. [4], f_{max} > 1 THz by Mei *et al*. [3], and f_T = 660 GHz from metamorphic HEMTs by Leuther *et al*. [2]. Theoretically, transconductance (g_m) in saturation is a fundamental figure of merit that reflects the carrier transport properties of the $In_xGa_{1-x}As$ QW channel and thus has served as a device metric to evaluate the high-frequency characteristics of those devices. To further improve the high-frequency characteristics, higher g_m should be delivered in the devices. In fact, most of the innovative progresses on those devices have been engineered such that g_m was maximized, such as reduction of gate length (L_g), increase of the indium mole fraction (x) in the QW channel design, and optimization of epitaxial growth conditions [5-8]. Especially, the general way to evaluate carrier method is only applicated to Long-L_g. As a result, it is important to understand and improve the carrier transport properties of $In_xGa_{1-x}As$ QW HEMTs, especially at short-L_g. However, there has been little work on the saturation velocity (v_{sat}), even though v_{sat} is a parameter of primary importance for ultra-high-frequency devices.

In essence, the $In_xGa_{1-x}As$ QW HEMTs are equivalent to fully-depleted (FD) SOI MOSFETs from the electrostatic integrity point of view [14-15]. Therefore, the intrinsic transconductance (g_{m_int}) of the $In_xGa_{1-x}As$ QW HEMTs should operate the principle of a MOSFET from the mobility-relevant to the velocity-saturation regimes. Based on these facts, we aim to propose a new and simple methodology to analyze carrier transport properties for the $In_xGa_{1-x}As$ QW HEMTs from the measured g_m scaling behavior in saturation, yielding the effective mobility (μ_{n_eff}) and v_{sat}. We tested the $In_{0.53}Ga_{0.47}As$ QW HEMTs with L_g from 10 μm to 20 nm and investigate their carrier transport properties.

THEORY

The technique that will be explained in this section applies to any type of field-effect transistors, including HEMTs. Since, the extracted v_{sat} in this work is the velocity in short-channel HEMTs, which has about the same physical meaning as the velocity saturation phenomenon in short-channel Si FETs. Under the gradual-channel approximation, the gate-width normalized intrinsic transconductance (g_{m_int}) of a FET in saturation is given as follows [16]

$$\boldsymbol{g_{m\_int} = C_{gi} \cdot \left[1 - \left\{1 + \frac{2(V_{GSi} - V_T)}{E_C \cdot L_g}\right\}^{-1/2}\right] \cdot v_{sat}} \quad \cdots (1)$$

In the common-source configuration, the g_{m_int} of the FET is governed by its C_{gi}, E_C and v_{sat}. Here, C_{gi} is the intrinsic gate capacitance per unit area that includes the effect of the density-of-states (DOS) bottleneck and the quantum-mechanical nature of the channel carriers. v_{sat} and E_c are the saturation velocity and the critical field intensity of the QW channel, respectively. Note that (1) is valid from the mobility-

relevant to the velocity-saturation regimes under the assumption that the overall behavior of the channel-carrier's drift velocity under the gate with lateral electric field along the channel direction is represented by an equation of the form:

$$v_{drift} = \frac{E/E_C}{1+E/E_C} \cdot v_{sat} \quad where\ E_C = v_{sat}/\mu_{n\_eff} \qquad \cdots (2)$$

In each rage of L_g, g_{m_int} may be expressed as (3). For long gate lengths, it is dominated by C_{gi}, μ_{n_eff} and L_g per unit area such as first equation(I) at (3) , and by v_{sat} and C_{gi} in the short-channel region such as in the second equation(II) at (3).

$$\text{(I)}\ g_{m\_int} = L_g^{-1} \cdot \mu_{eff} \cdot C_{gi} \cdot (V_{GS} - V_T) \qquad \cdots (3)$$
$$\text{(II)}\ g_{m\_int} = C_{gi} \cdot v_{sat}$$

Rearranging (1) in terms of $1/L_g$, we finally obtain.

$$\left(1 - \frac{g_{m\_int}}{C_{gi} \cdot v_{sat}}\right)^{-2} = \frac{2(V_{GSi} - V_T)}{E_C} \frac{1}{L_g} + 1 \qquad \cdots (4)$$

It is important to recognize that the left-hand-side (LHS) of (4) is linearly proportional to the reciprocal of L_g and the corresponding *y-intercept* is unity. This means that one can evaluate the carrier transport properties of a QW channel by investigating the g_{m_int} in the sense of the LHS of (4) and selecting a certain value of v_{sat} that results in a condition of the *y-intercept* = 1.

Figure 1 illustrates the key technique to evaluate the carrier transport properties in this paper, where v_{sat} is determined such that the *y-intercept* of the LHS loci becomes unity. When v_{sat} is extracted from the fact that the y-intercept = 1, μ_{n_eff} is extracted from linearity, as shown in **Fig. 1**.

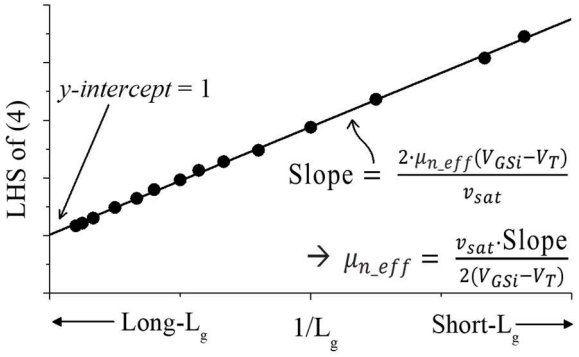


Fig. 1. Illustration of the proposed new methodology to evaluate the carrier transport properties of an FET.

According to the relationship between the intrinsic transconductance and the extrinsic transconductance with the effect of g_o considered as in [18]. g_{m_ext} can finally be expressed by the combination of the above g_{m_int} and the g_{o_ext} describing R_S and electrostatic integrity in (5). We used (5) to project the measured g_{m_ext} of fabricated devices with various value of L_g, by comparing measured and projected, and it will be mentioned later.

$$g_{m\_ext} = \left[\frac{1}{C_{gi}\cdot\left[1-\left\{1+\frac{2(V_{GSi}-V_T)}{E_C\cdot L_g}\right\}^{-1/2}\right]\cdot v_{sat}} + R_S\right]^{-1} \cdot (1 - 2R_S \cdot g_{o\_ext}) \qquad \cdots (5)$$

RESULT AND DISCUSSION

As a test vehicle in this study, we fabricated $In_{0.53}Ga_{Ga}As$ QW HEMTs as shown in **Figure 2**. **Fig. 2 (a)** illustrate the cross-sectional schematics of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ QW HEMTs. We fabricated on 3-inch InP substrates using *i*-line stepper and E-beam lithography mix-matched. **Fig. 2 (b)** and **(c)** show cross-sectional SEM and TEM images for L_g = 1 μm and L_g = 30 nm with a T-shaped gate using tri-E-beam resist, respectively. The test devices studied in this paper had a wide range of L_g from 10 μm to 20 nm. Details on the device

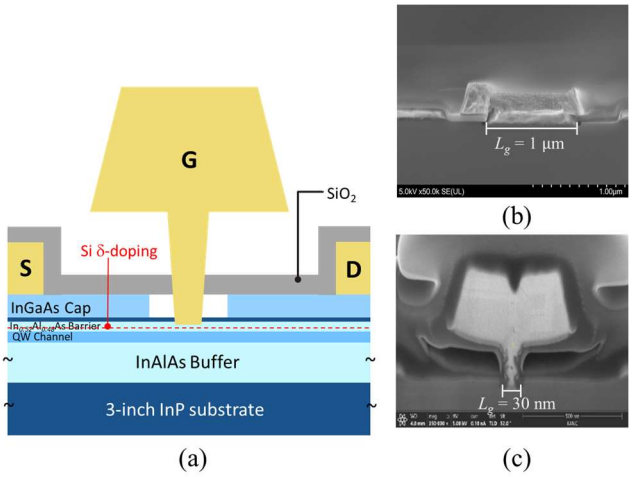
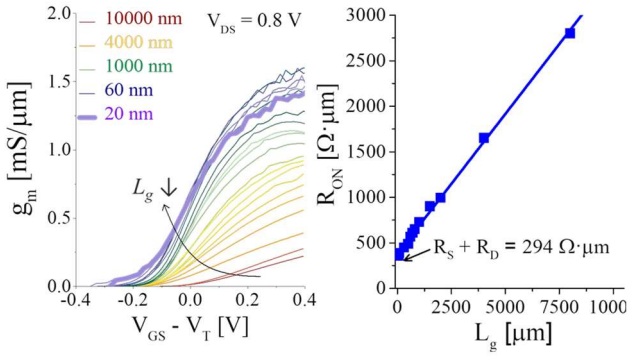


Fig. 2. (a) A schematic sketch of an $In_{0.53}Ga_{0.47}As$ QW HEMT, **(b)** cross-sectional SEM image for the fabricated L_g = 1 μm, and **(c)** cross-sectional TEM image for T-gate with L_g = 30 nm.

fabrication can be found in [17].

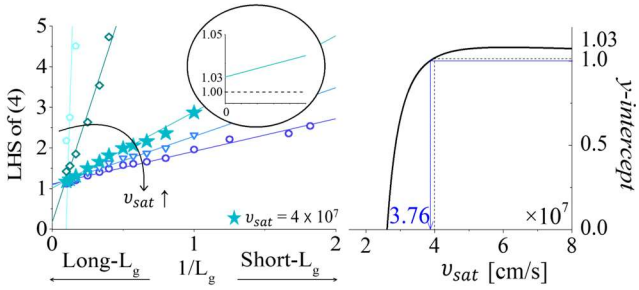
Figure 3 (a) shows g_m as a function of the gate over-drive voltage ($V_{GS} - V_T$) for $In_{0.53}Ga_{0.47}As$ QW HEMTs with various gate lengths. Note that g_m is linearly proportional to ($V_{GS} - V_T$) for long-L_g devices, whereas g_m becomes independent of the gate over-drive voltage and L_g in the limit of very short-L_g devices. **Figure 3 (b)** shows a R_{ON} as a function of *Lg*. Since R_{ON} was given by the sum of the source/drain series resistances(R_{SD}) and the channel resistance under the Schottky gate(R_{ch}), R_{ON} of the fabricated devices was scaled down linearly with L_g. Given the g_m scaling behavior above, we are now able to test the proposed technique in the section 'Theory'. In doing so, the g_{m_int} was extracted as in [18], considering the effects of the finite output conductance (g_o) that comes from either the channel-length modulation in long-L_g devices or the positive shift of V_T with V_{DS} in short-L_g devices. To experimentally extract a value of C_{gi}, we used high-frequency capacitance-voltage measurements and correlated them to the theoretical calculations, as in [20].



(a) (b)

Fig. 3. **(a)** g_m against V_{GS} - V_T at V_{DS} = 0.8 V for $In_{0.53}Ga_{0.47}As$ QW HEMTs with L_g from 10 μm to 20 nm, and (b) R_{ON} against L_g for various L_g.

Figure 4 (a) plots the LHS of (4) against the reciprocal of L_g for the $In_{0.53}Ga_{0.47}As$ QW HEMTs. Here, each curve was constructed for different values of v_{sat} (2×10^7, 3×10^7, 4×10^7, 5×10^7 and 6×10^7 cm/s). **Fig. 4 (a)** shows that all the constructed curves were linearly proportional to the reciprocal of L_g with a correlation coefficient over 0.99. And the *y-intercept* extracted from the linear dependency of each curve was approaching unity when v_{sat} was around 4×10^7 cm/s, and it was actually apart from unity for other values of v_{sat}. In fact, the choice of $v_{sat} = 4 \times 10^7$ cm/s *yielded* a value of *y-intercept* = 1.03. **Figure 4 (b)** plots the extracted *y-intercept* as a function of v_{sat} for various gate over-driving voltages, to find out a value of v_{sat} such that *y-intercept* becomes unity. Indeed, there existed a singular value of v_{sat} that led to *y-intercept* = 1. For the $In_{0.53}Ga_{0.47}As$ QW HEMTs, this condition occurred exactly for $v_{sat} = 3.76 \times 10^7$ cm/s at $V_{ov} = 0.36$ V.



(a) (b)

Fig. 4. **(a)** LHS of (4) against the reciprocal of L_g for various values of v_{sat} ,and **(b)** the extracted *y-intercept* against v_{sat}.

At this condition, the effective mobility could also be extracted from the linear slope, as explained in **Fig. 1**. This yielded a value of μ_{n_eff} = 10,500 $cm^2/V{\cdot}s$, which was very close to a value of Hall mobility (μ_{n_Hall} = 10,000 $cm^2/V{\cdot}s$) at 300 K, increasing the credibility of the proposed technique in this work. Historically, v_{sat} is difficult in defining and measuring from fabricated devices. It has been judged by the average velocity (v_{avg}) under the gate, from the delay time analysis using high-frequency S-parameter data. Besides, the $In_xGa_{1-x}As$ material systems are a direct bandgap semiconductor with low effective mass for electrons, easily yielding the velocity overshoot phenomenon at the drain side of the gate, especially for short gate lengths. However, as we previously mentioned, the v_{sat} extracted in this work is the same physical meaning as the velocity saturation phenomenon in short-channel Si FETs.

As a result, the two velocities fundamentally originated from different device physics. The extracted values of v_{sat} in this work are larger than those in the literature. This is mainly due to the $In_xGa_{1-x}As$ QW channel with short L_g do not experience Gunn effect, since the transit time (τ_{TT}) under the gate of $In_xGa_{1-x}As$ QW HEMTs is too short for the *IVS* events to occur [4, 21].

Finally, **Figure 5** compare the measured g_m and g_{m_int} of $In_{0.53}Ga_{0.47}As$ QW HEMTs to the projected ones that were constructed from (1) with values of v_{sat} and μ_{n_eff}, which were extracted as in **Fig. 4**. We compared g_{m_int} and g_{m_ext} with modeled for R_S = 147 Ω · μm, C_{gi} = 0.68 μF/cm^2 with DC measurement with table in **Fig. 5**. Both projected transconductances were in excellent agreement with the measured transconductances.

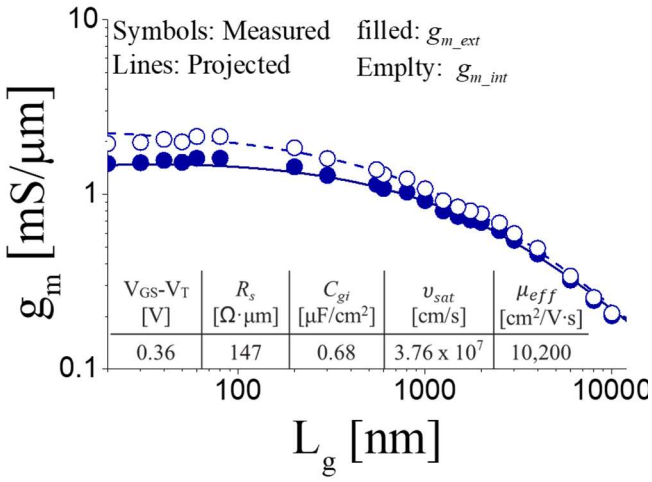


Fig. 5 Comparison of measured (symbols) to projected (lines) g_m and g_{m_int} for the $In_{0.53}Ga_{0.47}As$ QW HEMTs at V_{DS} = 0.8 V and $V_{GS} - V_T$ = 0.36 V.

After building the physical and simple model for the g_m of the fabricated devices, we assess the amount of improvement of g_m that could be achieved by reducing the R_S and enhancing the carrier transport properties. When R_S is arbitrarily entered as under 140 Ω · μm, it becomes more prominent as L_g is scaled down aggressively. Moreover, we can expect increasing g_m would be more dramatic if the carrier transport properties of the In-rich $In_xGa_{1-x}As$ QW channel were used.

CONCLUSION

In this study, for $In_{0.53}Ga_{0.47}As$ QW HEMT devices having a wide range of L_g, a methodology for deriving carrier transport characteristics (μ_{n_eff}, v_{sat}) can be derived through analytical g_m modeling composed of physical factors C_{gi}, L_g, R_S, g_{m_int}, and g_{o_ext} simultaneously and can be only used Si FET formula. So it can be applied to any type of FET. The proposed technique in this study by comparing the measured transconductances to those projected with the modeled values of μ_{n_eff} and v_{sat}. Lastly, by using the proposed new methodology in this work, we can expect further improvement on g_m by enhancing the carrier transport properties of the in-rich QW channel layer.

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REFERENCES

[1] E. Chang, C. Kuo, H. Hsu, C. Chian, and Y. Miyamoto, “InAs Thin-Channel High-Electron-Mobility Transistors with Very High Current-Gain Cutoff Frequency for Emerging Submillimeter-Wave Applications”, 2013 *Applied Physics Express*, 2013, Volume6, Number 3, doi: 10.7567/APEX.6.034001.

[2] A. Leuther, S. Koch, A. Tessmann, I. Kallfass, T.Merkle, H. Massler, R. Loesch, M. Schlechtweg, S. Saito, and O. Ambacher, "20 nm metamorphic HEMT with 660 GHZ f_T," *IPRM 2011 - 23rd International Conference on Indium Phosphide and Related Materials*, 2011, pp. 1-4.

[3] A. Vardi, L. Kong, W. Lu, X. Cai, X. Zhao, J. Grajal, and J. A. del Alamo, "Self-aligned InGaAs FinFETs with 5-nm fin-width and 5-nm gate-contact separation," 2017 *IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 17.6.1-17.6.4, doi: 10.1109/IEDM.2017.8268411.

[4] H.-B. Jo, S.-W. Yun, J.-G. Kim, D.-Y. Yun, I.-G. Lee, D.-H. Kim, T.-W. Kim, S.-K. Kim, J. Yun, T. Kim, T. Tsutsumi, H. Sugiyama, and H. Matsuzaki, "L_g = 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel HEMTs with f_T = 738 GHz and f_{max} = 492 GHz," *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 8.4.1-8.4.4, doi: 10.1109/IEDM13553.2020.9372070.

[5] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiymizu., "547-GHz f_T $In_{0.7}Ga_{0.3}As$-$In_{0.52}Al_{0.48}As$ HEMTs with reduced source and drain resistance," in *IEEE Electron Device Letters*, vol. 25, no. 5, pp. 241-243, May 2004, doi: 10.1109/LED.2004.826543.

[6] D.-Y. Yun, H.-B. Jo, S.-W. Son, J.-M. Baek, J.-H. Lee, T.-W. Kim, D.-H. Kim, T. Tsutsumi, H. Sugiyama, and H. Matsuzaki, "Impact of the Source-to-Drain Spacing on the DC and RF Characteristics of InGaAs/InAlAs High-Electron Mobility Transistors," in *IEEE Electron Device Letters*, vol. 39, no. 12, pp. 1844-1847, Dec. 2018, doi: 10.1109/LED.2018.2876709.

[7] N. Waldron, D. -H. Kim, and J. A. del Alamo, "A Self-Aligned InGaAs HEMT Architecture for Logic Applications," in *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 297-304, Jan. 2010, doi: 10.1109/TED.2009.2035031.

[8] T. Takahashi, Y. Kawano, K. Makiyama, S. Shiba, M. Sato, Y. Nakasha, and N. Hara, "Enhancement of fmax to 910 GHz by Adopting Asymmetric Gate Recess and Double-Side-Doped Structure in 75-nm-Gate InAlAs/InGaAs HEMTs," in *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 89-95, Jan. 2017, doi: 10.1109/TED.2016.2624899.

[9] U. Radhakrishna, L. Wei, D. -S. Lee, T. Palacios, and D. A. Antoniadis, "Physics-based GaN HEMT transport and charge model: Experimental verification and performance projection," *2012 International Electron Devices Meeting*, 2012, pp. 13.6.1-13.6.4, doi: 10.1109/IEDM.2012.6479038.

[10] I. Angelov, H. Zirath, and N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 12, pp. 2258-2266, Dec. 1992, doi: 10.1109/22.179888.

[11] W. R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 12, pp. 1383-1394, Dec. 1985, doi: 10.1109/TMTT.1985.1133229.

[12]M. C. Curras-Francos, "Table-based nonlinear HEMT model extracted from time-domain large-signal measurements," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 5, pp. 1593-1600, May 2005, doi: 10.1109/TMTT.2005.847049.

[13] Y. H. Chang and J. J. Chang, "Analysis of an EEHEMT Model for InP pHEMTs," *2007 IEEE Conference on Electron Devices and Solid-State Circuits*, 2007, pp. 237-240, doi: 10.1109/EDSSC.2007.4450106.

[14] D.-H. Kim, J. A. del Alamo, J. -H. Lee, and K. -S. Seo, "Logic Suitability of 50-nm $In_{0.7}Ga_{0.3}As$ HEMTs for Beyond-CMOS Applications," in *IEEE Transactions on Electron Devices*, vol. 54, no. 10, pp. 2606-2613, Oct. 2007, doi: 10.1109/TED.2007.904986.

[15] D.-H. Kim and J. A. del Alamo, "Lateral and Vertical Scaling of $In_{0.7}Ga_{0.3}As$ HEMTs for Post-Si-CMOS Logic Applications," in *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2546-2553, Oct. 2008, doi: 10.1109/TED.2008.2002994.

[16] J. A. del Alamo, "Integrated Microelectronic Devices: physics and modeling," *Pearson*, 2018.

[17] S.-W. Yun, H.-B. Jo, J.-H. Yoo, W.-S. Park, H.-S. Jeong, S.-M. Choi, H.-J. Kim, S. George, J.-M. Beak, I.-G. Lee, T.-W. Kim, S.-K. Kim, J. Yun, T. Kim, T. Tsutsumi, H. Sugiyama, H. Matsuzaki, and D.-H. Kim, “$In_xGa_{1-x}As$ quantum-well high-electron-mobility transistors with a record combination of f_T and f_{max}: From the mobility relevant to ballistic transport regimes,” *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021, pp. 11.3.1-11.3.4, doi: 10.1109/IEDM19574.2021.9720667.

[18] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's," in *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 448-450, Feb. 1987, doi: 10.1109/T-ED.1987.22942.

[19] W.-S. Park, J.-G. Kim, S.-W. Yun, H.-S. Jeong, H.-B. Jo, T.-W. Kim, T. Tsutsumi, H. Sugiyama, H. Matsuzaki, and D.-H. Kim, "Extraction of effective mobility of $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ quantum well high-electron-mobility transistors on InP substrate," *Solid-state Electronics (SSE)*, 2022, Volume 197, doi: 10.1016/j.sse.2022.108446.

[20] E. Kobayashi, C. Hamaguchi, T. Matsuoka, and K. Taniguchi, "Monte Carlo study of hot-electron transport in an InGaAs/InAlAs single heterostructure," in *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2353-2360, Oct. 1989, doi: 10.1109/16.40921.