Optical and Electrical Methods for Yield Improvement of T-Shaped Gates for AlGaN/GaN HEMT

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Abstract

The optical and electrical yield of T-shaped gates for GaN HEMT technology could be significantly improved using a combination of automated optical inspection (AOI) and electrical mapping to diagnose the origin of the defects. Using the AOI, we identified that some aligned gate metal cuts were located along a macroscopic circular line at one extremity of the wafers. Electrical parameters were defined to study the occurrence and distribution of these defects, as they typically lead to pinch-off issues. DOEs were performed at different process steps. It enabled the detection of the root cause for the failure mode. Following this study, it became possible through a process change to suppress the occurrence of the aligned gate cuts and the associated unopened gate feet, as confirmed by AOI and electrical measurements.

INTRODUCTION

United Monolithic Semiconductors (UMS) has been developing the 100 nm gate GaN-HEMT technology (GH10) for applications at and above Q-band. This technology needs to maximize its gain at this frequency range. This requires a low gate resistance combined with low source and drain parasitic capacitances. For this reason, a T-gate with a high gate foot height is desired for this technology. In this configuration, the wings of the T-gate contribute to reducing the gate resistance [1]. The high gate foot height, on the other hand, decreases the parasitic capacitance from the wings in the source and drain directions [2].

While the T-gate configuration is attractive to reaching higher RF performances, it also increases the complexity of the gate process, which could lead to a lower yield compared to a standard dielectric-assisted gate. The yield of this new gate module therefore needs to be carefully monitored and optimized [3], which is the focus of this study.

EXPERIMENTAL

The wafers in this study consist of 4″ GaN epitaxy on SiC, representative of the GH10 technology. The T-gates of the GH10 transistors were processed with a tri-layer resist stack based on electron-sensitive PMMA layers, as depicted in Fig. 1. First, the three PMMA layers were exposed by electron beam (Ebeam) lithography. Secondly, they were developed to define the foot length, the gate head width, and the undercut. Before the gate metal is deposited, the dielectric SiN layer is etched at the gate foot using the same lithography mask.

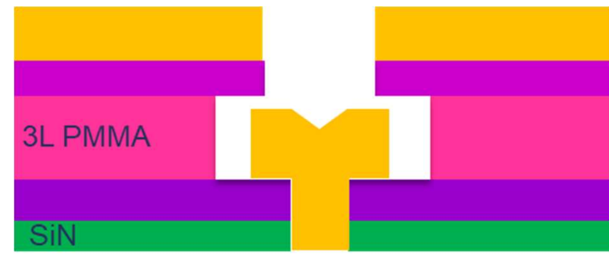

Fig. 1. Schematic representation of the T-gate processed with tri-layer PMMA, before metal lift-off.

The parameter R_gate, i.e., the electrical resistance of a gate metal line with a total length of 1825 µm, was measured on all the reticles of the wafers. The parameter $rlkPO$, used to identify pinch-off issues and defined in the next section, was calculated from measurements on 10x100µm transistors. These transistors have indeed a higher probability of having pinch-off issues due to their large gate width. Both parameters were measured or calculated from measurements performed on the wafer prober test system.

The AOI inspections were performed on a KLA-TENCOR surface inspection system. The green points on the AOI mapping refer to defects classified as non-critical since they were located outside the active area. The red points refer to critical defects found in the active area. The black points consist of defects that were not manually reviewed but which can be nevertheless considered as critical, due to their proximity to a defect classified as critical on the same reticle.

RESULTS AND DISCUSSION

The optical inspection after the gate metal lift-off of several GH10 wafers highlighted the presence of a particular defect pattern. We observed some aligned gate defects, as

seen in Fig. 2a. There was generally one defect per gate finger, at a similar location. The SEM inspection of these gate defects revealed the presence of a gate metal cut (Fig. 2b). The SiN at the gate foot opening was also not well etched at this position.

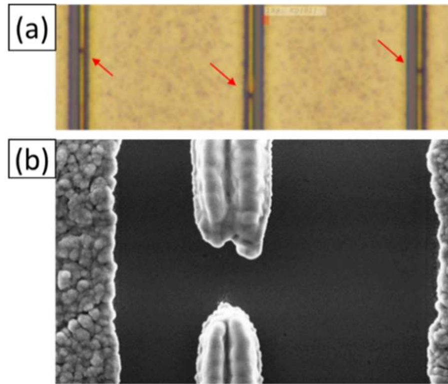

Fig. 2. Typical optical picture representing (a) the aligned gate cuts and (b) the associated SEM picture.

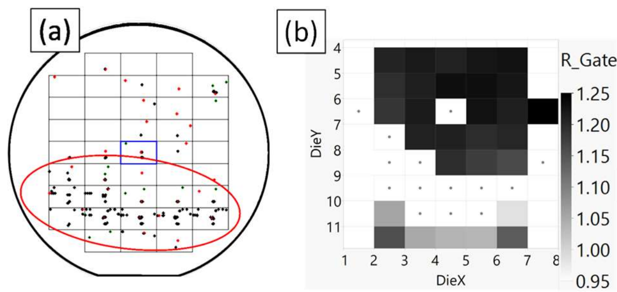

Fig. 3. AOI mapping (a) and electrical mapping of the parameter R_gate (b) on the same GH10 wafer.

To understand the distribution of these defects, automatic optical inspection (AOI) measurements were performed systematically on the GH10 wafers after gate metal lift-off. The aligned gate cuts appeared to be confined in a specific area of the wafer, as indicated in Fig. 3a. These defects formed a macroscopic ellipsoidal defect trace at one extremity of the wafer. The electrical mapping of the parameter R_gate for the same wafer is displayed in Fig. 3b. The R_gate values in Fig. 3a are normalized by the average value of this parameter across the wafer. The black dots on the mapping correspond to positions where the compliance of the measurement had been reached, which is typically the case when one or several gate cuts are present on the gate line. Due to the long gate line length of the measured structure, there is a high probability of having a gate cut in this structure on a reticle affected optically by the gate cut trace. Thus, the electrical mapping of R_gate mirrors the defect trace found on the AOI mapping very well. Comparing the AOI and the electrical mapping of R_gate, it became easy to confirm the presence of the gate metal cut trace without having to review all the pictures for all wafers manually.

Scanning Electron Microscope (SEM) inspection is typically done on GH10 after gate foot etching to check the dimension and quality of the foot opening. On several wafers, we observed locally some SiN residues in the foot opening (Fig. 4a). At other positions, we observed that the bottom PMMA of the three-layer resist was locally not opened or not developed successfully (Fig. 4b). It is reasonable to think that SiN residues in the foot opening originate from remaining resist at this location, which prevented the etching of the SiN. These defects are typically not visible in AOI after the gate metal lift-off. The thickness of the remaining SiN and bottom resist is indeed too small to create a sufficient contrast once the metal is deposited on the top. These defects also do not lead in most cases to a real gate metal cut since the metal can still be deposited in the three-layer opening. They are nevertheless undesired since they typically lead to pinch-off issues, the gate foot metal being not in direct contact with the semiconductor.

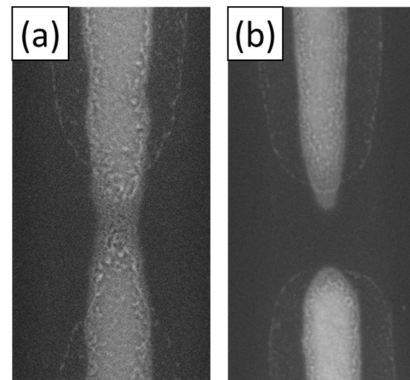

Fig. 4. SEM pictures of (a) unopened gate foot with SiN residues and (b) unopened bottom PMMA.

The transistors with local residues in their foot opening are expected to display some pinch-off issues close to the threshold voltage Vt. The transistor should eventually pinch-off at lower Vgs voltages, the applied field being sufficient to close the channel, even at positions where the gate metal foot is not directly in contact with the semiconductor. To get an idea of the pinch-off quality, the parameter $rlkPO$ was defined as $rlkPO = I(Vt - 1V)/I(-7V)$, where $I(Vt - 1V)$ is the current at $Vgs = Vt - 1V$ and $I(-7V)$ the current at $Vgs = -7V$, for a Vds of 10V. The threshold voltage Vt is arbitrarily defined as the voltage at which the drain current Ids is equal to $1 mA.mm^{-1}$. The position of Vt and $Vt - 1V$ is indicated on Fig. 5 for two different GH10 transistors on the same wafer. The transistor with the red transfer characteristic curve typically displays a pinch-off issue. The calculated $rlkPO$ for this transistor will be much above 1, since the current at $Vgs = Vt - 1V$ is much higher than the current measured at -7V. On the contrary, the parameter $rlkPO$ for

the green curve, which does not display pinch-off issue, will be below 1. The parameter $rlkPO$ can therefore be used as an indicator for the pinch-off quality with $rlkPO < 1$ defined as the criteria for good pinch-off. This parameter presents the advantage of being independent of the leakage level of the transistor, which could vary from wafer to wafer if process variations are being tested, which is typically the case with a technology in development.

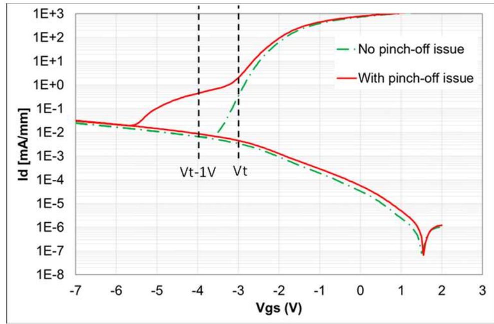

Fig. 5. Transfer characteristic of two GH10 transistors

The electrical mapping of the parameter $rlkPO$, measured on 10x100µm transistors on a GH10 wafer, is displayed in Fig. 6b. It can be observed that there exists a region with $rlkPO$ values well above 1. This region corresponds to the position of the gate metal cut trace, observed in AOI on the same wafer (Fig. 6a). It is important to mention that transistors that did not have optical defects also displayed large $rlkPO$ values when located in this region. The parameter $rlkPO$ could also not be calculated on several positions on the wafer. This is due to gate metal cuts which make it impossible for the transistor to pinch-off. In this case, it is impossible to extract Vt and therefore to calculate $rlkPO$. The transistors outside of the gate cut trace region displayed $rlkPO$ values lower than 1, signalling that they pinch-off correctly. This result suggests that the unopened gate feet and the gate metal cuts share the same origin. It also indicates that a transistor without apparent gate cut in AOI could nevertheless be affected by SiN or resist residues in the gate foot, leading to pinch-off issues if it is in a region around the gate cut trace.

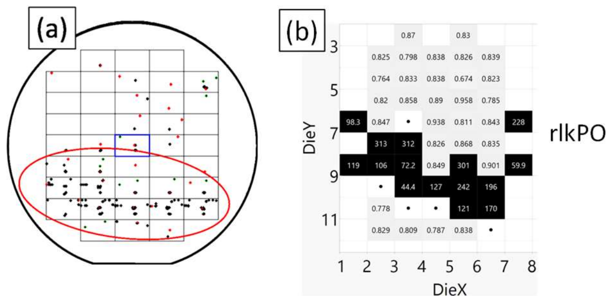

Fig. 6. AOI mapping (a) and electrical mapping (b) of the parameter $rlkPO$ on the same GH10 wafer.

Several tests were performed to investigate the origin of the gate metal cuts and residues in the foot opening. After several trials, the position of the gate cut trace could be changed by rotating the wafers by 180° at the critical process step (Fig. 7a, b). The distance of the gate cut trace from the wafer border could also be modified through process variations (Fig. 7a, c). With this understanding, it became possible to confine the gate metal cut trace at the very extremity of the wafers, where no chips are delivered on our qualified technologies.

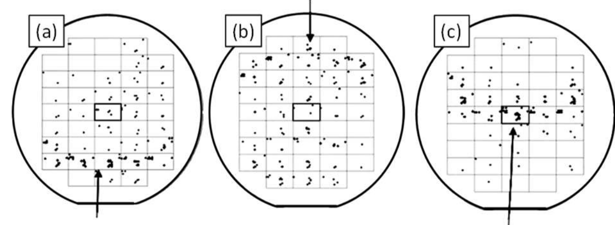

Fig. 7. AOI mappings of three different GH10 wafers. Intentional process variations could modify the position of the gate cut trace.

The trend chart of Fig. 8 displays the number of error codes in the measurement of the parameter R_gate. It can be seen that the number of error codes signalling the presence of a gate cut on this structure is significantly decreased after the implementation of the process change. This confirmed that the origin of the gate cuts was well understood and that the corrective action had been effective.

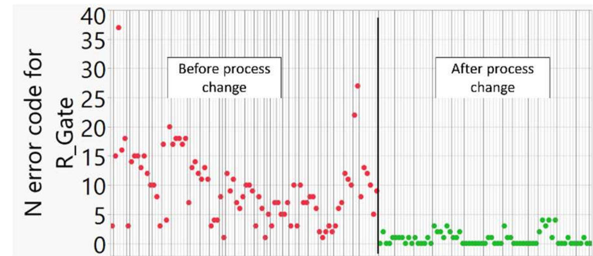

Fig. 8. Number of error codes in the measurement of R_gate, associated to gate metal cuts, before and after the process change.

A few error codes for the parameter R_gate were still found on some wafers, even after the implementation of the process change (Fig. 8, Fig. 9). In this case, the AOI and R_gate mapping show the presence of a few gate cuts in the anti-flat region of the wafer. The orientation of the wafers has been fixed following the implementation of the process change in a way that the gate cut trace should always appear at the extremity of wafer's anti-flat. This should facilitate future defect root cause analyses since these aligned gate cuts can be excluded elsewhere on the wafer.

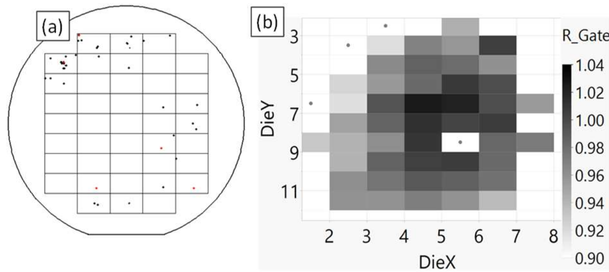

Fig. 9. Typical AOI mapping and associated electrical mapping for the parameter R_gate after the process change.

The trend chart in Fig. 10 displays the percentage of reticles with $rlkPO$ values above 1. It can be seen that the implementation of the process change significantly reduced the number of pinch-off issues on the wafer, indicating that the residues in gate foot openings should be less frequent. Some reticles still displayed $rlkPO$ values above 1. A few of them could be associated with the metal gate cut trace at the wafer's anti-flat. Other affected positions were distributed at random locations on the wafers. It is important to note that some substrate and process variations could also lead to pinch-off issues, independently of the gate cut trace issue described in this study. The parameter $rlkPO$ will be further monitored to continuously control and improve the ability of the transistors to pinch-off correctly.

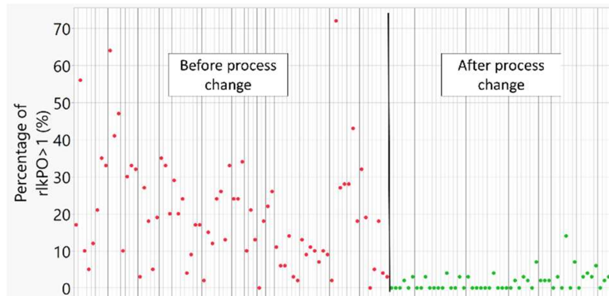

Fig. 10. Percentage of measured transistors with $rklPO$ values above 1, associated to pinch off issues, before and after the process change.

Conclusions

In conclusion, this study shows that a combination of AOI and electrical mappings could greatly facilitate the defect root cause analysis of tri-layer-based T-gates. Following this analysis, the implementation of a process change resulted in a significantly improved yield of the gate module on the GH10 technology. The efficiency of the corrective action can be well demonstrated with the trend chart of the parameters R_gate and $rlkPO$. This confirmed further that the gate metal cut trace and the unopened gate foot share a common origin, even if an unopened gate foot does not always lead to a gate cut visible in AOI. The parameters R_gate and $rlkPO$ are still being monitored for continuous process yield optimization.

Acknowledgements

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Acronyms

DOE: Design of Experiments
SEM: Scanning Electron Microscope
HEMT: High-Electron-Mobility Transistor
AOI: Automated Optical Inspection
PMMA: Poly(methyl methacrylate)