L_g = 25 nm $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ High-Electron Mobility Transistors on InP Substrate with Both f_T and f_{max} in Excess of 700 GHz

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Keywords: Cut-off frequency (f_T), maximum oscillation frequency (f_{max}), high-mobility-transistor (HEMT), $In_xGa_{1-x}As$

Abstract

We present an L_g = 25 nm $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ HEMT on a 3-inch InP substrate that delivers excellent high-frequency characteristics. The device exhibited a value of maximum transconductance (g_{m_max}) = 2.4 mS/µm at V_{DS} = 0.5 V and on-resistance (R_{ON}) = 294 Ω·µm. At V_{GS} = 0.15 V and V_{DS} = 0.5 V, the same device displayed an excellent combination of cut-off frequency (f_T) = 709 GHz and maximum-oscillation frequency (f_{max}) = 702 GHz. At its core, the indium-rich $In_{0.8}Ga_{0.2}As$ composite channel with superior Hall mobility (μ_{n_Hall}) of 13,500 $cm^2V^{-1}s^{-1}$ at 300 K was implemented, and the gate length (L_g) was successfully scaled down to 25 nm while maintaining the electrostatic integrity of the device.

INTRODUCTION

As predicted by Edholm's law, wireless data rates have doubled every 18 months over the past three decades [1]. The evolving sixth-generation (6G) wireless communication technologies will demand higher operating frequencies of around 300 GHz with data rates approaching 0.1 Tbps [2-3]. To meet this pressing requirement, semiconductor transistor technologies must be advanced in terms of noise and power efficiency at these frequencies in o rder to continue supporting the development of digital communications systems. This acquires a semiconductor transistor technology with THz operation speed.

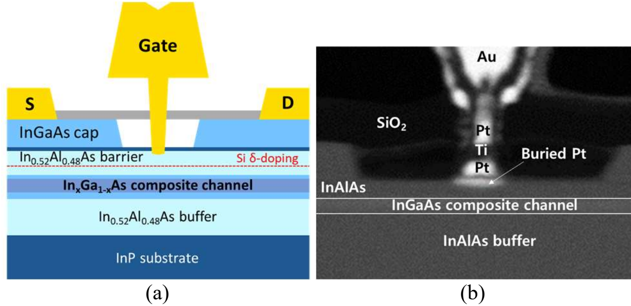
Indium-rich (x > 0.53) $In_xGa_{1-x}As$ high-electron mobility transistors (HEMTs) on an InP substrate have shown great success for various low-noise and ultra-high-frequency applications from microwave to sub-millimeter-wave (sub-MMW), such as security/medical imaging system, collision avoidance radar, wireless local area networks (WLANs) and especially next-generation telecommunications [4-6]. To fully exploit the sub-MMW band, there is an immediate need to develop semiconductor transistor technologies that are capable of processing a signal in the sub-MMW regime. In this work, we demonstrated an L_g = 25 nm $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ quantum-well (QW) HEMT on a 3-inch InP substate with an outstanding combination of DC and high-frequency characteristics.

FABRICATION PROCESS

The epitaxial layer structure used in this work was grown on a 3-inch semi-insulating InP substrate using metal-organic chemical-vapor-deposition (MOCVD). From top to bottom, the epitaxial layer structure consisted of a 30 nm thick heavily-doped multilayer cap structure with n+ $In_{0.53}Ga_{0.47}As$ and n+ $In_{0.52}Al_{0.48}As$, a 3 nm thick InP etch-stopper, a 9 nm thick $In_{0.52}Al_{0.48}As$ barrier/spacer with Si δ-doping, a 9 nm thick indium-rich $In_{0.8}Ga_{0.2}As$ QW channel, and a 200-nm $In_{0.52}Al_{0.48}As$ buffer on the InP substrate. Details on the material growth were reported in Ref. 7. Key aspects are as follows: (i) a multi-layer cap design to lower S/D ohmic contact resistance, and (ii) an $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ (1/5/3 nm) composite-channel to improve carrier transport properties. As reported previously [7], the Hall mobility (μ_{n_Hall}) was measured to be 13,500 $cm^2V^{-1}s^{-1}$ with a two-dimensional electron gas density (n_{2-DEG}) of approximately 3×10^{12} cm^{-2} at room temperature.

The process started with device isolation via mesa etching with a diluted H_3PO_4-based wet etching solution. Source-to-drain spacing (L_{SD}) was scaled down to 0.8 µm and a non-alloyed metal stack of Ti/Mo/Ti/Pt/Au (5/10/10/10/25 nm) was used to form S/D ohmic contacts. Here, we intentionally thinned the thickness of S/D ohmic metals down to 60 nm, to obtain a uniform coating of the first ZEP e-beam resist in the tri-layer e-beam resist scheme during a T-gate e-beam lithography process step. After a contact pad formation of Ti/Au (20/500 nm), a 20-nm thick SiO_2 by plasma-enhanced-chemical-vapor-deposition (PECVD) was formed in between the source and drain ohmic contacts. After a gate recess process, a SiO_2-assisted T-gate with a metal stack of Pt/Ti/Pt/Au was created using a JBX-9300FS e-beam lithography machine with 100 kV, where the T-gate was placed in a tightly spaced source and drain with less than 50 nm alignment accuracy.

Fig. 1 (a) and (b) shows a schematic cartoon of an $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMT on an InP substrate with the composite channel and a cross-sectional transmission-electron-microscope (TEM) image after the gate process. The device fabrication was nearly the same as in the previous report from our group [8]. This is a two-step recess process with a gate-to-channel distance, t_{ins}, of approximately 5 nm. Source-to-drain spacing (L_{SD}) was scaled down to 0.8 µm, and a non-alloyed metal stack of Ti/Mo/Ti/Pt/Au (5/10/10/10/200 nm) was used to form S/D ohmic contact. After a gate recess process, a SiO_2-assisted T-gate with a metal stack of Pt/Ti/Pt/Au was formed.



(a) (b)

Fig. 1. (a) Cross-sectional schematic and (b) STEM image of an $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMT on InP substrate.

DEVICE PERFORMANCE

Since the fabricated $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMT in this work adopts the non-alloyed source and drain ohmic contacts, the overall source resistance (R_S) is a function of the actual source-to-gate spacing (L_{gs}), sheet resistances of the cap layer (R_{sh_cap}) and the channel layer (R_{sh_ch}), the ohmic metal contact resistivity to the multi-layer cap (ρ_c) and the barrier tunneling resistivity ($\rho_{barrier}$) through the $In_{0.52}Al_{0.48}As$ barrier layer [9]. To extract all the parameters in R_S, we have designed two separate test patterns. One is a conventional regular cap TLM device and the other is called a recessed TLM device with various L_{gs} and L_g dimensions to extract R_{sh_ch} and $\rho_{barrier}$. Armed with the extracted values of those parameters, it was possible to predict the R_S with various dimensions of L_{gs}. Fig. 2 compares the measured and modeled R_S as a function of L_{gs}, showing that the modeled R_s is in excellent agreement with the measured one. The results also reveal that there is almost no decrease in R_s even with L_{gs} scale down to 0.5 µm and below. Based on these findings, the dimension of L_{ds} was designed to be 0.8 µm in this experiment to achieve a sufficiently low R_S.

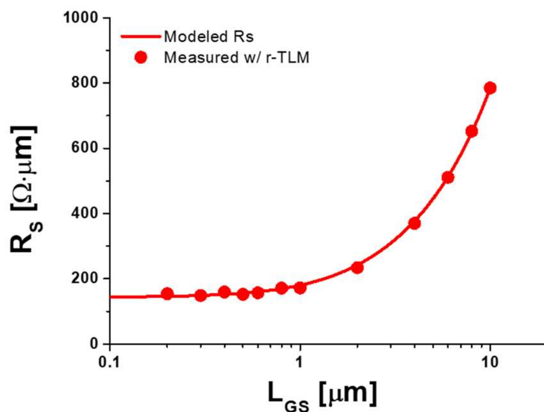


Fig. 2. Comparison of the modeled and measured R_s against L_{gs}.

Fig. 3 (a) shows the DC output characteristics of our representative $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMTs with L_g = 25 nm. The measured R_{ON} is less than 300 Ω·µm from the output characteristics, which was due to the combination of the capping layer design and the optimized ohmic process. The ohmic contact resistance (R_c) of approximately 40 Ω·µm was measured from the transmission-line-method (TLM). As shown in Fig. 3 (b), the same device delivered the maximum transconductance (g_{m_max}) of 2.4 mS/µm at V_{DS} = 0.8 V.

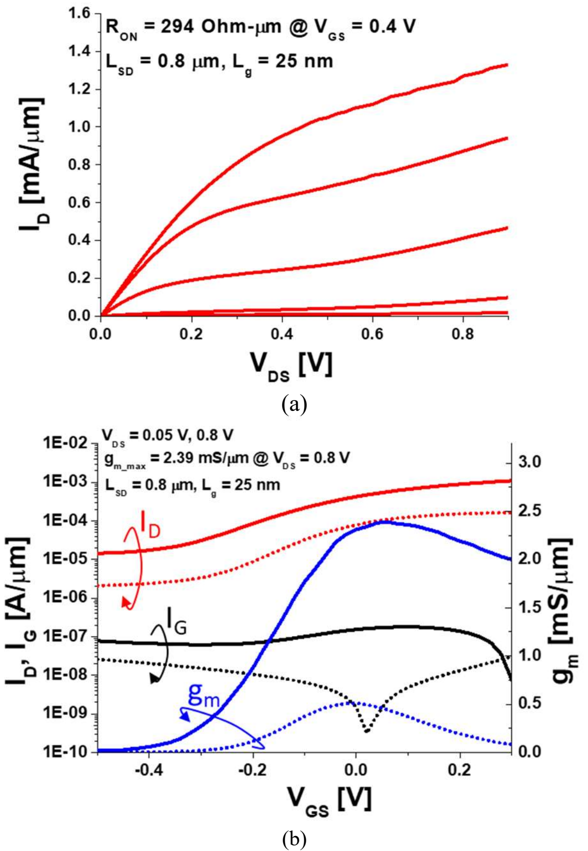


Fig. 3 (a) Output characteristics and (b) subthreshold and transconductance (g_m) characteristics at V_{DS} = 0.05/0.8 V of the fabricated $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMT with L_g = 25 nm.

The microwave characteristics of our representative $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW-HEMTs were characterized from 1–67 GHz using an Agilent PNA system with off-wafer

calibration. On-wafer open and short patterns were utilized to subtract pad-related capacitance and inductance components from measured scattering parameters (S-parameters) [10]. Fig. 4 plots a measured short-circuit current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g), and a maximum stable gain (MSG) after de-embedding pad-related parasitic components for the fabricated device with L_g = 25 nm and W_g = 2 × 20 μm at V_{DS} = 0.5 V and V_{GS} = 0.15 V near the peak g_m bias condition. An excellent combination of f_T = 709 GHz and f_{max} = 702 GHz was obtained by extrapolating $|h_{21}|^2$ and U_g with a slope of -20 dB/decade.

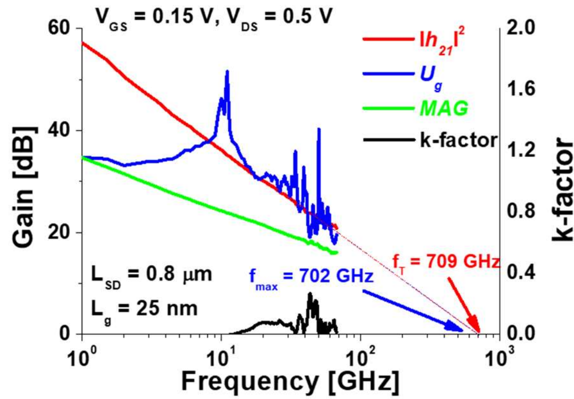


Fig. 4. Measured (Solid lines) and extrapolated RF gains (dashed lines) for the L_g = 25 nm InGaAs/InAlAs HEMT at V_{DS} = 0.5 V and V_{GS} = 0.15 V.

Conclusions

In this work, we have demonstrated the L_g = 25 nm $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW-HEMT technology that yielded outstanding g_{m_max} = 2.4 S/mm and high-frequency characteristics such as f_T = 709 GHz and f_{max} = 702 GHz at V_{DS} = 0.5 V. These results came from minimizing the contact resistance (R_C) and scaling L_{SD} down to 0.8 μm, coupled with the use of the indium-rich $In_{0.8}Ga_{0.2}As$ composite channel design scheme.

Acknowledgements

This work has been sponsored by Samsung Research Funding & Incubation Center of Samsung Electronics under SRFC-IT2201-07.

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