Plasma Dicing of thin-film LEDs

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Abstract

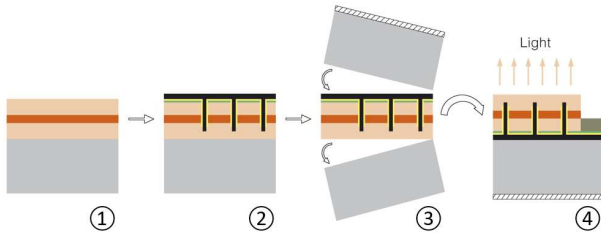
In the semiconductor industry wafer dicing, also known as die singulation, has been traditionally conducted using methods, like mechanical sawing and laser techniques. But these methods reveal various drawbacks and limitations. There is a risk of chipping or cracking from the saw approach, and slag, ablation damage as well as heat affected zones (HAZ) from the laser [1]. This damage cannot be totally avoided, and therefore implicate the need for an exclusion zone, which isolates the active die from these incidents. Further space is used to provide a sufficiently wide dicing street for the singulation medium (e.g., saw blade or laser spot) to move across the wafer. Although the described damage could be mitigated by reduced dicing speed, it always results in compromises in pattern density and throughput. Especially the trend for thinner wafers and smaller die sizes for various applications (power devices, LEDs, etc.) renders them less cost effective and sometimes even not applicable anymore. These issues could be overcome by using plasma etching for wafer singulation. In this paper we will describe the plasma dicing flow implemented for our latest generation thin-film LEDs.

Introduction

In the early 2000s for silicon-based devices the idea of applying plasma etching for wafer dicing was proposed [2]. The according silicon etching is based on the time multiplexed deep reactive ion etching technique (DRIE, or so-called BOSCH process), which was originally developed for applications in MEMS or TSV formation [3]. This technique can achieve very deep and narrow trenches in silicon with high selectivity to common mask materials such as photoresist, polyimides, and dielectric films (e.g., silicon dioxide). Since the introduction of our thin-film LED technology, also for us plasma dicing came into the game.

The basic steps of our thin-film LED approach are shown in Fig. 1. A III-V epitaxial layer stack is grown on a suitable substrate (e.g., Sapphire, GaAs), followed by mirror and contact formation. Thereafter the epitaxial film is transferred to a silicon wafer by eutectic bonding followed by the removal of the original growth substrate, and then completed by final chip processing [4].

In the following we will depict the plasma dicing process flow for our latest generation thin-film LEDs, the associated advantages and implementation challenges.



① Epilayer growth on substrate (e.g. Sapphire, GaAs)
② Mirror and contact formation
③ Transfer to Silicon carrier and substrate removal
④ Final chip processing

Fig. 1. ams-OSRAM thin-film technology approach.

Plasma Dicing flow

Our plasma dicing approach is based on a hybrid method in combination of both ultrafast pulse laser grooving and DRIE plasma etching [5]. In Fig. 2 the corresponding fundamental plasma dicing process flow is shown. After silicon wafer thinning (down to a thickness of 120µm) and backside metallization the wafer is mounted on an industry standard tape frame [6], then a water-soluble, in-house customized polyvinyl alcohol (PVA) based protecting layer is applied on the structured frontside of the wafer (Fig. 2a). Water-soluble polymers as resist mask have two attractive characteristics for our dicing application: 1) They can be deposited conveniently by spin-coating, air-dried and the solvent removed at a low temperature, and 2) the resulting layer can be dissolved in water; no corrosive reagents or organic solvents are needed.

The utilized frames are typically reusable stainless steel or plastic. They have no impact on the process result, however the temperature of the frame must be actively managed to maintain the properties of the attached tape. For wafer mounting various commercially available tapes can be used. The choice depends on the reaction of film and adhesive to plasma conditions and the functionality of next process steps (like re-taping). The quality of the tape/wafer interface is also a critical property for plasma dicing, whereas it is not such an issue for the traditional dicing techniques. Any trapped volumes will expand in vacuum (creating “bubbles”) and so this part of the wafer is removed from the cooling surfaces causing loss of temperature control. As a result, the tape can

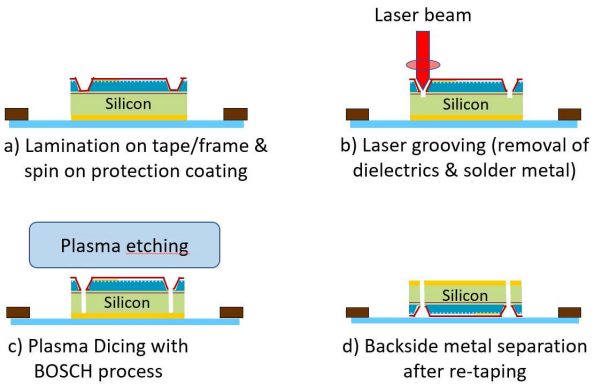


Fig. 2. Plasma dicing process flow.

burn causing the ultimate loss of the wafer. Hence it is essential for the taping process to ensure the tension of the tape and the mounting procedures and equipment are such that creasing or slackening of the tape is avoided. With this precaution trapping of gases will be prevented, and "bubbles" would not appear.

In the next step the dicing street will be uncovered from dielectric films and solder metals by short pulse laser grooving to reveal the silicon beneath. (Fig. 2b). The standard DRIE process that is employed to etch silicon is ineffective for etching metals. To provide non-metal dicing streets ultrafast pulse laser grooving was chosen because it turned out, that wet and dry etching were not applicable here.

Depending on the characteristics of laser irradiation, the optical reaction with materials can be drastically different. Within ultrafast time scale e.g., nano-, pico- or femto-second, the peak laser pulse power can be very high and pass over the non-linear absorption threshold. Therefore, a highly focused ultrafast pulse laser beam can create a very clean lesion at the focal point i.e., a near "cold" ablation with no or only minimal heat affected zone (HAZ), not only in materials such as silicon

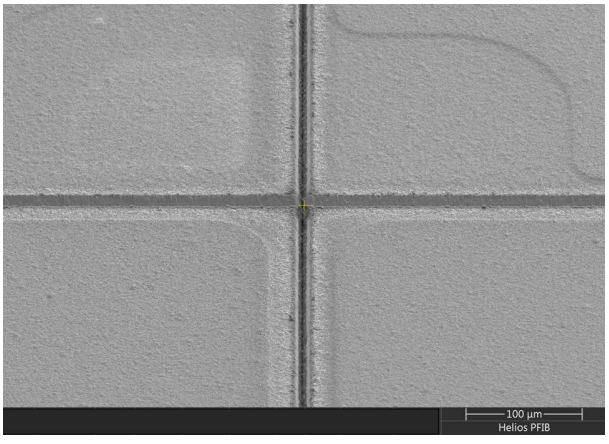


Fig. 3. Top view SEM image of a dicing street after short pulse Laser Grooving.

and sapphire but also opaque metals [7]. To achieve "cold" ablation apart from time scale, also other machine parameter such as laser power, focal depth, and feed speed must be adjusted properly. The applied laser grooving process generate a V-shaped groove with a kerf width at the silicon of about 6µm. As shown in Fig. 3, the formed edges of the dicing streets exhibit a certain roughness, they are not as sharp as using photolithography.

After laser grooving the silicon is etched all the way down to the backside metal by time multiplexed DRIE (so-called BOSCH process) using SF_6 and C_4F_8 process gases (Fig. 2c). Unlike standard plasma etching processes it consists of a reiterating three-step cycle:

1) C_4F_8 based fluorocarbon polymer film deposition.
2) Bottom fluorocarbon polymer film etching with SF_6.
3) Isotropic silicon etching with SF_6.

In the deposition process, a CF-based fluorocarbon polymer passivation film is deposited on the sidewalls and bottom surface of the trench. In the bottom film etching step, the fluorocarbon polymer film on the trench bottom is etched anisotropic. In the last process step, only the silicon at the bottom of the trench, where the polymer film has been removed, is etched isotropic. This approach allows for producing deep features with exceptional anisotropy, etch-rate, and etch mask selectivity. Moreover, repeatable and reliable etching is ensured with OES end-point detection (EPD) using the silicon byproduct emission line at 440nm. As the plasma process stops on metal, there is no need for any protective measures to avoid notching on the lower chip edge [9][10]. During processing the wafer and tape frame are clamped by an electrostatic chuck (ESC) and kept at low temperature (< 70°C) via He backside cooling, preventing heat damage to the tape. Typically, our wafer shows a noticeable warpage, so without an ESC the wafer temperature may rise above the applicable temperature of the tape and then the tape may melt. After re-taping the backside metal in the dicing streets is removed by a proprietary process, and so the dies are fully separated. Another re-taping step is needed to allow the removal of the frontside PVA mask by a de-ionized water-based cleaning process, lastly followed by final visual inspection.

Benefits and Implementation Challenges

A) More dies per wafer

Compared to the so far used full-cut laser dicing the implementation of plasma dicing exhibit advantages in terms of cost and quality. The shrinkage of the exclusion zone and dicing street, which means more dies per wafer, results in markedly cost reduction, especially for small dies [1]. The gain in good die per wafer can be estimated with equation (1) and afterwards translated in a percentage increase, shown in Fig. 4.

$$DPW = \frac{\pi}{4}\left(\frac{D}{d+w}\right)^2 - \frac{\pi}{\sqrt{2}}\left(\frac{D}{d+w}\right) \qquad (1)$$

Where DPW is the good die per wafer, D is the usable diameter of the wafer, d is the width of the square die, and w is the width of the dicing streets [11]. Especially for die sizes within the typical range for LEDs, the gain in die per wafer and so the reduction of dicing cost-of-ownership is quite significant.

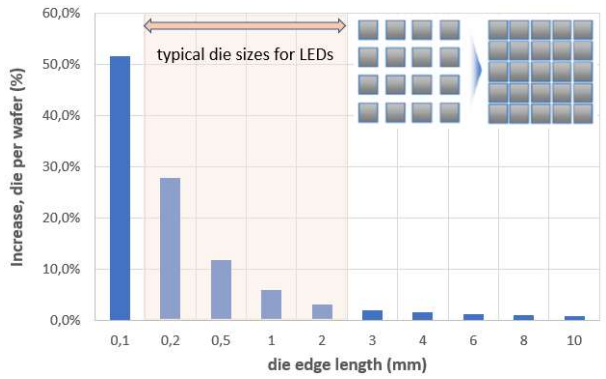


Fig. 4. Calculated percentage increase in available complete good die versus die size through a 30µm reduction of the dicing street widths (see inlet picture). Wafer size is 150mm with 2mm edge exclusion.

B) Chip size independent throughput

Plasma dicing processes can have a significant throughput advantage over conventional saw and laser-based processes. In contrast to serial sawing and laser processes, plasma etching is a parallel process that etches all exposed trenches across the wafer simultaneously, which results in significantly shorter process times for smaller die (less than 2mm edge length) and thinner wafers (less than 250µm thick). In addition, the process times are almost independent of chip size. Plasma dicing throughput continues to increase as the wafer thickness decreases and, unlike conventional dicing technologies, there is no lower limit regarding chip size and/or wafer thickness.

C) Improved die fracture strength

Due to the brittle nature of silicon, particularly thinned silicon wafers are mechanically extremely fragile. Die fracture occurs via crack propagation along the surface or from within the material itself. To achieve high die fracture strength, it is critical during the singulation process that no sidewall damage (i.e., cracking or chipping) occurs. The plasma dicing process removes the silicon by turning it into a gas without any mechanical or thermal stress resulting in almost defect-free sidewall surfaces. Fig. 5 summarizes the measured die fracture strengths for diced 1mm x 1mm dies on 120µm thick silicon wafer by laser dicing and plasma-based dicing. The die fracture measurements are done using the 3-point bending method. As the results indicate, the plasma-based technique has up to factor 2 higher die fracture

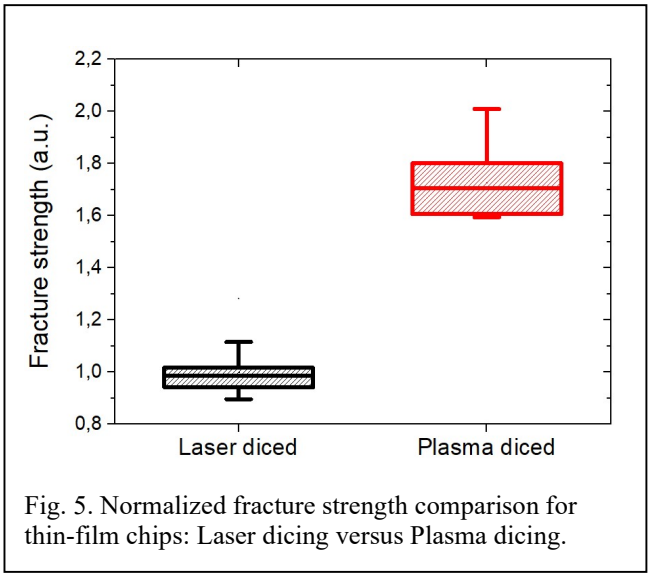


Fig. 5. Normalized fracture strength comparison for thin-film chips: Laser dicing versus Plasma dicing.

strength compared to our laser-based dicing. Therefore, the probability of die cracking during package assembly, reliability tests, and operation life is significantly reduced. This asserts a key benefit of the plasma-based technique compared to the conventional methods.

D) Implementation challenges

Although anisotropic high aspect ratio deep silicon etching using the BOSCH process is usually straightforward on wafer level using lithographically generated etch masks, there were some challenges to overcome during the implementation of the plasma dicing technology for our thin-film LED devices.

Initially, the plasma process must be adapted to the used tape frames, to avoid tape overheating and to keep tape properties, so that downstream processes like re-taping are still working flawlessly.

Both, the narrow dicing street width (~ 6µm), and the noticeable edge roughness of the dicing streets after laser grooving (see Fig. 3) could badly influence the integrity of the chip sidewall (headword "scallop collapse"), especially on the top area of the chip [8]. Worst case of such sidewall deterioration could end up in distinct lateral undercut beneath the solder metal on top of the chip. But lowering the laser grooving caused dicing street edge roughness and particularly a well-tuned DRIE process could manage this.

Furthermore, the width of the etched trench at the bottom of the chip must comply with a certain lower limit, otherwise the backside metal removal in the dicing streets, especially for micrometer range thicknesses, is not functional. For this reason and to ensure a faultless chip sidewall, the parameters of each BOSCH process step must be optimized and properly matched.

Fig. 6 shows an SEM image of a plasma diced thin-film chip. The wavy topography (so-called scallops) at the

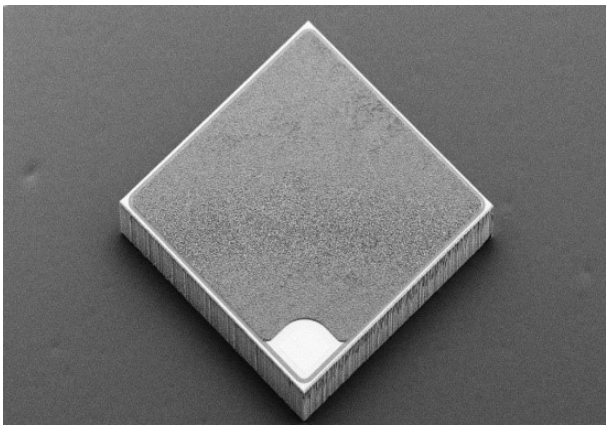


Fig. 6. SEM image of a plasma diced thin-film LED chip.

sidewall is formed due to the repeat of etching and passivation during the DRIE process, whereas the vertical striations are caused by the roughness of the dicing streets provoked by the laser grooving process.

CONCLUSIONS

We described the implementation of a DRIE-based plasma dicing process for our latest generation thin-film LEDs. Despite some integration challenges, plasma dicing offers considerable benefits for die singulation, namely increased and almost die size independent throughput, more dies per wafer and improved die quality/strength. Hence, plasma dicing has what it takes to become future benchmark technology for applications seeking to increase die strength, throughputs and yields for small and/or thinned fragile dies on various wafer diameters (150mm up to 300mm).

ACKNOWLEDGEMENTS

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ACRONYMS

DRIE: Deep Reactive Ion Etching
EPD: endpoint detection
HAZ: Heat Affected Zone
LED: Light Emitting Diode
MEMS: microelectromechanical systems
OES: optical emission spectroscopy
PVA: Polyvinyl alcohol-based resist material
SEM: scanning electron microscope
TSV: through silicon via